



Vikas Kumar Thawani

Table of Contents

1 Overview	2
2 Functional Safety Failure In Time (FIT) Rates	3
2.1 8-DWV (wide-body SOIC) Package.....	3
2.2 16-DW (wide-body SOIC) Package.....	4
3 Failure Mode Distribution (FMD)	5
4 Pin Failure Mode Analysis (Pin FMA)	6
4.1 8-DWV Package.....	6
4.2 16-DW Package.....	9

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for ISO1042-Q1 (8-DWV and 16-DW package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

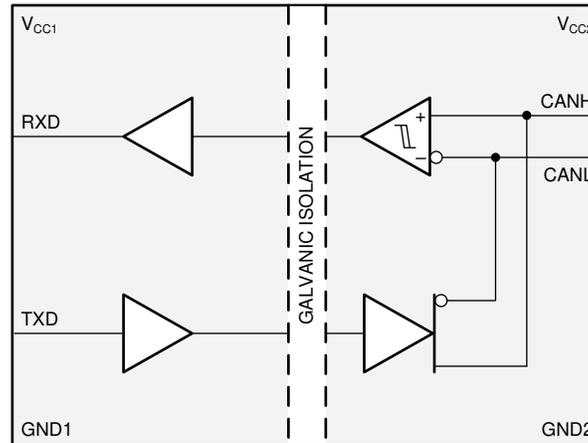


Figure 1-1. Functional Block Diagram

ISO1042-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 8-DWV (wide-body SOIC) Package

This section provides Functional Safety Failure In Time (FIT) rates for 8-DWV package of ISO1042-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total Component FIT Rate	18
Die FIT Rate	3
Package FIT Rate	15

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 200 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55 °C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 16-DW (wide-body SOIC) Package

This section provides Functional Safety Failure In Time (FIT) rates for the 16-DW package of ISO1042-Q1 based on two different industry-wide used reliability standards:

- [Table 2-3](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-4](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total Component FIT Rate	28
Die FIT Rate	3
Package FIT Rate	25

The failure rate and mission profile information in [Table 2-3](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 200 mW
- Climate type: World-wide Table 8
- Package factor (λ_3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55 °C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-4](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ISO1042-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
CAN bus output not in voltage or timing specification	32%
CAN bus output goes recessive	19%
CAN bus output stuck dominant	12%
CAN bus output undetermined	5%
CAN bus output Hi Z	2%
RXD output not in voltage or timing specification	12%
RXD output undetermined	8%
RXD output stuck high	8%
RXD output stuck low	2%

The FMD in [Table 3-1](#) excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ISo1042-Q1 (8-DWV and 16-DW package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#) and [Table 4-6](#).)
- Pin open-circuited (see [Table 4-3](#) and [Table 4-7](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#) and [Table 4-8](#))
- Pin short-circuited to supply (see [Table 4-5](#) and [Table 4-9](#))

[Table 4-2](#) through [Table 4-9](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#). Note that when pin short to ground case is discussed, only same side ground shorts are considered.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 8-DWV Package

[Figure 4-1](#) shows the ISO1042-Q1 pin diagram for the 8-DWV package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ISO1042-Q1 data sheet.

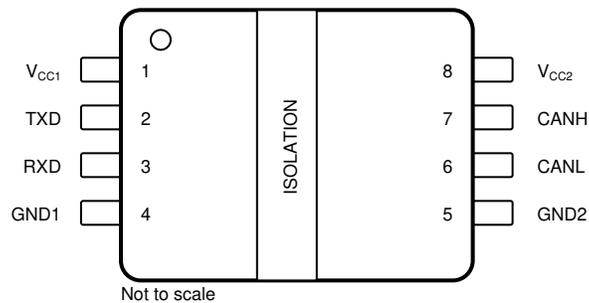


Figure 4-1. Pin Diagram (8-DWV) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V _{CC1}	1	No power to the device on side-1. Observe that the absolute maximum rating for TXD pin is met; otherwise device damage may be plausible.	A
TXD	2	TXD stuck logic low i.e. tries to put CAN bus to dominant state permanently, but after DTO, CAN bus goes recessive. Communication corrupted for DTO time.	B
RXD	3	RXD output stuck low. So not able to replicate CAN bus information. If CAN bus remains recessive for extended duration, RXD stuck low creates a short between supply and ground, causing possible device damage.	A
GND1	4	Device continues to function as expected. Normal operation.	D
GND2	5	Device continues to function as expected. Normal operation.	D
CANL	6	CANL stuck low. No proper recessive voltage, communication between nodes in CAN network corrupted.	B
CANH	7	CANH stuck low. Differential Vod (CANH-CANL) is negative, causing communication corruption.	B
V _{CC2}	8	No power to the device on side-2. CANH/CANL high impedance, communication lost. RXD=default high.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V _{CC1}	1	Operation undetermined. Either device is unpowered and RXD state undetermined, CAN bus recessive or through internal ESD diode on TXD pin, device can power up if TXD is driven to logic high. If TXD has current sourcing capability to provide regular operating current of device, ESD diode conducts that current and device damage plausible.	A
TXD	2	No data transmission possible on CAN bus. RXD replicates CAN bus traffic.	B
RXD	3	No CAN bus traffic reception possible.	B
GND1	4	Device unpowered on side1. RXD state undetermined, CAN bus recessive.	B
GND2	5	Device unpowered on side-2. RXD default high state, CAN bus high impedance.	B
CANL	6	State of CANL undetermined. Data communication to and from CAN bus lost.	B
CANH	7	State of CANH undetermined. Data communication to and from CAN bus lost.	B
V _{CC2}	8	Device unpowered on side-2, RXD default high, CAN bus high impedance.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
V _{CC1}	1	TXD	TXD input stuck high. CAN bus stuck recessive. Communication from node to CAN bus corrupted.	B
TXD	2	RXD	If TXD is low continuously, CAN bus stays dominant till Dominant timeout, then CAN bus goes recessive, so RXD goes high. RXD driven high internally being shorted to TXD low can create high current between supply and ground and cause possible device damage.	A
RXD	3	GND1	RXD receive data shorted to ground. CAN bus staying recessive for extended duration can cause RXD to be driven high internally and create short between supply and ground, causing possible device damage.	A
GND1	4	RXD	Already considered in above row.	A
GND2	5	CANL	CANL stuck low. No proper recessive voltage, communication between nodes in CAN network corrupted.	B
CANL	6	CANH	Communication corrupted as differential output always zero either for TXD high or low.	B
CANH	7	V _{CC2}	CANH stuck high, so always differential voltage on CAN bus even in recessive state. Communication corrupted.	B
V _{CC2}	8	CANH	Already considered in above row.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V _{CC1}	1	No effect. Normal operation.	D
TXD	2	TXD input stuck high. CAN bus stuck recessive. Communication from node to CAN bus corrupted.	B
RXD	3	RXD receive data stuck high. If CAN bus is dominant for extended duration, RXD driven internally low can create short between supply and ground, causing possible device damage.	A
GND1	4	Device side-1 unpowered. Observe that the absolute maximum ratings for TXD pins of the device are met, otherwise device damage may be plausible.	A
GND2	5	Device side-2 unpowered. CAN bus high impedance. RXD default high.	B
CANL	6	CANL stuck high, so differential output is always negative. Communication corrupted.	B
CANH	7	CANH stuck high, so always differential voltage on CAN bus even in recessive state. Communication corrupted.	B
V _{CC2}	8	No effect. Normal operation.	D

4.2 16-DW Package

Figure 4-2 shows the ISO1042-Q1 pin diagram for the 16-DW package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ISO1042-Q1 data sheet.

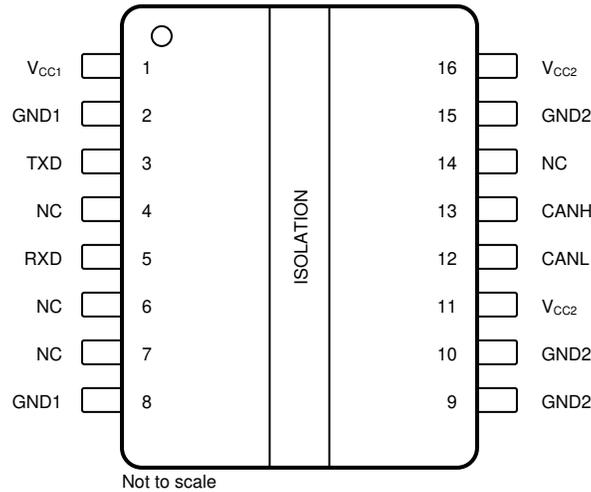


Figure 4-2. Pin Diagram (16-DW Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V _{CC1}	1	No power to the device on side-1. Observe that the absolute maximum rating for TXD pin is met; otherwise device damage may be plausible.	A
GND1	2	Device continues to function as expected. Normal operation.	D
TXD	3	TXD stuck logic low i.e. tries to put CAN bus to dominant state permanently, but after DTO, CAN bus goes recessive. Communication corrupted for DTO time.	B
NC	4	Device continues to function as expected. Normal operation.	D
RXD	5	RXD output stuck low. So not able to replicate CAN bus information. If CAN bus remains recessive for extended duration, RXD stuck low creates a short between supply and ground, causing possible device damage.	A
NC	6	Device continues to function as expected. Normal operation.	D
NC	7	Device continues to function as expected. Normal operation.	D
GND1	8	Device continues to function as expected. Normal operation.	D
GND2	9	Device continues to function as expected. Normal operation.	D
GND2	10	Device continues to function as expected. Normal operation.	D
V _{CC2}	11	No power to the device on side-2. CANH/CANL high impedance, communication lost. RXD=default high.	B
CANL	12	CANL stuck low. No proper recessive voltage, communication between nodes in CAN network corrupted.	B
CANH	13	CANH stuck low. Differential Vod (CANH-CANL) is negative, causing communication corruption.	B
NC	14	Device continues to function as expected. Normal operation.	D
GND2	15	Device continues to function as expected. Normal operation.	D
V _{CC2}	16	No power to the device on side-2. CANH/CANL high impedance, communication lost. RXD=default high.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V _{CC1}	1	Operation undetermined. Either device is unpowered and RXD state undetermined, CAN bus recessive or through internal ESD diode on TXD pin, device can power up if TXD is driven to logic high. If TXD has current sourcing capability to provide regular operating current of device, ESD diode conducts that current and device damage plausible.	A
GND1	2	Device gets return ground through pin8. Normal operation.	D
TXD	3	No data transmission possible on CAN bus. RXD replicates CAN bus traffic.	B
NC	4	Device continues to function as expected. Normal operation.	D
RXD	5	No CAN bus traffic reception possible.	B
NC	6	Device continues to function as expected. Normal operation.	D
NC	7	Device continues to function as expected. Normal operation.	D
GND1	8	Device gets return ground through pin2. Normal operation.	D
GND2	9	Device gets return ground through pin10/15. EMC performance may be affected.	C
GND2	10	Device gets return ground through pin9/15. EMC performance may be affected.	C
V _{CC2}	11	No power to the device on side-2. CANH/CANL high impedance, communication lost. RXD=default high.	B
CANL	12	CANL state undetermined. Communication corrupted to and from the CAN bus.	B
CANH	13	CANH state undetermined. Communication corrupted to and from the CAN bus.	B
NC	14	Device continues to function as expected. Normal operation.	D
GND2	15	Device gets return ground through pin9/10. EMC performance may be affected.	C
V _{CC2}	16	No power to the device on side-2. CANH/CANL high impedance, communication lost. RXD=default high.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
V _{CC1}	1	GND1	No power to the device on side-1. Observe that the absolute maximum rating for TXD pin is met; otherwise device damage may be plausible.	A
GND1	2	TXD	TXD stuck logic low i.e. tries to put CAN bus to dominant state permanently, but after DTO, CAN bus goes recessive. Communication corrupted for DTO time.	B
TXD	3	NC	Device continues to function as expected. Normal operation.	D
NC	4	RXD	Device continues to function as expected. Normal operation.	D
RXD	5	NC	Device continues to function as expected. Normal operation.	D
NC	6	NC	Device continues to function as expected. Normal operation.	D
NC	7	GND1	Device continues to function as expected. Normal operation.	D
GND1	8	NC	Already considered above.	D
GND2	9	GND2	Device continues to function as expected. Normal operation	D
GND2	10	V _{CC2}	No power to the device on side-2. CANH/CANL high impedance, communication lost. RXD=default high.	B
V _{CC2}	11	CANL	CANL stuck high, so differential output is always negative. Communication corrupted.	B
CANL	12	CANH	Communication corrupted as differential output always zero either for TXD high or low.	B
CANH	13	NC	Device continues to function as expected. Normal operation.	D
NC	14	GND2	Device continues to function as expected. Normal operation.	D
GND2	15	V _{CC2}	No power to the device on side-2. CANH/CANL high impedance, communication lost. RXD=default high.	B
V _{CC2}	16	GND2	Already considered above.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V _{CC1}	1	Device continues to function as expected. Normal operation.	D
GND1	2	This can create potential difference between pin2 and pin8, causing high current to flow in device and potential device damage.	A
TXD	3	TXD stuck high, CAN bus recessive. Communication from device to CAN bus lost. RXD can still monitor CAN bus traffic.	B
NC	4	Device continues to function as expected. Normal operation.	D
RXD	5	RXD stuck high, so CAN bus traffic reception corrupted.	B
NC	6	Device continues to function as expected. Normal operation.	D
NC	7	Device continues to function as expected. Normal operation.	D
GND1	8	This can create potential difference between pin2 and pin8, causing high current to flow in device and potential device damage.	A
GND2	9	This can create potential difference between pin9 and pin10/15, causing high current to flow in device and potential device damage.	A
GND2	10	This can create potential difference between pin10 and pin9/15, causing high current to flow in device and potential device damage.	A
V _{CC2}	11	Device continues to function as expected. Normal operation.	D
CANL	12	CANL stuck high, so differential output is always negative. Communication corrupted.	B
CANH	13	CANH stuck high, so always differential voltage on CAN bus even in recessive state. Communication corrupted.	B
NC	14	Device continues to function as expected. Normal operation.	D
GND2	15	This can create potential difference between pin15 and pin10/9, causing high current to flow in device and potential device damage.	A
V _{CC2}	16	Device continues to function as expected. Normal operation.	D

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated