Application Report

TLIN1028xS-Q1 Functional Safety FIT, Failure Mode Distribution and Pin FMA

Richard Hubbard

ABSTRACT

This document contains information for TLIN10283S-Q1 and TLIN10285S-Q1 which are local interconnect network (LIN) transcievers with integrated LDO (8-pin SOIC package) to aid in a functional safety system design.

Available information:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

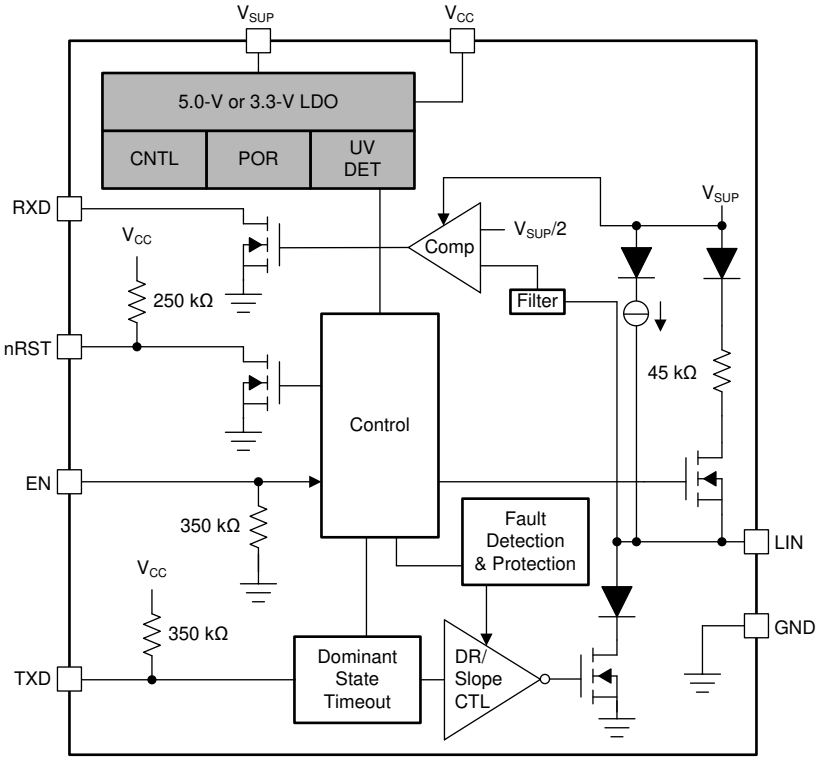

Figure 1-1. Functional Block Diagram

TLIN10283S-Q1 and TLIN10285S-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

1 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TLIN10283S-Q1 and TLIN10285S-Q1 based on two different industry-wide used reliability standards:

- Table 1-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 1-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours), Full Load	FIT (Failures Per 10^9 Hours), 80% Load
Total Component FIT Rate	24	19
Die FIT Rate	15	11
Package FIT Rate	9	8

The failure rate and mission profile information in Table 1-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation, full load: 500 mW
- Power dissipation, 80% load: 400 mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- Electrical overstress (EOS) FIT rate assumed: 0 FIT

Table 1-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog /mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 1-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLIN10283S-Q1 and TLIN10285S-Q1 in Table 2-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 2-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Transmitter fail	45%
Receiver fail	5%
LDO fail	20%
Logic or IO cell fail	10%
Global power or state control fail	20%

3 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLIN10283S-Q1 and TLIN10285S-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 3-2)
- Pin open-circuited (see Table 3-3)
- Pin short-circuited to an adjacent pin (see Table 3-4)
- Pin short-circuited to V_{SUP} (see Table 3-5)
- Pin short-circuited to V_{CC} (see Table 3-6)

Table 3-2 through Table 3-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 3-1.

Table 3-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 3-1 shows the TLIN10283S-Q1 and TLIN10285S-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TLIN10283S-Q1 and TLIN10285S-Q1 datasheet.

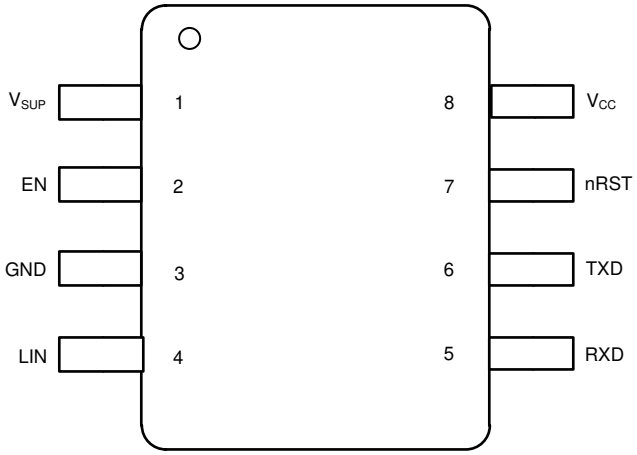

Figure 3-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the Pin FMA in this section:

- All conditions within recommended operating conditions.
- V_{CC} = 4.9 to 5.1 V for TLIN10285S-Q1
- V_{CC} = 3.23 to 3.37 V for TLIN10283S-Q1
- V_{SUP} = see recommended operating conditions in device data sheet

Table 3-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{SUP}	1	Device is unpowered and will not function	A
EN	2	Device may only operate in Standby mode after power-on. If the short occurs in Normal mode, the part would then be forced to enter SLP (TXD=dominant) or STBY (TXD=recessive) based on the state of TXD when the shorting occurred. The short to GND condition would disable LIN communication.	B
GND	3	None	D
LIN	4	LIN bus biased dominant, no LIN communication possible	B
RXD	5	RXD biased dominant, no communication from LIN bus to MCU possible	B
TXD	6	TXD biased dominant, no communication from MCU to LIN possible	B
nRST	7	nRST biased low causing the MCU to be in reset if connected in this manner	B
V_{CC}	8	Excessive current draw from V_{CC}. Thermal shut down will happen quickly.	A

Table 3-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Excess	Failure Effect Class
V_{SUP}	1	Device is unpowered and will not function	B
EN	2	Biased low due to internal pull-down so device in standby mode	B
GND	3	Device is unpowered and will not function	B
LIN	4	No LIN communication possible	B
RXD	5	No communication from LIN bus to MCU possible	B
TXD	6	No communication from MCU to LIN bus possible	B
nRST	7	No nRST output to MCU indicating a UV_{CC} event	C
V_{CC}	8	LDO unable to power external circuits	C

Table 3-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
V_{SUP}	1	EN	EN pin absolute max will be exceeded	A
EN	2	GND	EN biased to ground. See EN shorted to GND	B
GND	3	LIN	LIN biased dominant. See LIN shorted to GND	B
RXD	5	TXD	Communication between MCU and LIN bus disrupted	B
TXD	6	nRST	TXD biased recessive unless UV_{CC} event and then biased dominant, MCU to LIN bus communication not possiblen	B
nRST	7	V_{CC}	nRST internally connected to V_{CC} but a UV_{CC} event may not be provided to MCU in timely manner	C

Table 3-5. Pin FMA for Device Pins Short-Circuited to V_{SUP}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	2	Absolute max voltage exceeded	A
GND	3	Device will not function	A
LIN	4	Device biased recessive, no bus communication possible	B
RXD	5	Absolute max voltage exceeded	A
TXD	6	Absolute max voltage exceeded	A
nRST	7	Absolute max voltage exceeded	A
V_{CC}	8	Absolute max voltage exceeded	A

Table 3-6. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{SUP}	1	Absolute max voltage exceeded on V_{CC}	A
EN	2	EN biased high, mode change may not be possible	B
GND	3	Device will not function	A
LIN	4	Absolute max voltage exceeded on V_{CC}, no bus communication	A
RXD	5	RXD biased recessive, no communication from LIN bus to MCU	B
TXD	6	TXD biased recessive, no communication from MCU to LIN bus	B
nRST	7	None - internally biased to V_{CC}	D

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2020) to Revision A (October 2020)	Page
• Changes throughout the document	0

Trademarks

All other trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265