Application Report
SLLA447–March 2019

TUSB8044A schematic checklist

ABSTRACT

This schematic checklist provides a brief explanation of each TUSB8044A device pin and the recommended configuration of TUSB8044A device pins for default operation. TUSB8044A is a USB 3.1 Gen1 hub controller that provides one upstream port and four downstream ports and is compliant with the Universal Serial Bus (USB) specification. TUSB8044A is implemented with a digital state machine requiring no firmware programming however, this device has the ability to also be configured via pin strap, I2C, and SMBus communication. Use this information to check the connectivity for each TUSB8044A device on a system schematic.

This document is intended to aid design at the system level for general applications but should not be the only resource used. In addition to this list, use the information in the *TUSB8044A four-port USB 3.2x1 Gen1 hub with USB billboard data sheet*, *TUSB8044AEVM user's guide*, and associated documents to gain a full understanding of device functionality.

NOTE: TUSB8044A has many configurations; this schematic checklist covers a TUSB8044A USB Hub that is configured without external EEPROM with downstream power switching and overcurrent reporting.

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Trademarks

1 TUSB8044A Schematic Checklist

Pin Name	Pin Number(s)	Pin Description	Recommendation	Addtional Pin Considerations
Power Pins				
VDD33	16, 34, 52, 63	3.3 V Positive Power Supply	Place 0.1 uF decoupling capacitors on near each VDD33 pin to GND. Use one 10 uF bulk capacitor from VDD33 to GND.	VDD33 and VDD should have a ramp time of 0.2 ms to 100 ms. VDD33 and VDD have ramp order only when using a passive reset.
VDD	5, 8, 13, 21, 28, 31, 51, 57	1.1 V Positive Power Supply	Place 0.1 uF decoupling capacitors on near each VDD33 pin to GND. Use one 10 uF bulk capacitor from VDD33 to GND.	
GND	PAD	Ground	Connected to PCB Ground.	Ensure thermal pad has ample solder for stable connection to ground. Improper grounding can lead to functional issues in system.

I2C/SMBUS Pins				
SCL / SMBCLK	38	EEPROM Serial Clock	Leave unconnected.	The external interface is enabled when both the SCL/SMBCLK and SDA/SMBDAT terminals are pulled up to 3.3 V at the deassertion of reset. When used, EEPROM overwrites all the pin configurations. If EEPROM/I2C is used, connect a 2-kΩ pullup resistor to VDD33 and to SCL pin of external EEPROM.
SDA / SMBAT	37	EEPROM Serial Data.	Leave unconnected.	
Configuration and Miscellaneous Pins				
SMBUSz / SS_SUSPEND	39	I2C or SMBUS mode. Select Pin/SuperSpeed USB Suspend Status Indicator	Connect a 4.7-kΩ pullup resistor to VDD33 or leave NC to use internal pullup resistor for I^2C mode. Leaving SCL and SDA unconnected allows the device to use default configuration.	This setting is configured during the de-assertion of reset. After reset is de-asserted this pin indicatesSuperSpeed USB Suspend Status (Output active when enabled via device registers). Do not tie pin directly to supply but instead pull up or pull down using external resistor. Values read from EERPROM override pin values seen during reset.
PWRCTL_POL	41	Power control polarity. Controls behavior of PWRCTL pins.	Connect a 4.7-kΩ pull-down resistor to GND or leave NC to use internal pullup resistor. This indicates active high polarity for the PWRCTL pins on the downstream ports.	-
GANGED / SMBA2 / HS_UP	42	Ganged Operation Enable / SMBus address bit 2 / Upstream Port High-Speed Status Indicator	Connect a 4.7-kΩ pulldown resistor to GND or leave NC to use internal pulldown resistor indicating individual power control supported when power switching is enabled. Do not tie directly to supply, but instead pull up or pull down using external resistor or leave NC.	This setting is configured during the de-assertion of reset. After reset is de-asserted this pin indicates high-speed USB connection status of the upstream port (Output active when enabled via device registers). Values read from EERPROM override pin values seen during reset. If SMBUSz = 0, SMBUS slave address is '1000 10yz' in combination with the y equal to the FullPWRMGMTz / SMBA1 pin and z equal to the read/write bit, when GRSTz is deasserted.
FullPWRMGMTz / SMBA1/ SS_UP	40	Full Power Management Enable / SMBus Address bit 1.	Connect a 4.7-kΩ pulldown resistor to GND or leave NC to use internal pulldown resistor indicating power switching is supported by downstream ports. Do not tie directly to supply, but instead pull up or pull down using external resistor.	This setting is configured during the de-assertion of reset. After reset is de-asserted this pin indicates SuperSpeed USB connection status of the upstream port (Output active when enabled via device registers). Values read from EERPROM override pin values seen during reset. If SMBUSz = 0, SMBUS slave address is '1000 1x0z' in combination with the x equal to the GANGED / SMBA2 / HS_UP pin and z equal to the read/write bit, when GRSTz is deasserted.
AUTOENz / HS_SUSPEND	45	Automatic Charge Mode Enable / HS Suspend Status.	Connect a 4.7-kΩ pulldown resistor to GND or leave NC to use internal pulldown resistor indicating Automatic Mode is enabled on ports that are enabled for battery charging when the hub is unconnected. Do not tie directly to supply, but instead pull up or pull down using external resistor.	For more information on Automatic Mode, see the Battery Charging Features section in the *TUSB8044A four-port USB 3.2x1 Gen1 hub with USB billboard data sheet*. This setting is configured during the de-assertion of reset. After reset is de-asserted this pin indicates the high speed suspend state of the device (Output active when enabled via device registers).
XI	62	Crystal Clock Input.	Connect 24-MHz crystal input. When using a crystal a 1-MΩ feedback resistor is required between XI and XO. This pin can also be driven by an external oscillator.	See the USB2.0 Billboard, One Time Programmable (OTP) Configuration, and Clock Generation sections from the *TUSB8044A four-port USB 3.2x1 Gen1 hub with USB billboard data sheet* for more information.
XO	61	Crystal Clock Output	Connect 24-MHz crystal output. When using a crystal a 1-MΩ feedback resistor is required between XI and XO. If XI is driven by an external oscillator, this pin can be left unconnected.	
GRSTz	50	Device Active Low Reset.	For passive reset, connect 1 uF capacitor. VDD must be stable before VDD33. For active reset, VDD33 must be stable before the VDD11 supply and meet the 3 ms power-up delay (see t_{d2} spec from the Timing Requirements section in the *TUSB8044A four-port USB 3.2x1 Gen1 hub with USB billboard data sheet*. Both power supplies must be stable when GRSTzis de-asserted.	See the Timing Requirements and Crystal Requirements sections in the *TUSB8044A four-port USB 3.2x1 Gen1 hub with USB billboard data sheet* for more information on reset.
TEST	49	TEST mode enable.	Connect a 4.7-kΩ pulldown resistor to GND.	-
NC	60	No Connect.	Leave Floating.	-
Upstream Facing Port				
USB_SSTXP_UP	55	USB 3.1 Gen 1 (SuperSpeed) transmitter differential pair (positive).	Connect 0.1 uF AC coupling capacitor to USB Host SSRXp/n or USB Connector SSTXp/n.	-
USB_SSTXM_UP	56	USB 3.1 Gen 1 (SuperSpeed) transmitter differential pair (negative)	Connect 0.1 uF AC coupling capacitor to USB Host SSRXp/n or USB Connector SSTXp/n.	-

USB_SSRXP_UP	58	USB 3.1 Gen 1 (SuperSpeed) receiver differential pair (positive)	No AC coupling capacitor required, connect to USB Host SSTXp/n or USB Connector SSRXp/n.	-
USB_SSRXM_UP	59	USB 3.1 Gen 1 (SuperSpeed) receiver differential pair (negative)	No AC coupling capacitor required, connect to USB Host SSTXp/n or USB Connector SSRXp/n.	-
USB_DP_UP	53	Upstream Differential Pair for USB 2.0 (High Speed) Communication.	Connect DM0 and DP0 to USB host or upstream facing USB Connector D- and D+, respectively.	-
USB_DM_UP	54			-
USB_R1	64	Precision resistor reference.	Connect 9.53-kΩ ±1% resistor between USB_R1 and GND.	See the *TI USB hubs: adjusting USB_R1 application report* for more information.
USB_VBUS	48	USB upstream port power monitor, Vbus Detection.	Connect resistor divider using a 90.9-kΩ ±1% pullup resistor to Vbus and a 10-kΩ ±1% pulldown resistor to GND.	Resistor divider values can change with Vbus to keep voltage seen by USB_VBUS inside 0 V to 1.155 V range. See the Recommended Operating Conditions section in the *TUSB8044A four-port USB 3.2x1 Gen1 hub with USB billboard data sheet*.
Downstream Facing Port [4:1]				
USB_SSTXP_DN[4:1]	3, 11, 19, 26	USB 3.1 Gen 1 (SuperSpeed) transmitter differential pair.	Connect 0.1 uF AC coupling capacitor to USB Device / Hub SSRXp/n or USB Connector SSTXp/n.	If downstream port is unused, leave unconnected. No additional termination needed.
USB_SSTXM_DN[4:1]	4, 12, 20, 27		Connect 0.1 uF AC coupling capacitor to USB Device / Hub SSRXp/n or USB Connector SSTXp/n.	If downstream port is unused, leave unconnected. No additional termination needed.
USB_SSRXP_DN[4:1]	6,14, 22, 29	USB 3.1 Gen 1 (SuperSpeed) receiver differential pair.	No AC coupling capacitor, connect to USB Device / Hub SSTXp/n or USB Connector SSRXp/n.	If downstream port is unused, leave unconnected. No additional termination needed.
USB_SSRXM_DN[4:1]	7, 15, 230		No AC coupling capacitor, connect to USB Device / Hub SSTXp/n or USB Connector SSRXp/n.	If downstream port is unused, leave unconnected. No additional termination needed.
USB_DP_DN[4:1]	1, 9, 17, 24	USB 2.0 (High Speed) Downstream Differential Pair	Connect DM[4:1] and DP[4:1] to D- and D+, respectively, to downstream facing USB connector.	If downstream port is unused, leave unconnected. No additional termination needed.
USB_DM_DN[4:1]	2, 10, 18, 25			If downstream port is unused, leave unconnected. No additional termination needed.
OVRCUR[4:1]z	44, 46, 47, 43	Indicates overcurrent event on downstream Port [4:1].	Connect to overcurrent indicator on power switch for downstream port [4:1] to allow overcurrent reporting to USB host.	If downstream port is unused, pull pin high with 4.7-kΩ pull up resistor to VD33. Overcurrent reporting required for USB-IF Compliance.
PWRCTL[4:1] /BATEN[4:1]	33, 35, 36, 32	Port 1 power control signals.	Connect to power switch EN pin to allow USB host control of downstream port power and protection in overcurrent event.	If downstream port is unused, leave unconnected.
Notes: Routing through ESD or common mode choke before receptacle is allowed and recommended. ESD protection should be placed as close as possible to the USB connectors. Common mode chokes should be placed between the USB hub and the ESD protection. Verify the pinout of the USB connectors. Verify pin-out of TUSB8044A matches the *TUSB8044A four-port USB 3.2x1 Gen1 hub with USB billboard data sheet*. Always refer to the *TUSB8044A four-port USB 3.2x1 Gen1 hub with USB billboard data sheet* for complete descriptions of each pin. For USB compliant applications overcurrent events on downstream ports must be reported to the USB host.				

2 References

- Texas Instruments, *TUSB8044A four-port USB 3.2x1 Gen1 hub with USB billboard data sheet*
- Texas Instruments, *TUSB8044AEVM user's guide*
- Texas Instruments, *TI USB hubs: adjusting USB_R1 application report*
- Texas Instruments, *Transition from USB 3.1 hub to USB 3.2 hub application report*

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