ENABLE Function with Unused Differential Input

Today, designers want to get the most out their gate drive designs and require more control out of their basic gate drivers. When selecting a gate driver, engineers can choose from a variety of pinouts and features. Simple single-channel gate drivers typically have between five to eight pins: supply, ground, differential inputs and differential outputs.

Gate drivers with dual-input configurations give the user flexibility to drive the device using either a noninverting input pin (IN+) or an inverting input pin (IN-) to control the state of the output. Use Table 1 as a reference to determine the state of the output when a bias is applied to the IN+ and IN- pins.

This TI TechNote demonstrates how to use an unused differential input as an ENABLE/DISABLE when the gate driver does not have a dedicated ENABLE pin. This technique allows the designer to use the same gate driver with different control or ENABLE requirements.

Table 1. Function Table for UCC53x0S

IN+	IN-	OUTH	OUTL
Low	X	High-Z	Low
X	High	High-Z	Low
High	Low	High	High-Z

There are three common input drive configurations for devices with IN+ and IN- pins:

1. Separate PWM signals to IN+ and IN- (differential drive)
2. Drive IN+ and short IN- to GND
3. Drive IN- and short IN+ to VCC1

For many applications, it is critical to ensure the gate driver does not pass a signal through and turn on the MOSFET or IGBT.

Some gate drivers include a dedicated ENABLE or DISABLE pin to accept or ignore the PWM input. But for differential input gate drivers, there is another option: either input may be repurposed as an ENABLE/DISABLE pin. An example of a gate driver with differential inputs is shown in Figure 1.

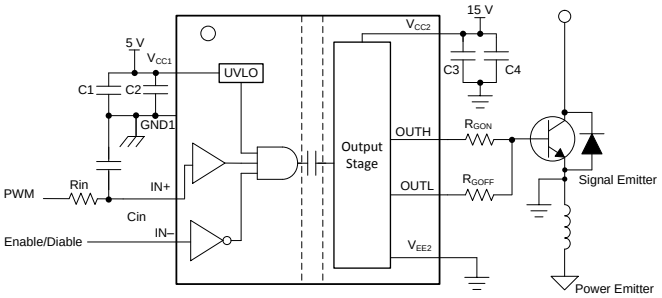

Figure 1. Gate Driver with Differential Inputs

How is this done? The ENABLE and DISABLE function is implemented with the IN+ or IN- input and takes advantage of the logical conjunction operation of the internal AND gate. The truth table of the AND gate tells us the logical AND operation of the three input signals (IN+, IN-, and UVLO) is true if and only if all of the signals are true (high). The input stage of UCC53x0 family is visualized in Figure 2.

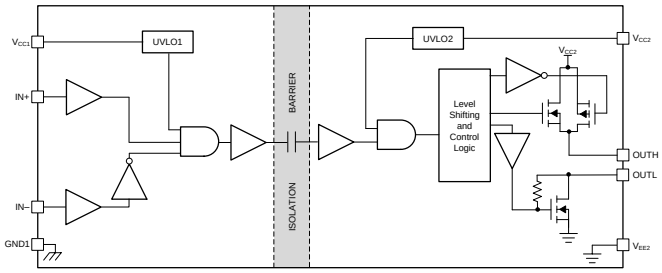

Figure 2. Gate Driver Function Block Diagram

In order for a high signal to pass, V_{CC1} has to be greater than the UVLO threshold, IN+ must be high, and IN- must be low due to the inverter connected to its input.

In contrast, if any of the three inputs to the AND gate are low then the output will also be low (a high signal at IN- passes through the inverter and flips to a low signal at the input of the AND gate).

The IN+ and IN- inputs offer non-inverting (Figure 1) and inverting (Figure 3) configurations and these figures show how to implement the ENABLE/DISABLE function. For a non-inverting configuration, the PWM input is tied to the IN+ pin and the IN- pin can be used to implement the DISABLE function using an external logic signal. OUT is disabled when IN- is biased high and OUT is enabled when IN- is biased low as shown in Figure 1.

The inverting configuration in Figure 3, applies the PWM input to the inverting pin IN-, and the IN+ pin can be used to implement the ENABLE function using an external logic signal. OUT is disabled when IN+ is biased low and OUT is enabled when IN+ is biased high.

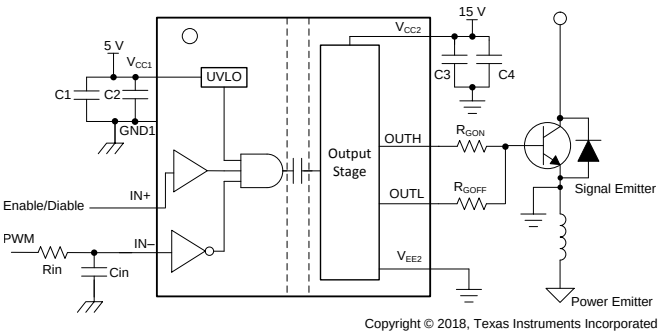

Figure 3. Inverting Configuration

Another method of repurposing an unused input as an ENABLE in shown in Figure 4. This ENABLE implementation can be used for applications with only one available PWM signal. The same PWM signal that drives IN+, drives IN- low through a discrete n-channel MOSFET and enables the output.

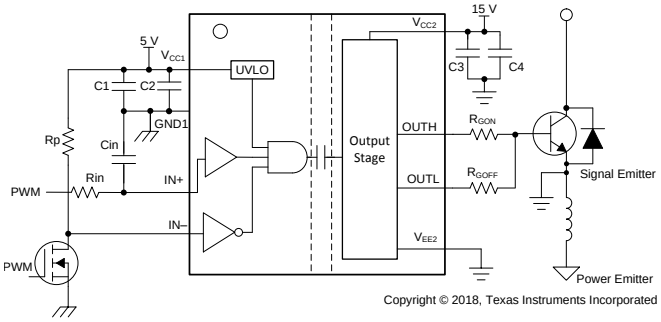

Figure 4. ENABLE Implementation Using a Discrete NMOS Transistor

The logic table for this configuration is shown in Table 2.

Table 2. Logic Table for Discrete NMOS ENABLE Implementation

PWM State	IN+	IN-	OUT
LOW	LOW	HIGH	LOW
HIGH	HIGH	LOW	HIGH

In summary, the output pin is driven into a high state only when IN+ pin is biased high and IN- is biased low. Table 1 uses the truth table found in the UCC53x0S datasheet as an example.

When configuring the unused IN+ or IN- input as an ENABLE or DISABLE pin, it is important to look at the input structure and determine if it is TTL or CMOS based. ENABLE pins typically are TTL based and have defined voltage levels and hysteresis. However, if the ENABLE pin function is used on CMOS inputs, the ENABLE/DISABLE feature will be dependent on some percentage of the supply voltage. It is possible to have both TTL and CMOS compatibility, as long as the supply voltage supports the required thresholds.

For example, the UCC2751x gate driver with TTL/CMOS compatible input-threshold logic is independent of the supply voltage. The typical high threshold will be approximately 2-V and the low threshold will be approximately 1-V. Digital power controllers can use 3.3-V or 5-V PWM signals to drive these logic level thresholds.

Devices with an ENABLE pin can have an ENABLE to output propagation delay different from the input to output propagation delay. For differential input gate drivers, the ENABLE/DISABLE delay will be the same as the input to output propagation delay of IN+ or IN-.

Table 3. Alternative Device Recommendations

Device	Optimized Parameters	Performance Trade-Off
UCC5310MC	Single Channel Isolated Gate Driver	Less Sink Current
UCC27517	Single Channel High Speed Low Side Driver	No Isolation
LM5114	Single Channel 7.6A Peak Current Low Side Driver	No Isolation

Table 4. Adjacent Tech Notes

Document Title	Literature Number
External Resistor Selection Guide	slla385
Understanding Peak IOH and IOL Currents	slla387
Low-Side Gate Drivers with UVLO vs BJT Totem-Pole	slua877

1 Related Documentation

1. UCC53x0 Datasheet
2. UCC2751x Datasheet
3. LM5114 Datasheet

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