Application Report
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# 10GBASE-KR link optimization with TLK10034 and TLK10232

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**ABSTRACT**

This application report highlights the 10 Gigabit Ethernet KR features of TI's TLK10034 and TLK10232 transceivers. The report provides information on 10GBASE-KR in general, important registers of the TLK devices, how to set up a BER test, how to optimize a given 10GBASE-KR link, and how to interpret test data provided by the devices.

**Contents**



**List of Figures**



**List of Tables**



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# 1 About 10GBASE-KR, Auto Negotiation, and Link Training

10GBASE-KR is a high -speed standard specifically designed for backplane Ethernet applications. The key features of this standard are the functions Auto Negotiation and Link Training, which are further explained in this section.

## 1.1 What Happens When Auto Negotiation is Active?

The transmitter of each device communicates to the other's receiver which modes of transmission they are able to handle. For the TLK10034 and the TLK10232, there are two available modes: 1G-KX and 10G-KR. The fastest both have in common is chosen as standard of operation. Auto Negotiation can only be used if implemented and activated in both communicating devices. For 10GBASE-KR operation using this feature is optional, but recommended.

Auto negotiation is enabled for the TLK10034 and TLK10232 by setting bit 12 in register AN_CONTROL (device address 0x07, address 0x0000). The default value of the register is 0x3000, which means that the device starts with auto negotiation active. If auto negotiation was first disabled and then enabled manually during a bring-up script, the procedure is initiated after a data path reset (set bit 3 under device address 0x1E, register 0x000E). It is recommended to disable auto negotiation for the start of the device's bring-up procedure and enable it again at the end. Another option is to use the restart function (set bit 9 in register 0x0000 to 1). Auto negotiation runs before link training is started; therefore, link training also has to be first disabled at the start of a bring- up procedure and afterwards it has to be enabled again.

## 1.2 What Happens When Link Training is Activated?

Through sending test sequences transmitter and receiver try to find the best configuration of the pre-cursor and post-cursor 1 parameters, which are explained in Section 4, for optimal channel matching. For each test, setting the BER will be determined and saved internally in the device. Measurement data is accessible after link training has successfully completed.

Link training for 10 GBASE-KR is enabled by default, when the device is powered up. To enable it manually, for example after a bring-up procedure, bit 1 in the PMA layer (device address 0x01) in register LT_TRAIN_CONTROL (register address 0x96, default 0x0002) has to be set high. For link training to then become active, a data path reset is necessary, which is done by setting bit 3 under device address 0x1E in register 0x000E.

The actual link training BER results can be read from the PMA layer's register 0x9012 for the TLK10034 and 0x9022 for the TLK10232. Setting bit 12 under device address 0x01 in register 0x9001 initiates the read out starting with the minimum post-cursor de-emphasis level.

The read out data can be interpreted as follows:

Registers 0x9012 and 0x9022 are 16-bit registers, but only the lower byte is valid data. The most significant bit (MSB) of this byte represents the most negative pre-cursor value, the least significant bit (LSB) the one for 0%. The first read register is the most positive post-cursor 1 setting. With every read the post-cursor 1 parameter is decreased to the next lower value, ending with the most negative after 32 reads. The bit patterns and corresponding post-cursor 1 values can be looked up from Table 5.

**NOTE:** Both auto negotiation and link training are automatically initiated every time the device is powered up or reset, unless both functions are directly disabled by a bring-up script.

# 2 General Requirements for 10GBASE-KR Applications

10GBASE-KR applications require a reference clock of either 156.25 MHz or 312.5 MHz to support data rates of 10.3125 Gbps. The reference clock for the TLK SerDes has to be applied from an external source via the REFCLK0 or the REFCLK1 pins of the TLK10034 or TLK10232. When using a reference clock of 156.25 MHz , the phase locked loop (PLL) multipliers should be adjusted to 16.5x on the high-speed (HS) side and 10x on the low-speed (LS) side to support the required 10.3125-Gbps data rate for KR applications. When using a reference clock of 312.5 MHz, the PLL multipliers on both the HS and LS side of the TLK devices would be half the value, respectively 8.25x and 5x. In the data sheets for the TLK devices, tables are provided to guide choosing the right multiplier settings for the developer's application, based on reference clock and number of LS lanes.

Only after it is verified that the PLLs are locked to the reference clock, further tests should be performed. Checking the PLL locking status can be done by observing, if bits 1 (LS PLL) and 0 (HS PLL) in register Channel_Status_1 (device address 0x1E, register 000F) are set. The PLLs are only able to lock, if the accuracy of the reference clock source is within ± 100 ppm of the specified frequency.

Additionally, the 10G BASE-KR standard requires the features auto negotiation and link training to be implemented in both the transmitting and the receiving devices. For non-KR applications there is an option in TLK10034 and TLK10232 to disable those features. More details on auto negotiation and link training regarding setup and beneficial adjustments for TI's TLK10034 and TLK10232 are discussed in the previous section and in Section 5, Section 6, and Section 7.

## 3 Setting up Tests and Measuring BER

Registers and bits mentioned in this section are the same for TLK10034 and TLK10232.

TI's TLK10034 and TLK10232 both come with a wide set of integrated test patterns. These include clock patterns at different frequencies (high, low and mixed), PRBS (Pseudorandom Binary Sequence) 2^7, PRBS 2^23, PRBS 2^31, CRPAT (Compliant Random Pattern), CJPAT (Continuous Jitter Pattern), and KR standard patterns (Square Wave or Pseudorandom). Various diagnostic tests can be performed by using these test patterns. It is possible to verify that the device is properly configured, perform BER testing on a given link and further they can help in link optimization of the 10-Gigabit Ethernet transceivers for a given transmission line.

There are two options to activate the test patterns available in the device:

- One option of the TLK devices is to use vendor-specific patterns. The vendor-specific patterns are located in the vendor space (device address 0x1E) and can be enabled under register LOOPBACK_TP_CONTROL (address 0x000B). Test pattern generation is activated by setting bit 13 for HS or bit 7 for LS, test pattern verification is enabled via bit 12 for HS or bit 6 for LS. The desired test pattern can be chosen by setting appropriate bits [10:8] for HS and [11] [5:4] for LS according to Table 1. Dependent on the used transmission mode, some patterns are disabled or only available on certain lanes of the device.

**Table 1. Bit Patterns for Different Test Patterns Available in the Vendor Space**

| Test Pattern | Bit Pattern |
|---|---|
| High Frequency | 000 |
| Low Frequency | 001 |
| Mixed Frequency | 010 |
| CRPAT long | 011 |
| CRPAT short | 100 |
| PRBS 2^7 | 101 |
| PRBS 2^23 | 110 |
| PRBS 2^31 | 111 |

- The second option for generating test patterns is used when testing KR based applications. The test patterns used for testing KR based applications are generated from the PCS layer of the TLK SerDes (device address 0x03) and have to be used according to IEEE802.3. They can be enabled in register PCS_TP_CONTROL (register 0x2A). Available test patterns are PRBS2^31, KR Pseudorandom and a square-wave test pattern. The corresponding bit patterns for their activation are displayed in Table 2.

**Table 2. Bit Patterns for Different Test Patterns From the PCS Layer**

| PCS Test Pattern | Enabling Bits |
|---|---|
| PRBS 2^31 | Generation: Bit 4 high, Verification: Bit 5 high |
| KR Pseudorandom | Generation: Bit 3 high, Verification: Bit 2 high, Bit 1 low |
| KR Square Wave | Generation: Bit 3 high, Verification: Bit 2 high, Bit 1 high |

## 3.1 High Speed (HS) Test

Before testing the whole transmission path, one test setup can be a simple loop back between the HS transmitter and the receiver with a test pattern to ensure proper configuration of the device. This can be done either with an integrated loopback feature (device internal) or by externally connecting transmitter and receiver pins. The other and more common used option is an analysis and evaluation of the end application's high-speed data channel. The corresponding error count register HS_ERROR_COUNTER (device address 0x1E, register 0x0010) gives information about the BER and indicates the quality of the transmission path. Adjustments can be made by changing different parameters on the transmitter or receiver side. For only testing the high-speed part of the channel, usually PRBS patterns are used to measure the BER. Due to PRBS test patterns not being valid data in 10GBASE-KR mode, which is expected by a KR-compliant device, a KR pseudorandom pattern should be used or SYNC_STATUS_CHECK_DISABLE bit (device address 0x1E, register 0x8021, bit 4) should be set to ensure valid verification of the test pattern. Valid KR data is framed using the 64b/66b encoding scheme, while PRBS is not. By disabling the sync status check feature in the SerDes, the TLK device will ignore the status bit check on the data and simply verify the PRBS pattern. This option should only be used when enabling the PRBS31 pattern generated from the PCS layer as previously described.

When running a BER test with PRBS2^7, PRBS2^23 or frequency test patterns not generated from the PCS layer, this has to be done with a different setup, a so called forced 10G-KR mode. This has to be done because in 10GBASE-KR mode requires the test patterns being generated from the PCS layer. Therefore to set the TLK device into the forced 10G-KR mode Auto-negotiation and Link Training have to be disabled, because they are specific 10G-KR features. For Auto-negotiation this can be done by setting bit 12 in register 0x07.0000 (AN_CONTROL) to zero. Link training is disabled by setting bit 14 in register 0x1E.0001 (CHANNEL_CONTROL_1) to zero.

## 3.2 Low Speed (LS) Test

Many different tests can be performed using the low speed XAUI side of the TLK SerDes. A loopback test can be performed from the LS transmitter to the LS receiver, by connecting the two and reading back the BER from register 0x0011 (LS_ERROR_COUNTER) at device address 0x1E. An additional test that can be performed is that the XAUI portion of the SerDes can be used to verify that the connections between the MAC/FPGA and the TLK PHY are working properly. This can be achieved by enabling the test pattern generators and verifiers in the TLK and MAC/FPGA and performing a BER test between the two. This option might not be available with the MAC/FPGA that is implemented in the design, so please check back with the MAC/FPGA vendor to verify this feature. When using the XAUI portion of the SerDes with the test patterns provided by the TLK10034/T LK10232, the test pattern will be applied to all four lanes.

If the HS side has been tested with the before mentioned method, the LS test verifies that the configuration of the SerDes device was done correctly. A full data path test can only be performed with a CRPAT test pattern applied to the XAUI side, because other test patterns like PRBS would not be properly decoded by the TLK10034/TLK10232. The test can include the usage of encoding/decoding as well as crosspoint switching (only available in TLK10232). The most important test that can be performed is sending a test pattern from the MAC/FPGA to the LS side of the TLK device, over the HS link and then from the LS side of the receiver back to the MAC/FPGA to verify the test pattern. For the end application, this test can be used to evaluate the configuration for all communicating devices of the link.

It is possible to detect errors individually for each low-speed lane in the LS_LNx_ERROR_COUNTER, where x can be 0 − 3 for the TLK10034 and the TLK10232 (device address 0x1E, registers 0x0011–0x0014). Important is that if encoding/decoding (8b/10b and 64b/66b) is used, this feature has to be activated on both transmitter and receiver side. For the test of XAUI applications on the LS side, usually CRPAT and CJPAT are the patterns of choice.

# 4 Important Parameters, Registers and Bits for Link Optimization

Registers and bits mentioned in this section are the same for TLK10034 and TLK10232.

As transmission channels are seldom ideal, the TLK10034 and TLK10232 both come with a set of integrated functions which can be used to match the transmitter and receiver to each other and to the transmission line. If the settings are adjusted manually, the parameters explained in this section are the ones which should be changed first for improving the performance of the data transmission. If link training is used some of those parameters will be adjusted by the device. But there are also different options of settings for link training, which are further discussed in Section 5.

## *4.1 Transmitter Side*

### 4.1.1 SWING – Register HS_SERDES_CONTROL_2, Device Address 0x1E, Address 0x0003, Bits 15:12

The swing parameter sets the amplitude of the transmitter signal. The according bit patterns can be achieved from Table 3 of this application note or the data sheet. In general, it can be assumed that with higher frequencies and longer transmission lines, it is necessary to increase the amplitude of the data signal.

**Table 3. SWING Bit Patterns and Corresponding Amplitude Values in mVpp, Device Address 0x1E, Register 0x0003, Bits [15:12]**

| SWING – Bit pattern | Amplitude in mVpp | SWING – Bit pattern | Amplitude in mVpp |
|---|---|---|---|
| 0000 | 130 | 1000 | 830 |
| 0001 | 220 | 1001 | 930 |
| 0010 | 300 | 1010 | 1020 |
| 0011 | 390 | 1011 | 1110 |
| 0100 | 480 | 1100 | 1180 |
| 0101 | 570 | 1101 | 1270 |
| 0110 | 660 | 1110 | 1340 |
| 0111 | 750 | 1111 | 1400 |

### 4.1.2 Pre-Cursor – Register HS_SERDES_CONTROL_4, Device Address 0x1E Address 0x0005, Bits 7:4

With the bits [7:4] the pre-cursor component tap weight can be adjusted to improve the signal integrity. The bit patterns for the negative values are commonly used to adjust the transmitter for higher frequencies and longer transmission lines. This parameter will be optimized during link training.

**Table 4. Pre-Cursor bit Patterns and Corresponding Tap Weights in %, Device Address 0x1E, Register 0x0005, Bits [7:4]**

| TWPRE – Bit patterns | TWPRE - Value in % | TWPRE – Bit patterns | TWPRE - Value in % |
|---|---|---|---|
| 0000 | 0 | 1000 | 0 |
| 0001 | +2.5 | 1001 | - 2.5 |
| 0010 | +5.0 | 1010 | - 5.0 |
| 0011 | +7 .5 | 1011 | - 7.5 |
| 0100 | +10.0 | 1100 | - 10.0 |
| 0101 | +12.5 | 1101 | - 12.5 |
| 0110 | +15.0 | 1110 | - 15.0 |
| 0111 | +17.5 | 1111 | - 17.5 |

#### 4.1.3 Post-Cursor 1 – Register HS_SERDES_CONTROL_4, Device Address 0x1E Address 0x0005, Bits 12:8

The bits [12:8] are used to adjust the main portion of the post-cursor component tap weight. There is also a second post-cursor component (post-cursor 2), but this one has less effect on improving the signal condition than the post-cursor 1 and is rather used for fine-tuning. Post-cursor 1 is also a parameter which is optimized during link training.

**Table 5. Post-Cursor 1 Bit Patterns and Corresponding Tap Weights in %, Device Address 0x1E, Register 0x0005, Bits [12:8]**

| TWPOST1 – Bit pattern | TWPOST1 - Value in % | TWPOST1 – Bit pattern | TWPOST1 - Value in % |
|---|---|---|---|
| 00000 | 0 | 10000 | 0 |
| 00001 | +2.5 | 10001 | - 2.5 |
| 00010 | +5.0 | 10010 | - 5.0 |
| 00011 | +7.5 | 10011 | - 7.5 |
| 00100 | +10.0 | 10100 | - 10.0 |
| 00101 | +12.5 | 10101 | - 12.5 |
| 00110 | +15.0 | 10110 | - 15.0 |
| 00111 | +17.5 | 10111 | - 17.5 |
| 01000 | +20.0 | 11000 | - 20.0 |
| 01001 | +22.2 | 11001 | -22.2 |
| 01010 | +25.0 | 11010 | - 25.0 |
| 01011 | +27.5 | 11011 | - 27.5 |
| 01100 | +30.0 | 11100 | - 30.0 |
| 01101 | +32.5 | 11101 | - 32.5 |
| 01110 | +35.0 | 11110 | - 35.0 |
| 01111 | +37.5 | 11111 | - 37.5 |

### *4.2 Receiver Side*

#### 4.2.1 ENTRACK – Register HS_SERDES_CONTROL_3, Device Address 0x1E, Register Address 0x04, Bit 15

Activating this parameter adds intersymbol interference (ISI) to the received signal enabling the receiver to better compensate for short channel with little to no loss. An example application that would implement the ENTRACK feature is SFI/XFI applications, where the channel between SerDes and the optical channel is typically very short, to limit the amount of ISI.

#### 4.2.2 EQ – Register HS_SERDES_CONTROL_3, Device Address 0x1E, Register Address 0x04, Bits 14:12

The TLK10034 and TLK10232 both contain adaptive equalizers on the receiver side, which amplify the high-frequency content of the incoming signal. A transmission path has a low-pass filter characteristic, accordingly attenuating the higher frequencies in the signal. The equalizer takes a major effect, if the width of the eye is very small due to the low-pass filter characteristic of the channel. Through the amplification of the high-frequency content, the signal edges will become steeper and thus produce a wider eye. With the EQPRE parameter the amount of pre-cursor ISI compensation is configured. The amount of the post-cursor ISI compensation is handled by the device's adaptive DFE (Decision Feedback Equalizer) and needs no user configuration.

**Table 6. Equalizer Bit Patterns, EQPRE Values and Corresponding FIR Coefficients**

| EQPRE – Bit Pattern [14:12] | EQPRE Value | FIR Coefficient |
|---|---|---|
| 000 | 1/9 | 1/2 |
| 001 | 3/9 | 1/4 |

**Table 6. Equalizer Bit Patterns, EQPRE Values and Corresponding FIR Coefficients (continued)**

| EQPRE – Bit Pattern [14:12] | EQPRE Value | FIR Coefficient |
|---|---|---|
| 010 | 5/9 | 1/6 |
| 011 | 7/9 | 1/8 |
| 100 | 9/9 | 1/10 |
| 101 | 11/9 | 1/12 |
| 110 | 13/9 | 1/14 |
| 111 | Disable | — |

The selectable values in Table 6 do not directly represent the coefficient, which is used in the 2-Tap-FIR-Filter of the FFE (Feed Forward Equalizer), but have a correlation to the used value. The corresponding FIR coefficients to the EQPRE values in the datasheet are displayed in the right column of Table 6. The implementation of the DFE and FFE on the receiver side is illustrated in Figure 1.

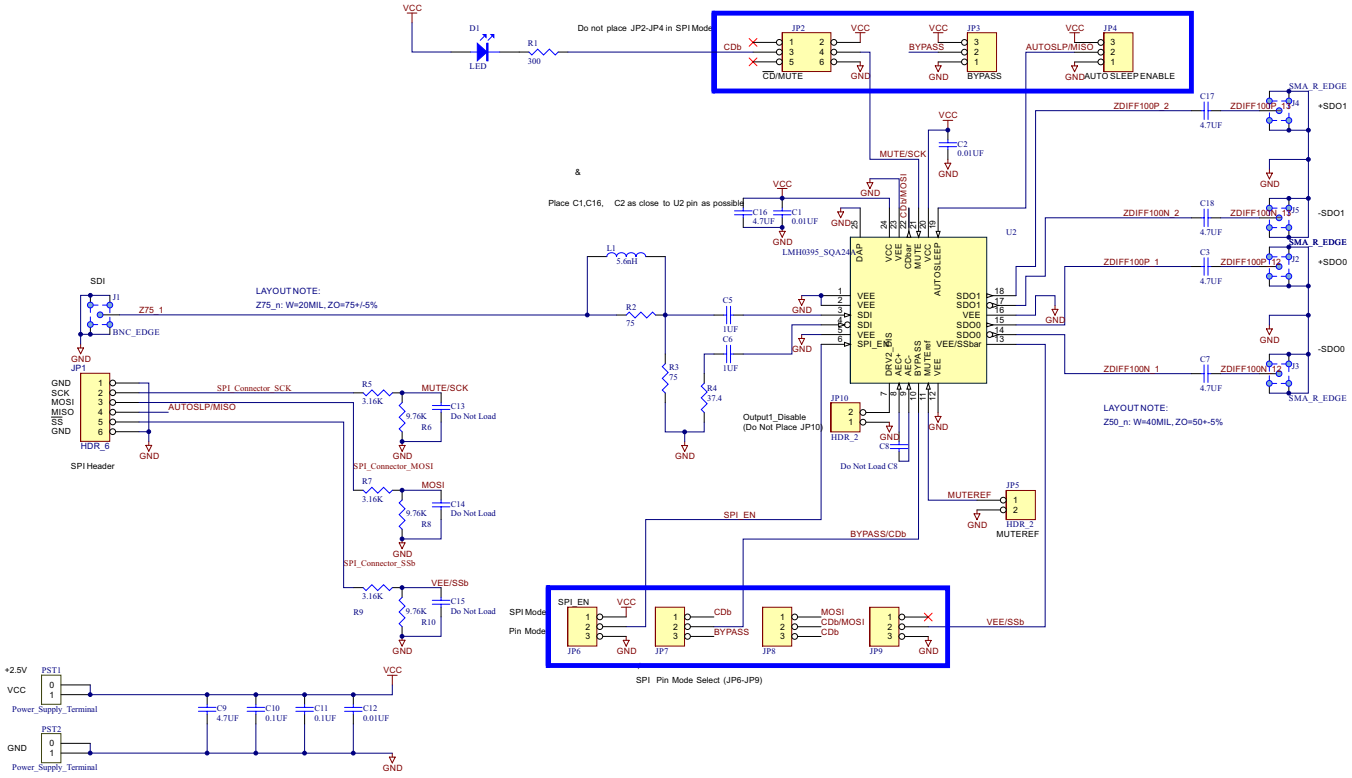


**Figure 1. Block Diagram of the DFE and FFE Implementation on the Receiver Side of TLK10034 and TLK10232**

## 5 Settings Which Influence Link Training Behavior

This section focuses on adjustments which can be made to improve the results of link training.

- Setting bit 9 under device address 0x01 (PMA), register 0x9001 will change the algorithm used for link training in the TLK10034. This influences the choice of final settings, which the device tested during link training. That algorithm is already set as default for the TLK10232.
- Another valuable adjustment can be, if under device address 0x01, register 0x9001 Bit 0 is set to 1. With this change t he device will gather more data during link training to find optimal settings, because it will use the full available PRE/post-cursor 1 range. Obviously this comes along with a longer time the device spends for link training.
- For link training, there is a certain amount of test attempts per measurement point. In register 0x9005 of the PMA layer, the number of training packets, which will be performed by link training, is stored.

The default value for the TLK10034 is 0x200 (decimal 512), for the TLK10232 it is 0x1C00 (decimal 7168). Improvements can be achieved by increasing the number of packets tested for both devices. The value 0x1C00, for example, will add additional workload for testing to the TLK10034. This leads to more time the process takes to complete but better overall results, because of more available test data. The time limit in IEEE 802.3 of 500 milliseconds will not be exceeded, in case a value of 0x1C00 or smaller is chosen.

The previously mentioned adjustments of this section usually have the biggest impact on link training performance and should always be attempted first, before trying to use one of the two following steps:

- Under device address 0x01, register 0x9001 with bits [7:4], different initial states for each different combination of settings can be enabled. A bit pattern of 1000 toggles the ENTRACK function at the beginning of link training. Setting these bits to 0100 will repeat the auto-zero calibration process. 0010 will toggle the receiver enable. A value of 0011 will reset the taps of the decision feedback equalizer. All of those bit patterns can also be combined.
- In register 0x9006 of the PMA layer bits [15:0] can be used to adjust the settling time between a change of parameters and the occurrence of the actual BER measurement. The default value of the register is 0x0000.

## 6 Evaluation of Link Training Results to Quantify Link Margin

The evaluation of link training data is very important to quantify the link margin. The real link might not exactly match the measured result, because there is always a limited time for a measurement to be completed.

As was already explained in Section 1.2, setting bit 12 under device address 0x01 in register 0x9 001 initiates the read out process starting with the minimum post-cursor 1 de-emphasis level. This only has to be done once at the beginning of the read out process. For the TLK10034, the BER data is stored in register 0x9012 (device address 0x01). Reading this register again will make the BER data of the next data set available. This procedure should be repeated until the data of every single link training step was obtained. The same procedure applies for the TLK10232 with the exception that for this device the BER data is located in register 0x9022, also under device address 0x01.

A transmission parameter setting can be characterized with high link margin, if as many adjacent settings (next possible variations of pre-cursor, post-cursor 1, SWING, EQPRE and ENTRACK values) as possible are all also error-free. The bigger the area with 0 BER, the better is the link margin.

For example, a read out of the pre-cursor and post-cursor 1 settings, like described in Section 1.2, can be graphically displayed with post-cursor 1 on the x-axis and pre-cursor on the y-axis. The best operation point can then be chosen by selecting one in the center of the biggest field with zero bit errors. In this case, the other parameters SWING, EQPRE, and ENTRACK are fixed to one specific setting.

Choosing a set of parameters within a high link margin area will give more safety that the link will stay error-free.

## 7 Link Down Issues and Solving Them

Registers and bits mentioned in this section are the same for TLK10034 and TLK10232.

If the link goes down, take the following actions:

1. Verifying that the link is down can be checked in the PMA_STATUS_1 register (device address 0x01, register 0x0001) if bit 2 equals 0.
2. If auto negotiation is enabled and fails after a data path reset, bit 5 in register 0x0001 (device address 0x07) will be read as 0. This case is most likely the first indication that there is an issue with the transmission path, because auto negotiation is running before link training.
3. A restart of link training should be initiated (under device address 0x01, in register 0x0096 LT_TRAIN_CONTROL set bit 0) just in case the link has changed. The bit will be cleared automatically. The verification that link training failed can be read from register 0x97, by checking, if bit 3 is set.
4. If the link does not come up again after link training was restarted on both devices, there is probably a problem with the transmission path. Restarting or power cycling the whole device is usually not necessary in those cases.

## 8 References


- *TLK10034 quad-channel XAUI/10GBASE-KR transceiver* (SLLSEC7)
- *TLK10232 dual-channel XAUI/10GBASE-KR transceiver with crosspoint* (SLLSEE1)
- IEEE802.3 – 2008 (http://www.ieee802.org/)

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (December 2014) to A Revision | Page |
|---|---|
| • Added content to Section 2 | 2 |

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