EVM User's Guide: AFE532A3WEVM

AFE532A3W Evaluation Module

Description

The AFE532A3WEVM is an easy-to-use platform to evaluate the functionality and performance of the AFEx32A3W commercial devices. The AFE532A3WEVM has optional circuits and jumpers to configure the AFE for different applications. The AFE532A3WEVM features two AFEx32A3W devices, referred to in this document as primary AFEx32A3W and auxiliary AFEx32A3W.

The 10-bit AFE532A3W, and 8-bit AFE432A3W are a pin-compatible family of three-channel, buffered, voltage-output (VOUT) and current-output (IOUT) smart analog front ends (AFEs). The AFE has two integrated digital-to-analog converters (DACs) and one channel that can be configured as a DAC or an analog-to-digital converter (ADC). The current output DAC has a 300-mA full scale range. The AFEx32A3W supports Hi-Z power-down mode and Hi-Z output during power-off conditions.

Get Started

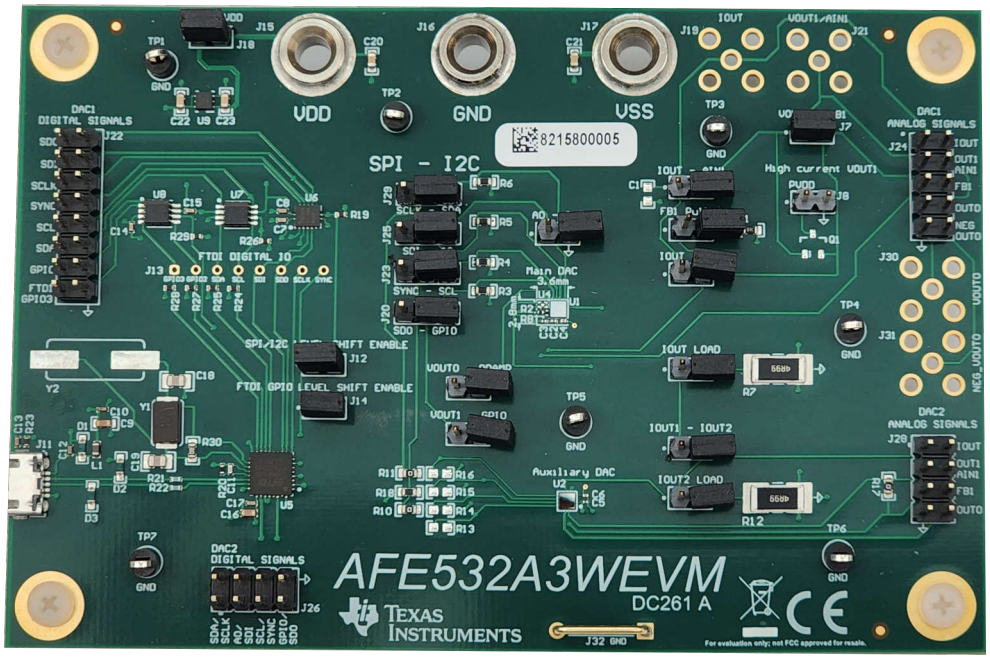
1. Order the EVM on ti.com.
2. Download and install the AFE532A3WEVM software.
3. Configure the hardware jumper settings.
4. Connect the USB and external AFE532A3WEVM supplies.
5. Launch the AFE532A3WEVM GUI.

Features

- Onboard 3.3-V VDD supply
- Jumpers to evaluate different AFE configurations
- Output voltage inverter circuit
- Onboard FT4222 controller for SPI or I^2C communication

Applications

- Optical module
- High performance computing
- Standard notebook PC



1 Evaluation Module Overview

1.1 Introduction

The multi-functional GPIO, function generation, and nonvolatile memory (NVM) enable these smart AFEs for use in applications and design reuse without the need for runtime software. These devices also automatically detect I^2C, SPI, and PMBus interfaces, and contain an internal reference.

This user's guide describes the characteristics, operation, and use of the AFE532A3WEVM evaluation module (EVM). This EVM is designed to evaluate the performance of the AFE532A3W and AFE432A3W commercial, buffered current and voltage output DACs in a variety of configurations. Throughout this document, all these devices are referred to as the AFEx32A3W, and the terms evaluation board, evaluation module, and EVM are synonymous with the AFE532A3WEVM. This document includes a schematic, printed-circuit board (PCB) layouts, and a complete bill of materials (BOM).

1.2 Kit Contents

Table 1-1 details the contents of the EVM kit. Contact the nearest TI Product Information Center if any component is missing. Make sure to verify the latest versions of the related software at the Texas Instruments website, www.ti.com.

Table 1-1. Contents of AFE532A3WEVM Kit

Item	Quantity
AFE532A3WEVM evaluation board PCB	1
USB micro-B plug to USB-A plug cable	1

1.3 Specification

Figure 1-1 shows a simplified schematic of the AFE532A3WEVM board. There are three connectors that provide access to all of the digital and analog signals on the EVM. The GPIO, I^2C, and SPI signals from the onboard controller are connected to the AFEx32A3W through two level translators. The level translators can be disabled to disconnect the onboard controller GPIO, I^2C, and SPI signals from the AFEx32A3W.

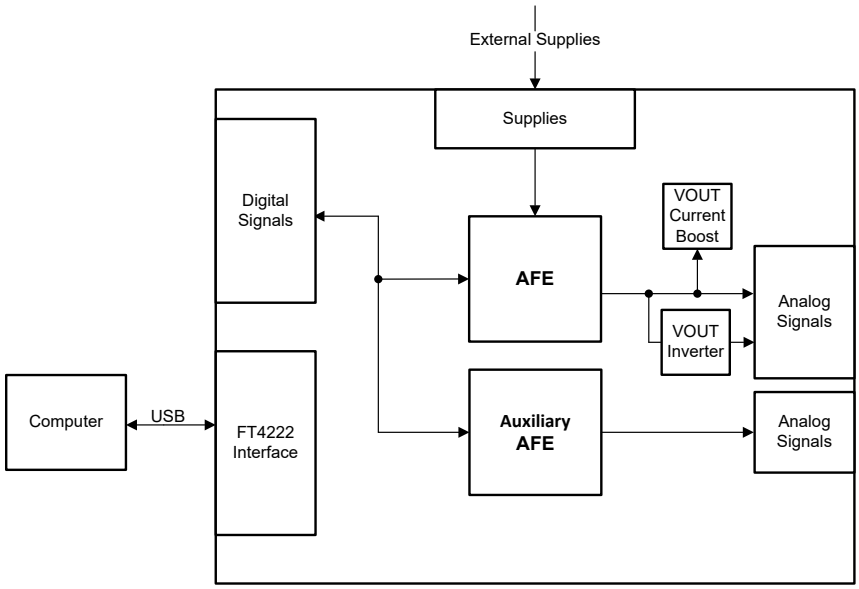


Figure 1-1. AFE532A3WEVM Simplified Schematic

1.4 Device Information

The following document provides information regarding Texas Instruments integrated circuits used in the assembly of the AFE532A3WEVM. This user's guide is available from the TI web site under literature number SLAU900. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions are available from the TI web site at www.ti.com, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

Table 1-2. Related Documentation

Document	Literature Number
AFE532A3W product page	SLASFB2
AFE432A3W product page	

2 Hardware

2.1 Hardware Setup

This section describes the overall system setup for the EVM. A computer runs the software that provides an interface to the AFE532A3WEVM through the onboard controller.

The USB connection generates a 5-V supply for the EVM. The onboard controller generates 3.3 V of power for the input/output (IO) signals generated by the onboard controller. These IO signals are level translated to the VDD voltage of the AFEx32A3W. An onboard, 3.3-V voltage regulator generates 3.3 V for use as the AFEx32A3W supply voltage (VDD).

2.1.1 Electrostatic Discharge Caution

CAUTION

Many of the components on the AFE532A3WEVM are susceptible to damage by electrostatic discharge (ESD). Observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

2.1.2 Power Configurations and Jumper Settings

The AFE532A3WEVM provides electrical connections to the device supply pins. Table 2-1 and Figure 2-1 shows the power supply connections.

Table 2-1. AFE532A3WEVM Power Supply Inputs

AFE532A3WEVM Connector	Supply Name	Voltage Range
J15	VDD	3 V to 5.5 V; remove jumper J18 if applying an external VDD to the device.
J16	GND	0 V
J17	VSS	–1.5 V to –5 V; required to use the inverting op-amp circuit.
J8	PVDD	PVDD supply for the VOUT1 current boost circuit

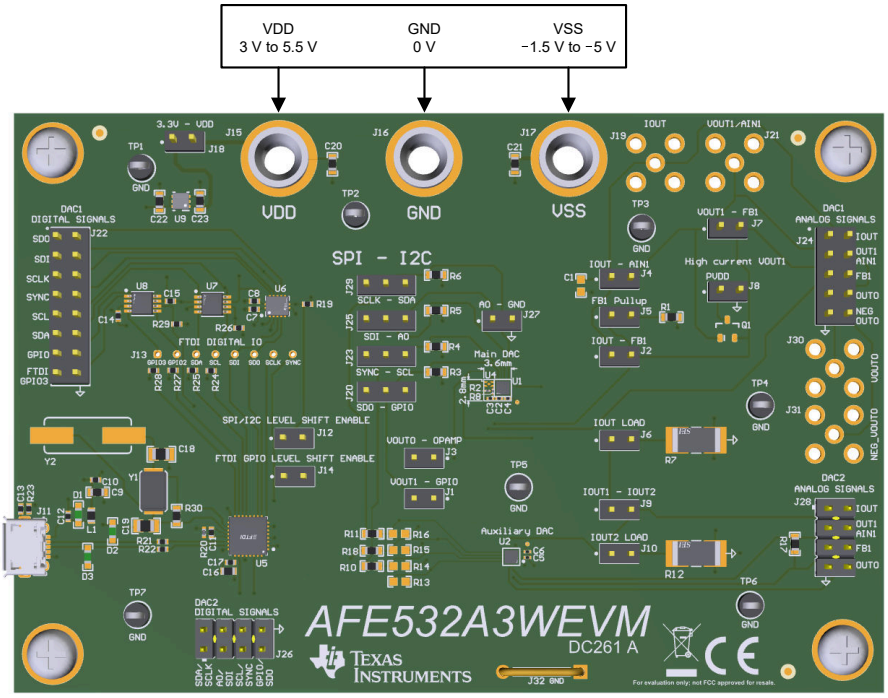


Figure 2-1. AFE532A3WEVM Power Supply Inputs

Table 2-2 provides the details of the configurable jumper settings on the AFE532A3WEVM.

Table 2-2. AFE532A3WEVM Jumper Settings

Jumper	Default Position	Available Option	Description
J1	Open: VOUT1 disconnected from GPIO/SDO	Closed: VOUT1 connected to GPIO/SDO	Connects VOUT1 to GPIO/SDO
J2	Open: IOUT disconnected from FB1	Closed: IOUT connected to FB1	Connects IOUT to FB1 (comparator input)
J3	Open: VOUT0 disconnected from op-amp input	Closed: VOUT0 connected to op-amp input	Connects VOUT0 to the op-amp input pin
J4	Open: IOUT disconnected from AIN1	Closed: IOUT connected to AIN1	Connects IOUT to AIN1 (ADC input)
J5	Open: FB1 disconnected from 10-kΩ pullup resistor	Closed: FB1 connected to 10-kΩ pullup resistor	Connect FB1 to a 10-kΩ pullup resistor
J6	Open: IOUT disconnected from 4.99-Ω load	Closed: IOUT connected to 4.99-Ω load	Connects IOUT to a 4.99-Ω load
J7	Closed: VOUT1 connected to FB1	Open: VOUT1 disconnected to FB1	Connects VOUT1 to FB1
J9	Open: IOUT disconnected from IOUT2	Closed: IOUT connected to IOUT2	Connects IOUT to IOUT2
J10	Open: IOUT2 disconnected from 4.99-Ω load	Closed: IOUT2 connected to 4.99-Ω load	Connects IOUT2 to a 4.99-Ω load
J12	Closed: FTDI SPI and I^2C enabled	Open: FTDI SPI and I^2C disabled	Enables the FTDI SPI and I^2C level translators
J14	Closed: FTDI GPIOs enabled	Open: FTDI GPIOs disabled	Enables the FTDI GPIO level translators
J18	Closed: 3.3-V supply connected to VDD	Open: 3.3-V supply disconnected from VDD	AFE VDD supply selection
J20	1-2: GPIO connected to AFE	2-3: SDO connected to AFE	I^2C or SPI selection
J23	1-2: SCL connected to AFE	2-3: SYNC connected to AFE	I^2C or SPI selection
J25	1-2: A0 connected to AFE	2-3: SDI connected to AFE	I^2C or SPI selection
J29	1-2: SDA connected to AFE	2-3: SCLK connected to AFE	I^2C or SPI selection

If an external supply is applied to J15, then remove jumper J18 to disconnect the 3.3-V regulator supply from the AFEx32A3W VDD pin.

GPIO2 and GPIO3 from the onboard controller are configured as outputs when the AFE532A3WEVM is controlled with the GUI. GPIO2 from the onboard controller is connected to the GPIO/SDO pin of the AFEx32A3W. If the AFE SDO pin is configured as an output, then remove jumper J14 to disable the GPIOs from the onboard controller.

Figure 2-2 shows the default jumper settings on the AFE532A3WEVM.

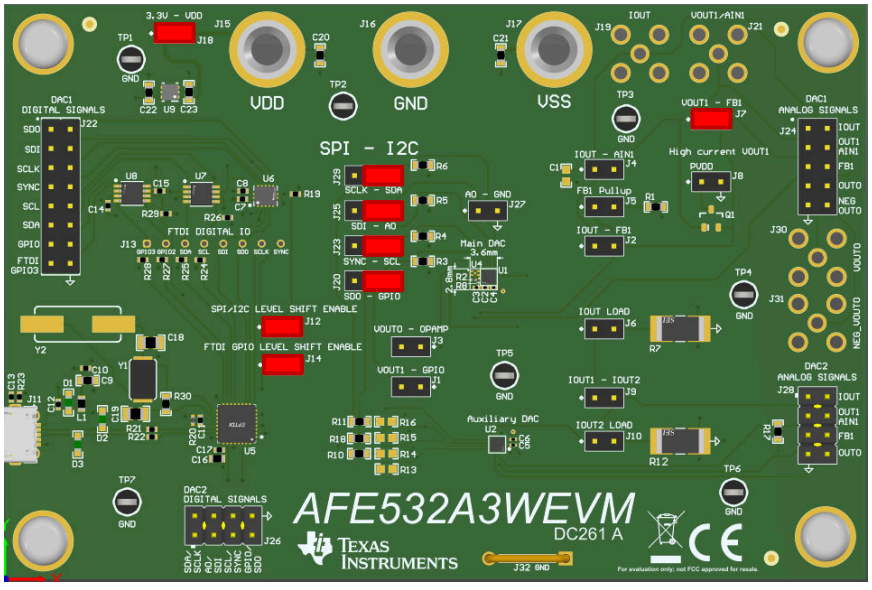


Figure 2-2. AFE532A3WEVM Default Jumper Settings

The AFE532A3WEVM has an optional inverting op-amp circuit that can be used to invert the VOUT0 output of the primary AFEx32A3W. Figure 2-3 shows how to configure the jumpers to enable the inverting op-amp circuit. VSS is connected to the negative supply of the inverting op-amp. Connect a –1.5-V to –5-V supply to J17 before closing jumper J3. The positive supply of the inverting op-amp is connected to ground.

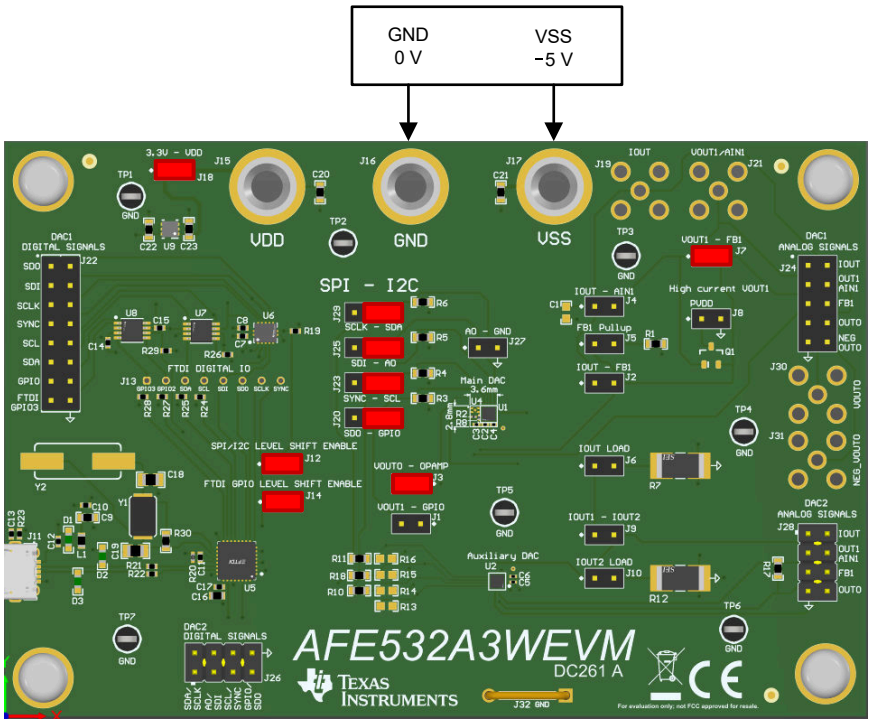


Figure 2-3. AFE532A3WEVM Inverting Op-amp Jumper Settings

The IOUTs of the primary and auxiliary AFEx32A3W devices can be connected in parallel to increase the total current output. Figure 2-4 shows the jumper configuration to connect the IOUTs in parallel. Close jumper J6 and/or jumper J10 to connect the resistive load to the parallel IOUT. An external VDD needs to be used if the combined current output exceeds the current limit of the USB port and/or the 500-mA current rating of the onboard regulator.

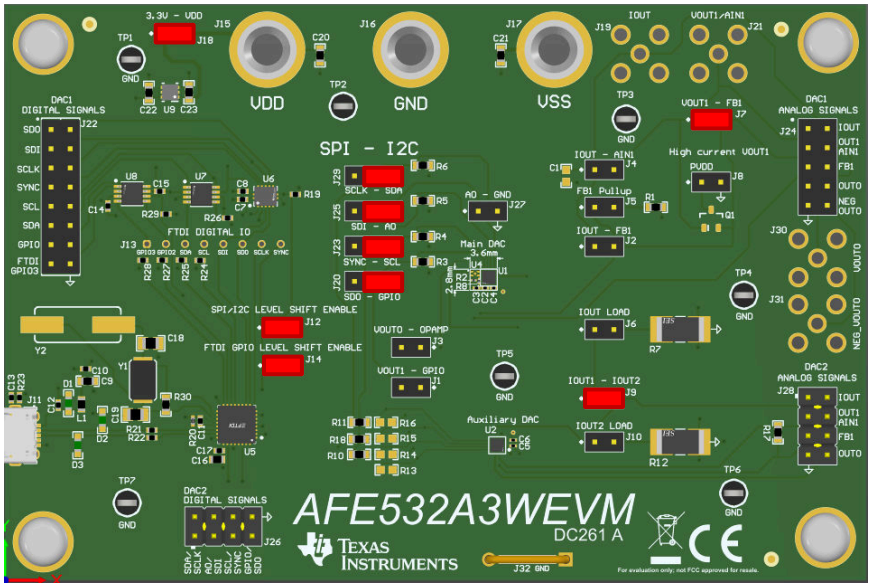


Figure 2-4. AFE532A3WEVM Parallel IOUT Jumper Settings

The AFEx32A3W can be used to monitor signals using the integrated programmable comparator. Figure 2-5 shows how to configure the AFE532A3WEVM jumpers to connect the IOUT pin to the comparator input and connect the comparator output to the GPIO/SDO pin. When the voltage across the 4.99-Ω load crosses a programmed threshold, the comparator output connected to the GPIO/SDO pin can be used to trigger alarm conditions or enter power-down mode.

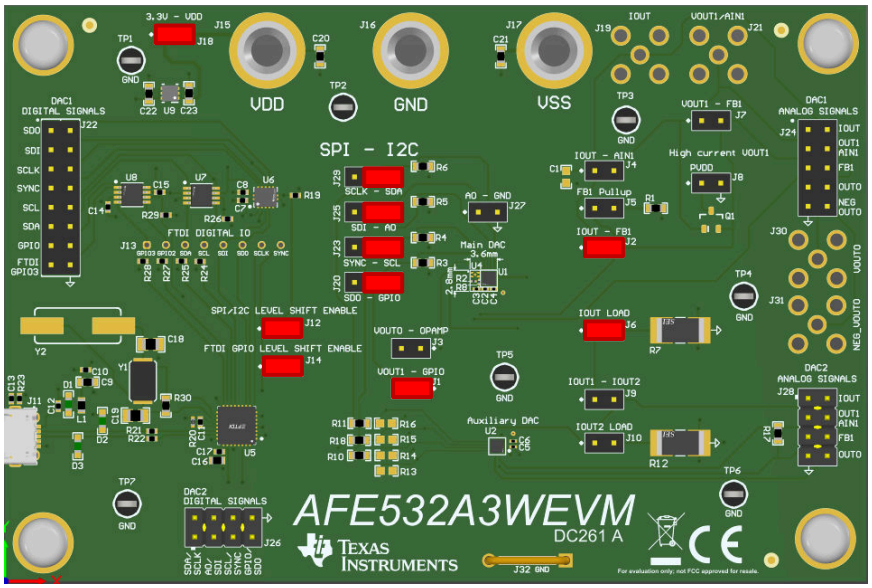


Figure 2-5. AFE532A3WEVM Comparator Input Jumper Settings

Figure 2-6 shows the jumper configuration to connect the IOUT pin to the ADC input. The ADC can be used to monitor the IOUT when the IOUT is connected to the 4.99-Ω load.

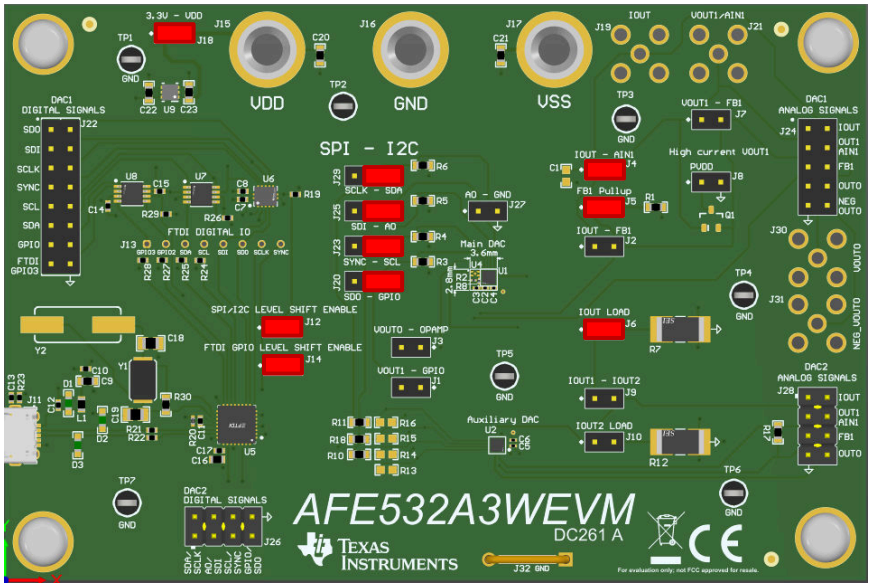


Figure 2-6. AFE532A3WEVM ADC Input Jumper Settings

2.1.3 Connecting the Hardware

After the power and jumper configurations are set up as per Section 2.1.2, connect the USB cable from the AFE532A3WEVM USB port to the computer.

2.2 Hardware Description

The following sections provide detailed information on the EVM hardware.

2.2.1 Signal Definitions

The AFE532A3WEVM provides access to all AFEx32A3W pins through connectors J22, J24, J26, and J28. J22 and J24 provide access to the pins of the primary AFEx32A3W. Table 2-3 and Table 2-4 list the J22 and J24 pin definitions.

Table 2-3. AFE532A3WEVM J22 Pin Definitions

Pin#	Signal	Description
1	SDO	SPI SDO
2	GND	Ground
3	SDI	SPI SDI
4	GND	Ground
5	SCLK	SPI SCLK
5	GND	Ground
7	SYNC	SPI SYNC
6	GND	Ground
9	SCL	I^2C SCL
10	GND	Ground
11	SDA	I^2C SDA
12	GND	Ground
13	GPIO	AFE GPIO
14	GND	Ground
15	FTDI_GPIO3	GPIO3 output of the on-board controller

Table 2-4. AFE532A3WEVM J24 Pin Definitions

Pin#	Signal	Description
1	GND	Ground
2	IOUT	Primary AFEx32A3W IOUT
3	GND	Ground
4	VOUT1/AIN1	Primary AFEx32A3W VOUT1/AIN1
5	GND	Ground
6	FB1	Primary AFEx32A3W FB1
7	GND	Ground
8	VOUT0	Primary AFEx32A3W VOUT0
9	GND	Ground
10	Negative VOUT0	Primary AFEx32A3W negative VOUT0

J26 and J28 provide access to the pins of the auxiliary AFEx32A3W. Table 2-5 and Table 2-6 list the J26, and J28 pin definitions.

Table 2-5. AFE532A3WEVM J26 Pin Definitions

Pin#	Signal	Description
1	SDA/SCLK	Auxiliary AFEx32A3W SDA/SCLK
2	GND	Ground
3	A0/SDI	Auxiliary AFEx32A3W A0/SDI
4	GND	Ground
5	SCL/SYNC	Auxiliary AFEx32A3W SCL/SYNC
6	GND	Ground
7	GPIO/SDO	Auxiliary AFEx32A3W GPIO/SDO
8	GND	Ground

Table 2-6. AFE532A3WEVM J28 Pin Definitions

Pin#	Signal	Description
1	GND	Ground
2	IOUT	Auxiliary AFEx32A3W SDA/SCLK
3	GND	Ground
4	VOUT1/AIN1	Auxiliary AFEx32A3W VOUT1/AIN1
5	GND	Ground
6	FB1	Auxiliary AFEx32A3W FB1
7	GND	Ground
8	VOUT0	Auxiliary AFEx32A3W VOUT0

2.2.2 Optional Circuitry

The AFE532A3WEVM has optional circuitry that can be used to evaluate the AFEx32A3W.

The AFEx32A3W can be used in optical module applications that require up to a 300 mA current source and a negative bias voltage. The negative bias voltage is generated by connecting the voltage output of the AFEx32A3W to an inverting op-amp. Figure 2-7 shows the block diagram for the negative bias circuit.

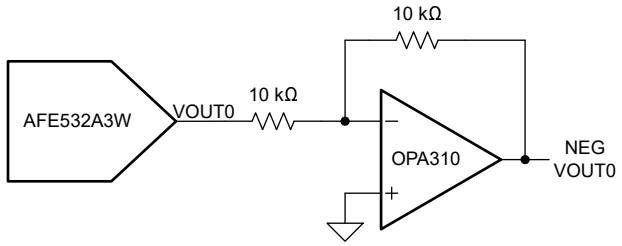


Figure 2-7. AFE532A3WEVM Negative Bias Circuit Block Diagram

Figure 2-8 shows the 2.8-mm × 3.6-mm negative bias circuit layout. The layout consists of the AFEx32A3W, OPA310, two size-0201 resistors, and three size-0201 capacitors.

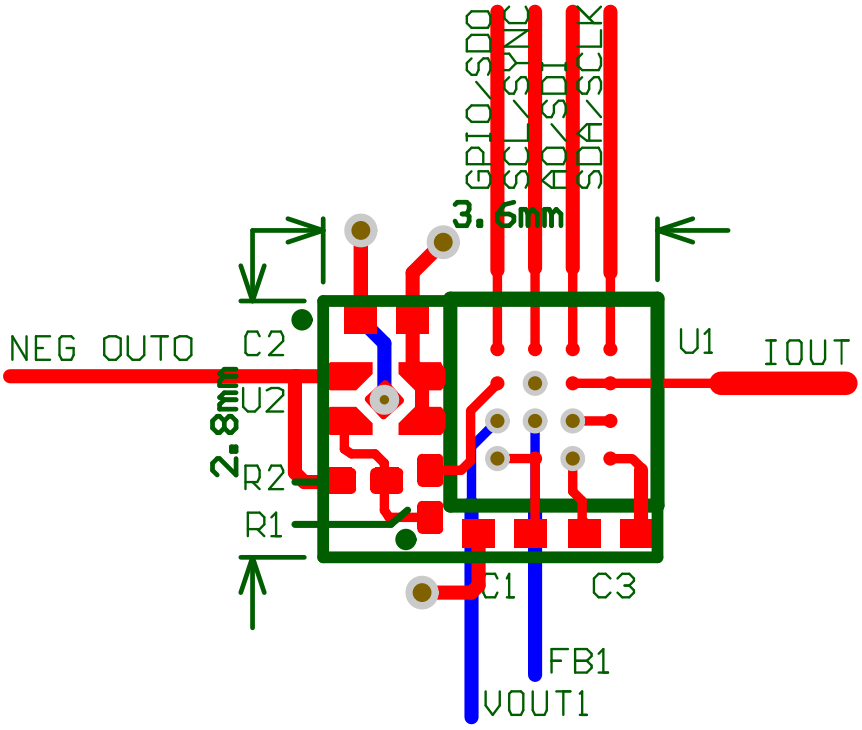


Figure 2-8. AFE532A3WEVM Negative Bias Circuit Layout

The output current capability of the AFEx32A3W VOUT channels can be increased with an external current boost circuit. Figure 2-7 shows the block diagram for the high current, voltage output circuit. Q1 is not populated on the AFE532A3WEVM. Remove the shunt from J7 before populating Q1. Connect PVDD to pin 1 of J8 and connect the load to the AFEx32A3W FB1 pin on pin 6 of J24.

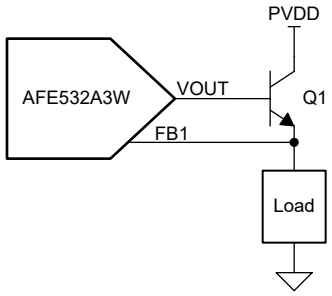


Figure 2-9. AFE532A3WEVM High Current Output Stage Block Diagram

3 Software

3.1 Software Setup

This section provides the procedure for EVM software installation.

3.1.1 Operating Systems

The EVM software is compatible with the Windows™ 10 operating system.

3.1.2 Software Installation

Make sure that the AFE532A3WEVM is not connected to the computer during the software installation.

The AFE532A3WEVM software can be downloaded from the device product folders or AFE532A3WEVM tool folder. After the software is downloaded, navigate to the download folder, and run the SMART-DAC-EVM-GUI installer executable.

When the AFE532A3WEVM software is launched, an installation dialog window opens and prompts the user to select an installation directory. Figure 3-1 shows that the software path defaults to *C:\Program Files (x86)\Texas Instruments\SMART-DAC-EVM-GUI*.

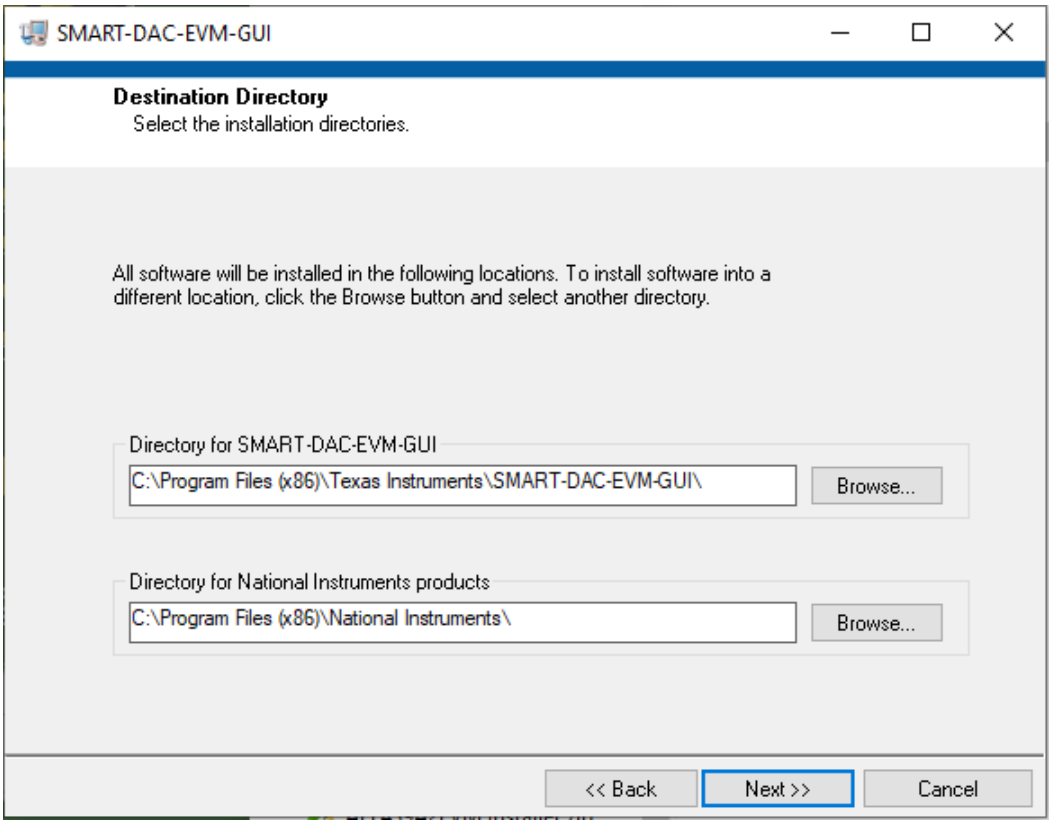


Figure 3-1. Software Installation Path

The software installation also installs the FTDI USB drivers, and automatically copies the required LabVIEW™ software files and drivers to the computer. The FTDI USB drivers install in a second executable. Figure 3-2 shows the window that is automatically launched after the software installation is complete.

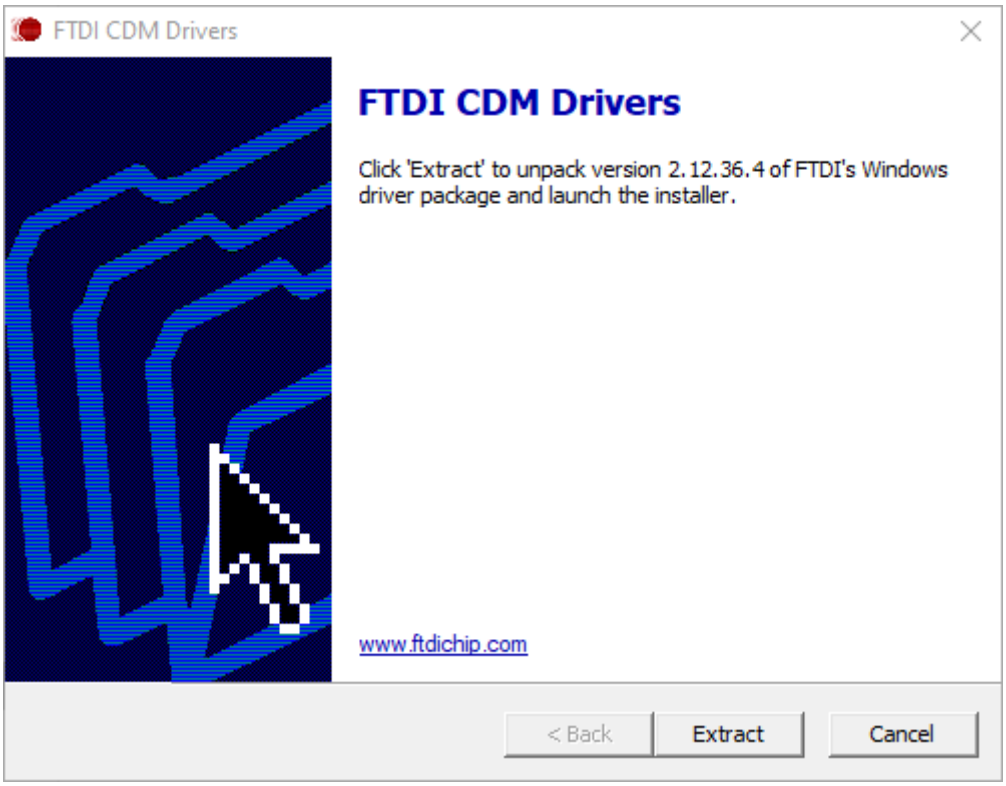


Figure 3-2. FTDI USB Drivers

3.2 Software Description

This section describes the features of the AFE532A3WEVM software, and discusses how to use these features. The software provides basic control of all the AFEx32A3W registers and functions.

3.2.1 Starting the Software

To launch the software, navigate to the SMART-DAC-EVM folder in the *Start* menu, and select the SMART-DAC-EVM icon.

Figure 3-3 shows the *Device Selector* window that pops up on start up. This window contains a drop-down menu to select which device register map is loaded into the GUI. Select the AFE532A3W when using the AFE532A3WEVM.

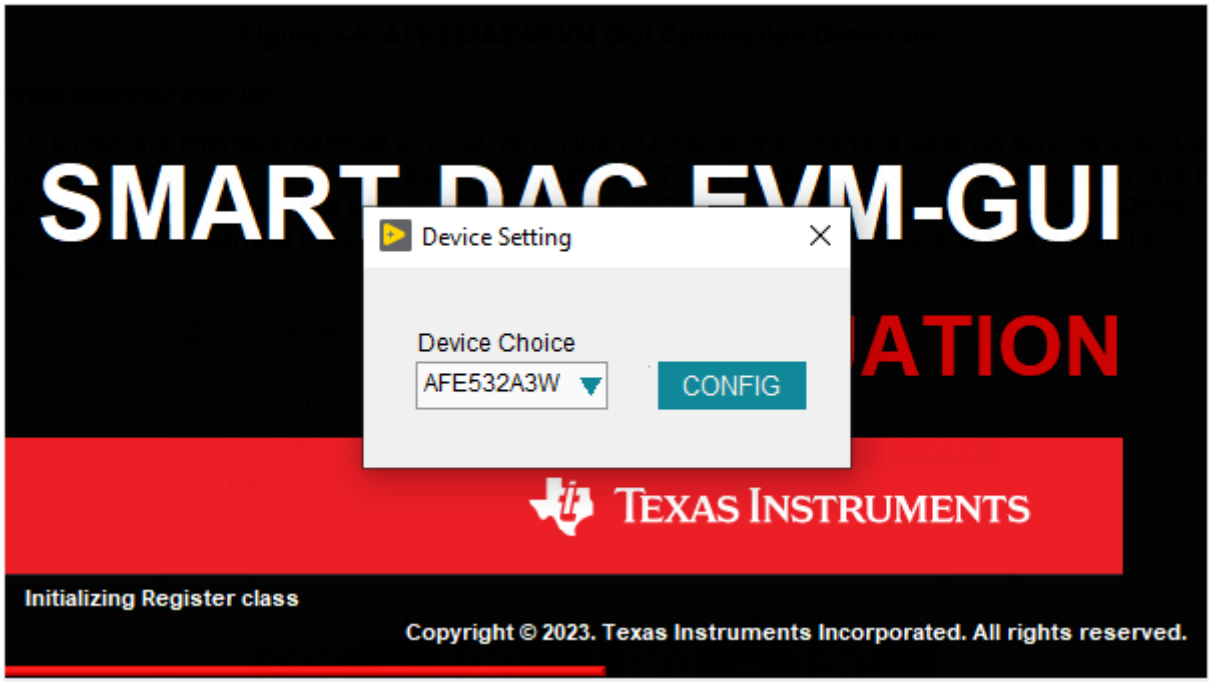


Figure 3-3. Device Selector

Figure 3-4 shows that if the onboard controller is connected correctly, the status bar at the bottom of the screen displays *CONNECTED*. If the controller is not properly connected or not connected at all, the status displays *DEMO*. If the GUI is not displaying the *CONNECTED* status while the EVM is connected, unplug and reconnect the EVM, and then relaunch the GUI software. If the display continues to display DEMO, uncheck the *Demo Mode* checkbox (see Figure 3-6, upper-right corner).

Figure 3-4. GUI Connection Detection

Figure 3-5 shows the *Interface Settings* window. When the GUI starts, the *Interface Settings* window pops up. This window contains drop-down menus that select protocol (SPI or I^{2}C) and, if I^{2}C protocol is selected, the I^{2}C device address. The menu does not pop up if the GUI starts in Demo mode. In this case, uncheck the *Demo Mode* checkbox. If the interface must be updated again, toggle the *Demo Mode* checkbox for the menu to reappear.

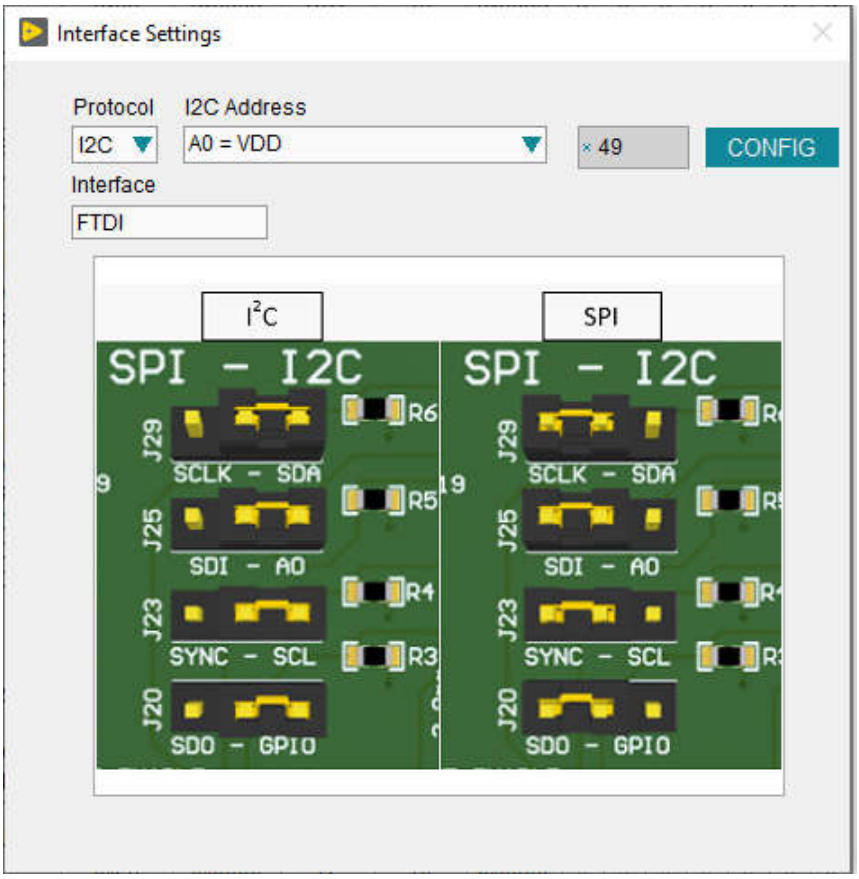


Figure 3-5. Interface Settings

3.2.2 Software Features

The AFE532A3WEVM GUI incorporates interactive functions that help configure an individual AFEx32A3W device using I^2C or SPI communication. These functions are built into several GUI pages, as shown in the following subsections. The menu bar on the far left of the GUI allows the user to switch between pages. The menu bar displays the *High Level Configuration* page, with the *Basic DAC* subpage, and the *Low Level Configuration* page.

Before using the GUI, see the respective device data sheet for detailed AFEx32A3W programming instructions.

3.2.2.1 High Level Configuration Page

Figure 3-6 shows the *High Level Configuration* page that provides an interface to quickly configure the parameters and relevant register settings for the respective AFEx32A3W device. The *High Level Configuration* page consists of the *Basic DAC* subpage.

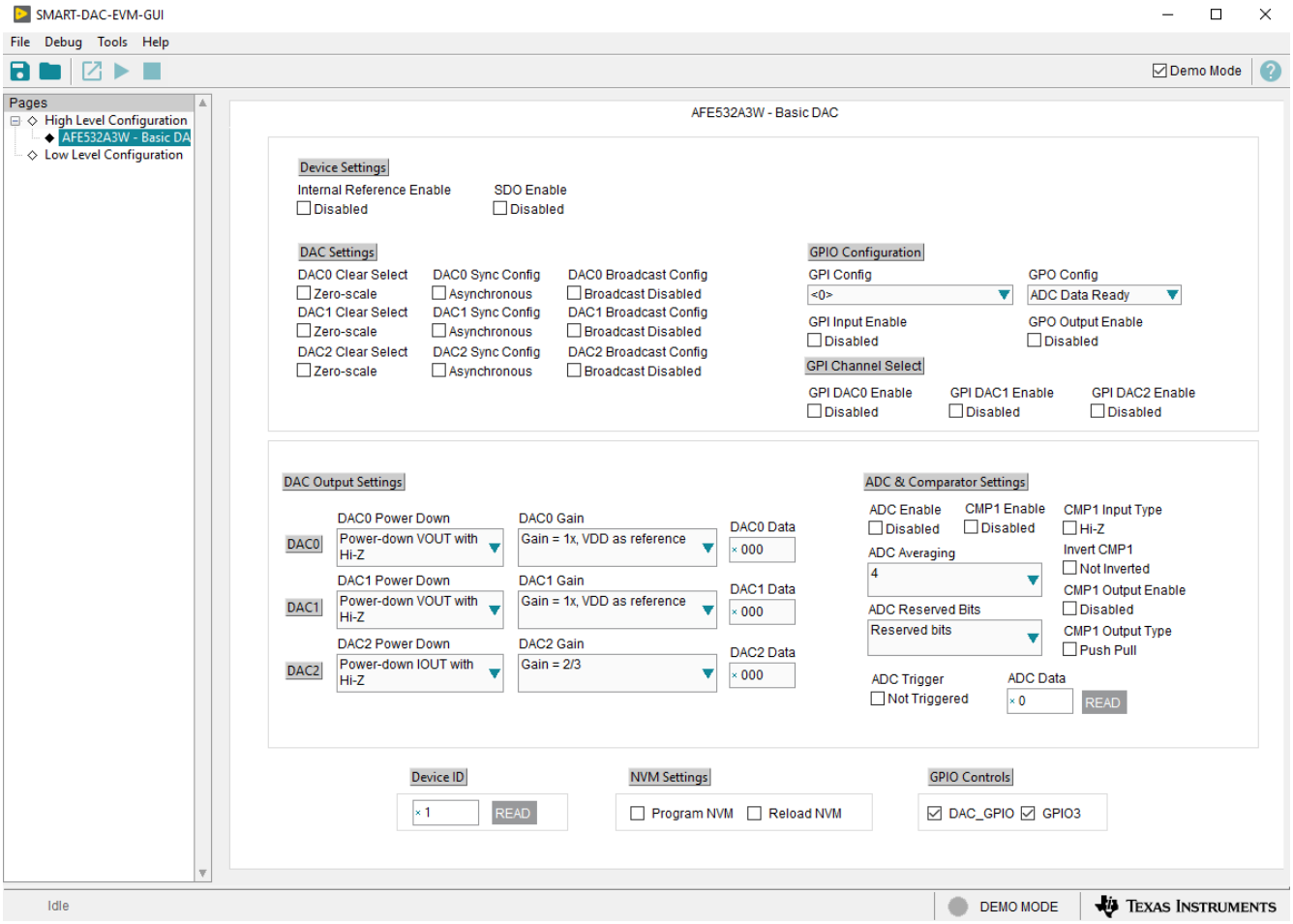


Figure 3-6. High Level Configuration Page

3.2.2.1.1 Basic DAC Subpage

Figure 3-7 shows the *Basic DAC* subpage that provides an interface to quickly power up, select the reference and output span, program the output voltage or current, and configure the ADC for the respective AFEx32A3W device. The *Basic DAC* subpage also provides controls to configure the GPIO pin on the respective AFEx32A3W device, and control the two GPIO outputs of the AFE532A3WEVM onboard controller. The register settings can be programmed or retrieved using the *Program NVM* or *Reload NVM* checkboxes, respectively.

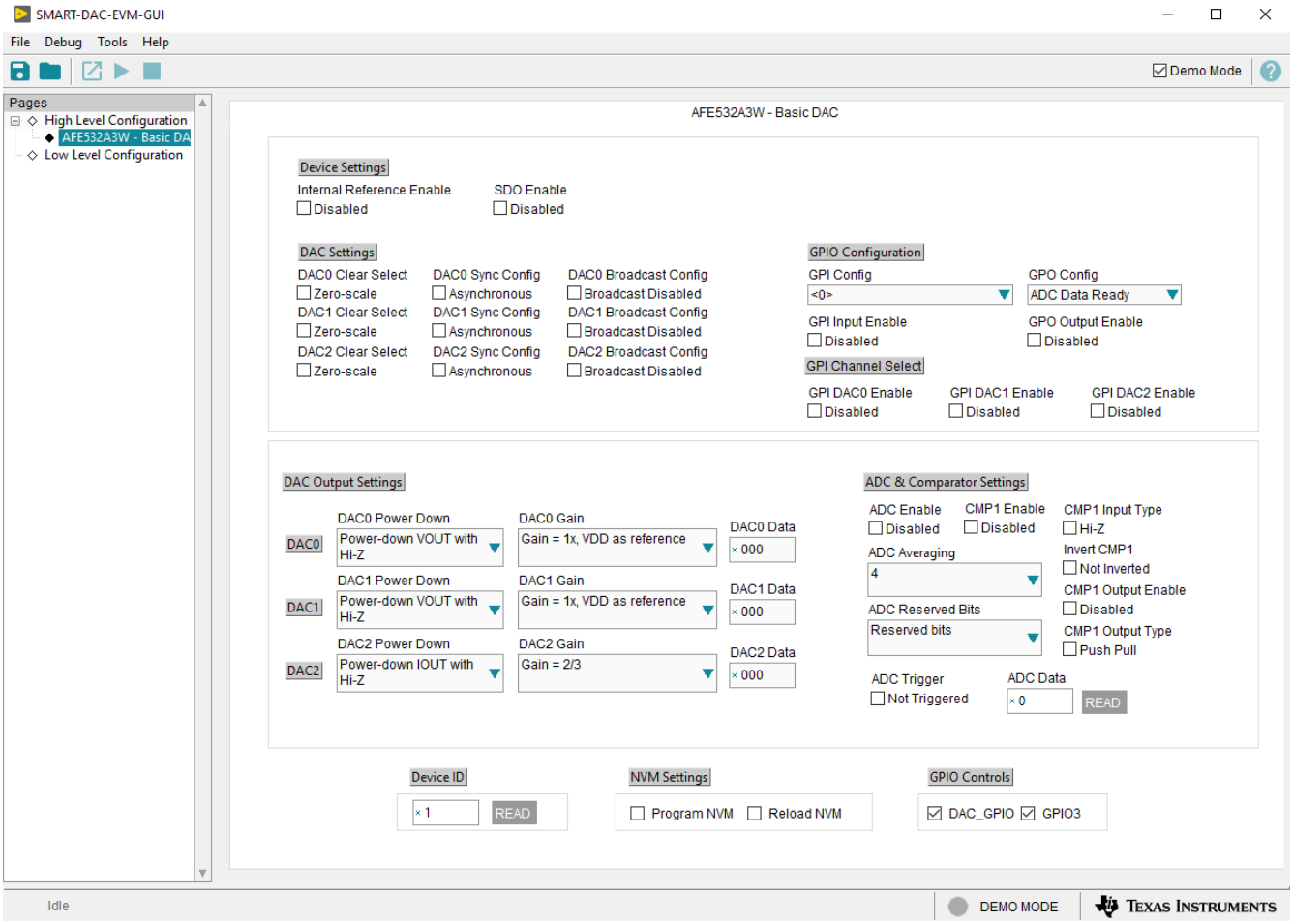


Figure 3-7. Basic DAC Subpage

3.2.2.2 Low Level Configuration Page

Figure 3-8 shows the *Low Level Configuration* page. This subpage allows access to low-level communication directly with the respective AFEx32A3W device registers. Select a register on the *Register Map* list to show a description of the values in that register, as well as information on the register address, default value, size, and current value. Data are written to the registers by entering a value in the value column of the GUI.

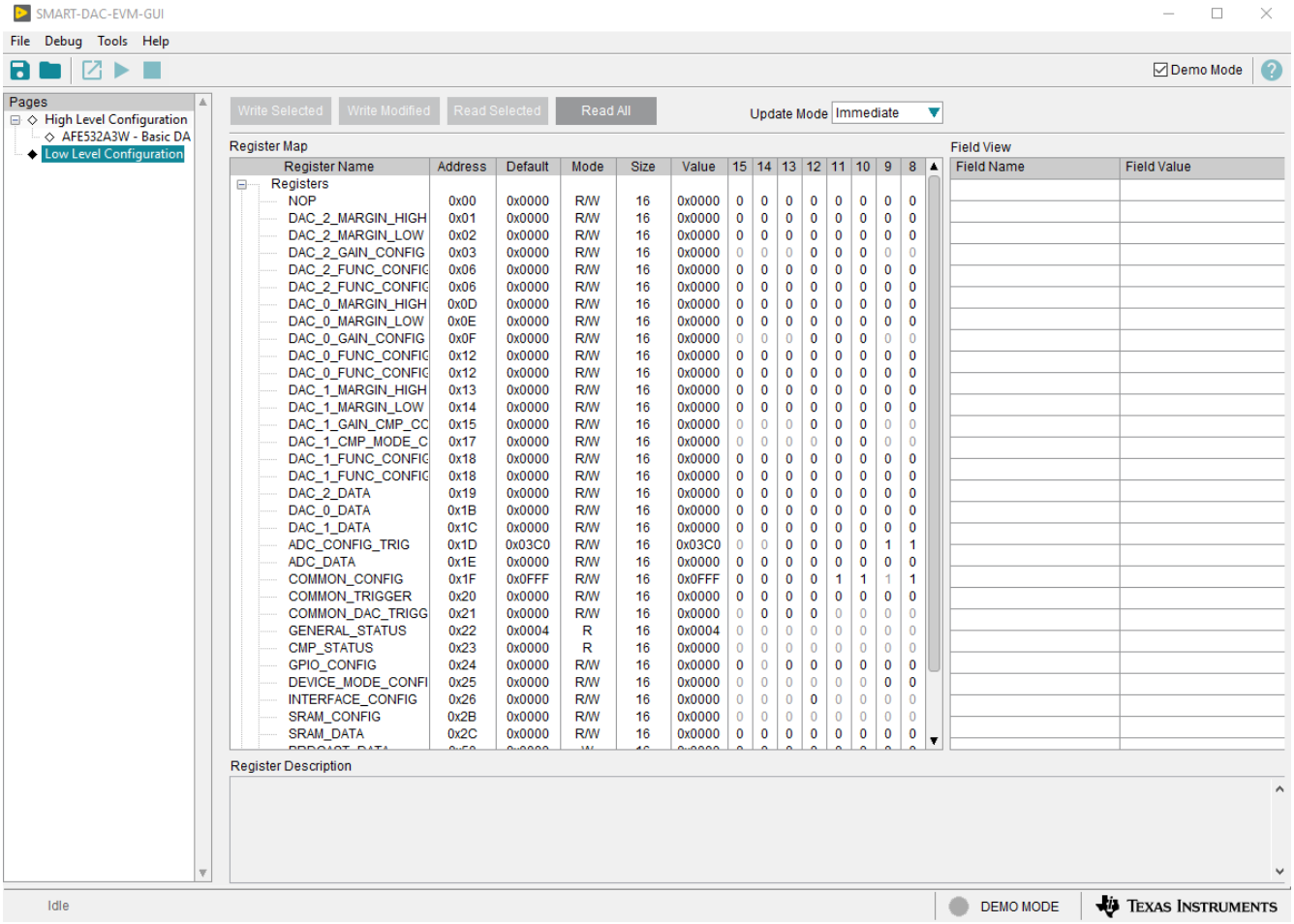


Figure 3-8. Low Level Configuration Page

To store the values of the register map locally, select *Save Configuration* under the *File* menu option. The stored configuration files can be recalled and loaded by selecting *Open Configuration*.

Figure 3-9 shows the four configuration buttons provided on the *Low Level Configuration* page that allow the user to read from and write to the device registers:

- **Write Selected**
- **Write Modified**
- **Read Selected**
- **Read All**

The **Write Modified** button is enabled only in *Deferred Update Mode*. *Deferred Update Mode* initiates a write operation only when the **Write Selected** or **Write Modified** buttons are pressed. By default, *Immediate Update Mode* is selected for the *Low Level Configuration* page write operations.

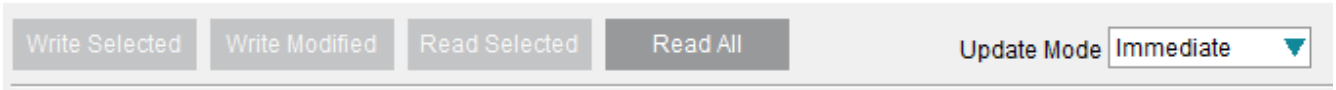


Figure 3-9. Low Level Configuration Page Options

4 Hardware Design Files

4.1 Schematics

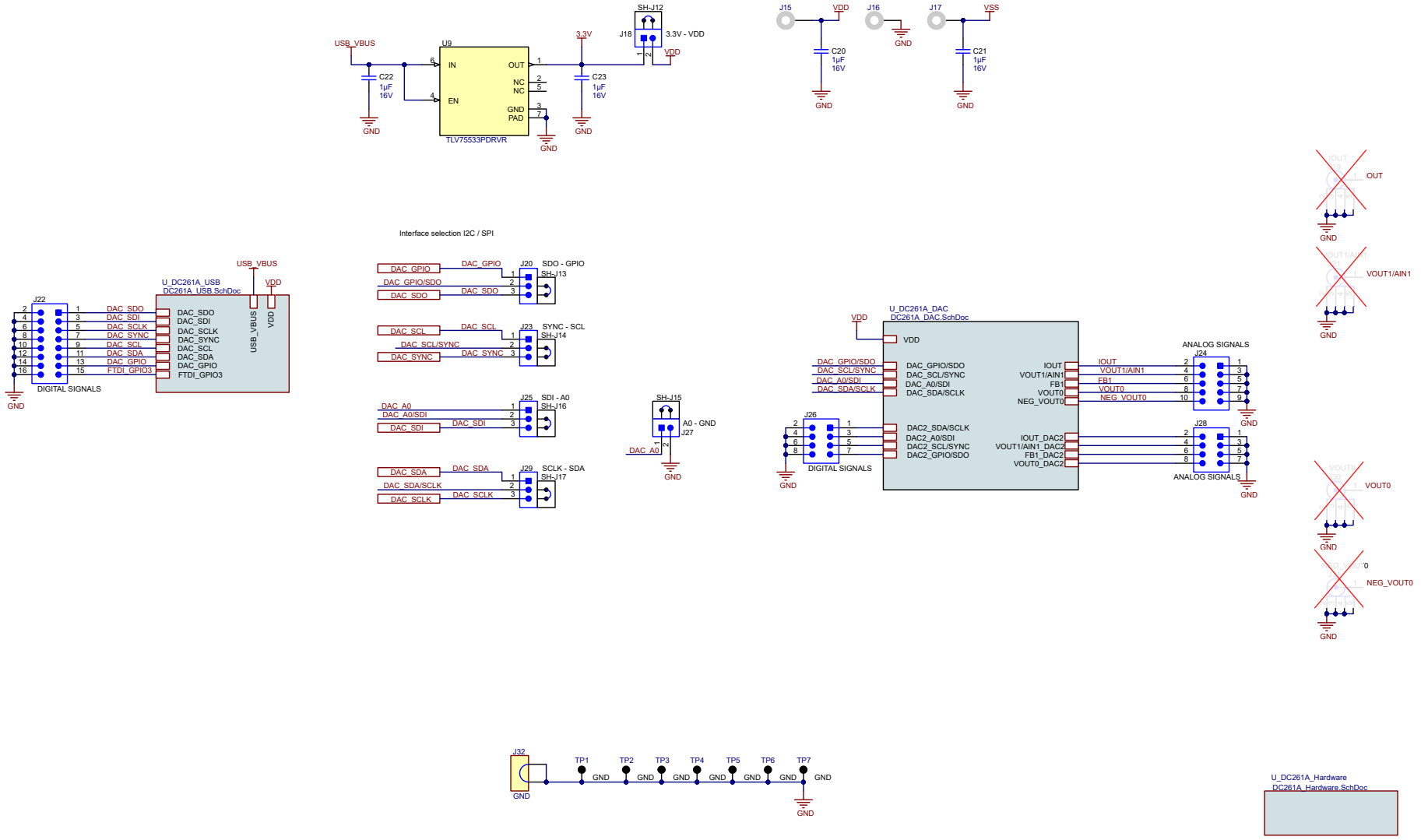


Figure 4-1. AFE532A3WEVM Schematic Page 1

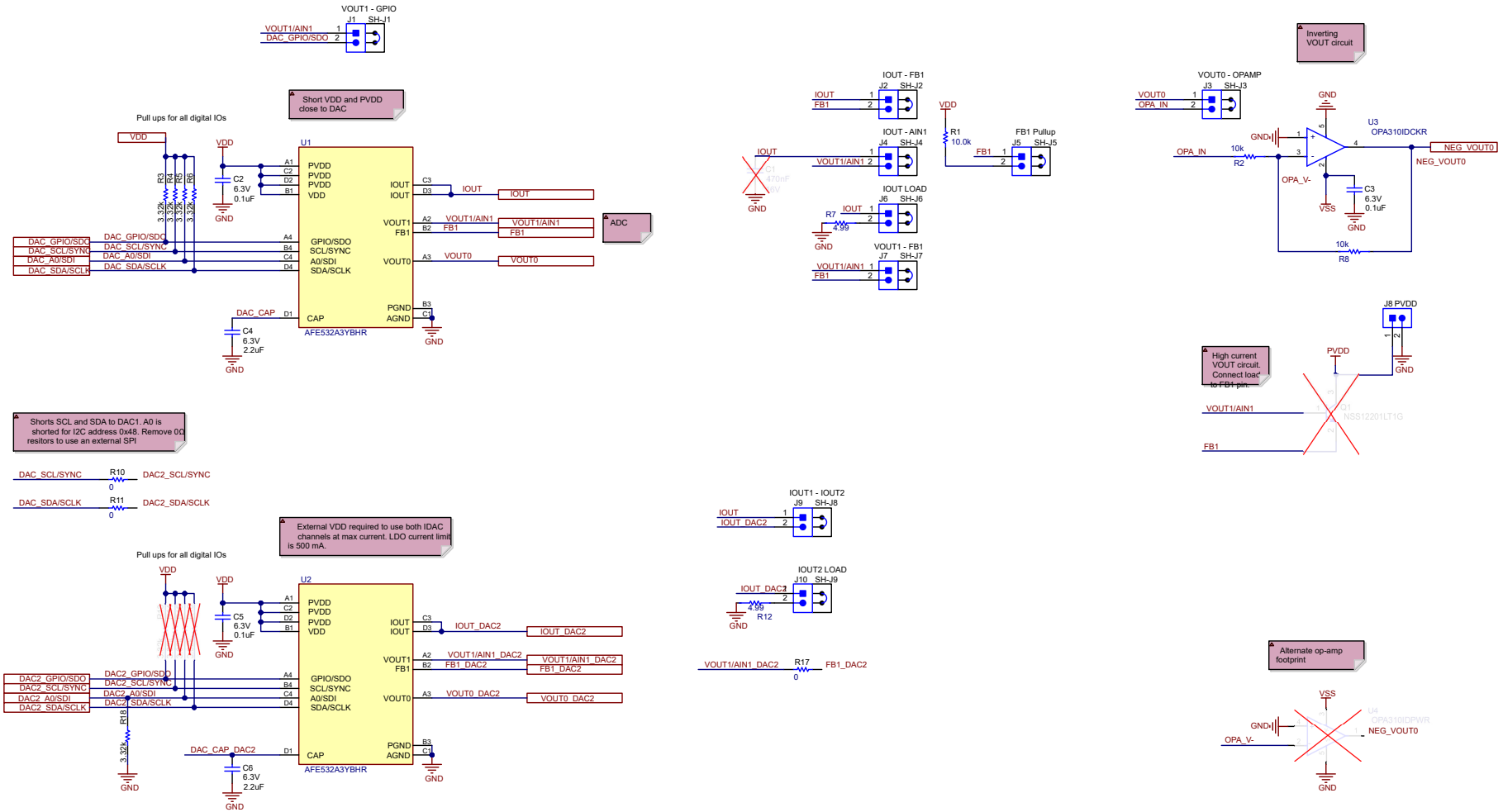


Figure 4-2. AFE532A3WEVM Schematic Page 2

4.2 PCB Layout

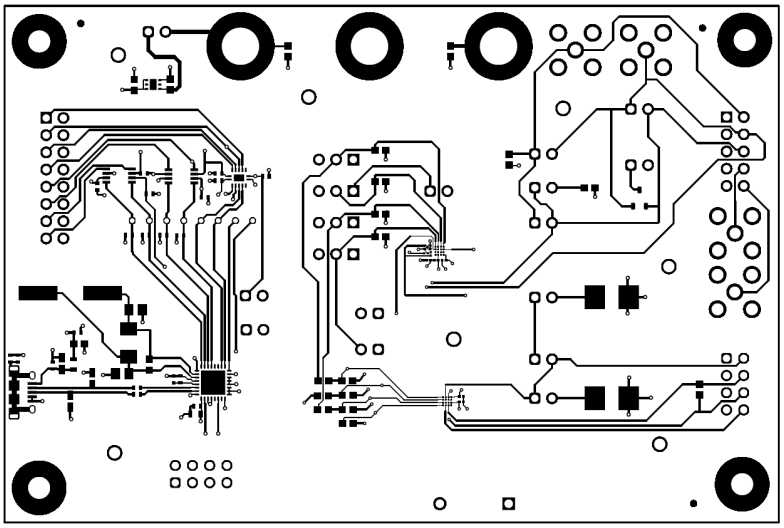


Figure 4-3. AFE532A3WEVM PCB Layer 1

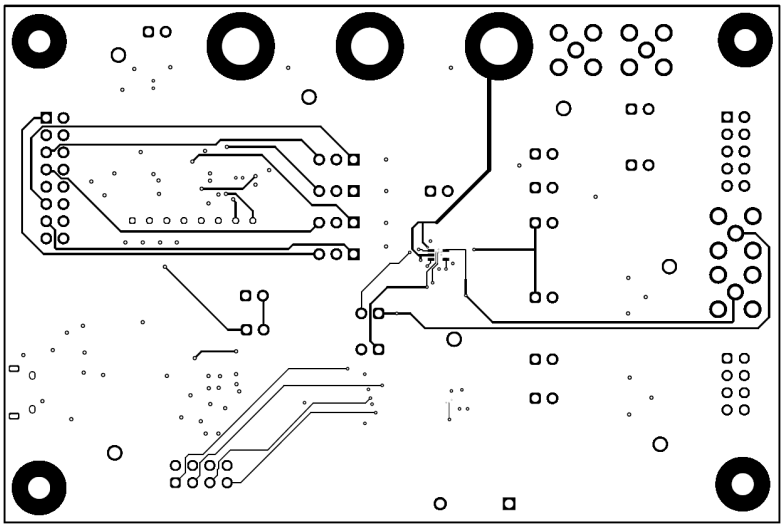


Figure 4-4. AFE532A3WEVM PCB Layer 2

4.3 Bill of Materials

Table 4-1. AFE532A3WEVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC261	Any
C2, C3, C5	3	0.1 µF	CAP, CERM, 0.1 µF, 6.3 V, +/- 10%, X5R, 0201	0201	GRM033R60J104KE19D	MuRata
C4, C6	2	2.2 µF	CAP, CERM, 2.2 µF, 6.3 V, +/- 20%, X5R, 0201	0201	CL03A225MQ3CRNC	Samsung Electro-Mechanics
C7, C8, C10, C12, C13, C14, C15, C17	8	0.1 µF	CAP, CERM, 0.1 µF, 25 V,+/- 10%, X7R, 0402	0402	CC0402KRX7R8BB104	Yageo
C9, C16	2	4.7 µF	CAP, CERM, 4.7 µF, 10 V, +/- 20%, X7R, 0603	0603	GRM188Z71A475ME15D	MuRata
C11	1	100 pF	CAP, CERM, 100 pF, 50 V, +/- 10%, X7R, 0402	0402	885012205055	Wurth Elektronik
C18, C19	2	18 pF	CAP, CERM, 18 pF, 50 V, +/- 5%, C0G/NP0, 0805	0805	08055A180JAT2A	AVX
C20, C21, C22, C23	4	1 µF	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603	0603	885012206052	Wurth Elektronik
D1, D2, D3	3	24 V	PulseGuard ESD Suppressor, 24VDC, SMT	0603 TVS Diode	PGB1010603MR	Littelfuse
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J12, J14, J18, J27	14		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J11	1		Receptacle, USB 2.0, Micro-USB Type B, R/A, SMT	USB-micro B USB 2.0, 0.65mm, 5 Pos, R/A, SMT	10118194-0001LF	FCI
J15, J16, J17	3		Standard Banana Jack, Uninsulated, 5.5mm	Keystone_575-4	575-4	Keystone
J20, J23, J25, J29	4		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
J22	1		Header, 100mil, 8x2, Gold, TH	PBC08DAAN	PBC08DAAN	Sullins Connector Solutions
J24	1		Header, 100mil, 5x2, Gold, TH	5x2 Header	TSW-105-07-G-D	Samtec
J26, J28	2		Header, 2.54mm, 4x2, Gold, TH	Header, 2.54mm, 4x2, TH	TSW-104-08-L-D	Samtec
J32	1			JUMPER2	D3082-05	Harwin
L1	1	600 Ω	Ferrite Bead, 600 ohm @ 100 MHz, 1 A, 0603	0603	782633601	Wurth Elektronik
R1	1	10.0 kΩ	RES, 10.0 kΩ, 1%, 0.1 W, 0603	0603	RCG060310K0FKEA	Vishay Draloric
R2, R8	2	10 kΩ	10 kΩ ±1% 0.05W, 1/20W Chip Resistor 0201 (0603 Metric) - Thick Film	0201	RMCF0201FT10K0	Stackpole
R3, R4, R5, R6, R18	5	3.32 kΩ	RES, 3.32 kΩ, 1%, 0.1 W, 0603	0603	RC0603FR-073K32L	Yageo

Table 4-1. AFE532A3WEVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R7, R12	2	4.99 Ω	4.99 Ω ±1% 2W Chip Resistor 2512 (6432 Metric) Moisture Resistant Thick Film	2512	RHC2512FT4R99	Stackpole Electronics Inc
R10, R11, R17	3	0 Ω	RES, 0 Ω, 0%, 0.25 W, AEC-Q200 Grade 0, 0603	0603	RCS06030000Z0EA	Vishay-Dale
R19, R26, R29	3	10.0 kΩ	RES, 10.0 kΩ, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT10K0	Stackpole Electronics Inc
R20	1	12 kΩ	12 kΩ ±1% 0.1W, 1/10W Chip Resistor 0402 (1005 Metric) Automotive AEC-Q200 Thick Film	0402	ERJ-2RKF1202X	Panasonic ECG
R21, R22	2	10 Ω	RES, 10.0 Ω, 1%, 0.063 W, 0402	0402	RK73H1ETTP10R0F	KOA Speer
R23	1	330 Ω	RES, 330 Ω, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF3300X	Panasonic
R24, R25, R27, R28	4	3.30 kΩ	RES, 3.30 kΩ, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RK73H1ETTP3301F	KOA Speer
R30	1	1.00 MΩ	RES, 1.00 MΩ, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M00FKEA	Vishay-Dale
TP1, TP2, TP3, TP4, TP5, TP6, TP7	7		Test Point, Compact, Black, TH	Black Compact Testpoint	5006	Keystone Electronics
U1, U2	2		AFE532A3YBHR	DSBGA16	AFE532A3YBHR	Texas Instruments
U3	1		Single, 5.5-V, 3-MHz high-output-current (150 mA) fast-shutdown (1 µs) operational amplifier 5-SC70 -40 to 125	SC70-5	OPA310IDCKR	Texas Instruments
U5	1		USB Bridge, USB to I²C/SPI USB 2.0 I²C, SPI 32-VQFN (5x5)	VQFN32	FT4222HQ-D-R	FTDI
U6	1		4-Bit Fixed Direction Voltage-Level Translator with Schmitt- Trigger Inputs, and Tri-State Outputs, WQFN14	WQFN14	TXU0304BQA	Texas Instruments
U7, U8	2		Voltage Level Translator Bidirectional 1 Circuit 2 Channel 24Mbps SM8	SSOP8	TCA9406DCTR	Texas Instruments
U9	1		500 mA LDO, DRV0006A (WSON-6)	DRV0006A	TLV75533PDRVR	Texas Instruments
Y1	1		Crystal, 12 MHz, 18 pF, SMD	ABM3	ABM3-12.000MHZ-B2-T	Abracon Corporation
C1	0	0.47 µF	CAP, CERM, 0.47 µF, 16 V, +/- 10%, X7R, 0603	0603	C0603C474K4RACTU	Kemet
J13	0		Header, 2.54mm, 8x1, Gold, TH	Header, 2.54mm, 8x1, TH	TS-108-G-AA	Samtec
J19, J21, J30, J31	0		SMA	SMA	142-0701-201	Cinch Connectivity
Q1	0	12 V	Transistor, NPN, 12 V, 2 A, SOT-23	SOT-23	NSS12201LT1G	ON Semiconductor
R13, R14, R15, R16	0	3.32 kΩ	RES, 3.32 kΩ, 1%, 0.1 W, 0603	0603	RC0603FR-073K32L	Yageo
U4	0		5-MHz, 15-V/µs High Slew-Rate, RRIO Op Amp	X2SON5	OPA310IDPWR	Texas Instruments

Table 4-1. AFE532A3WEVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
Y2	0		Crystal, 12 MHz, 30 ppm, 18 pF, SMD	11.4x4.7mm	ABLS2-12.000MHZ-D4Y-T	Abracon Corporation

5 Additional Information

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