Collin Wells, Ryan Andrews

TI Precision Designs: Verified Design

1% Error, 0-5 V Input, 0-500 mA Output, Low-Side Voltage-to-Current (V-I) Converter

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Design Resources

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TINA-TI™	SPICE Simulator
OPA735	Product Folder

Circuit Description

This low-side voltage-to-current (V-I) converter delivers a well-regulated current to a floating load. The design uses a small-signal op amp to control an NPN emitter-follower that sources current to the load. The current is accurately regulated by feeding back the voltage drop across a low-side current-sense resistor to the op amp.

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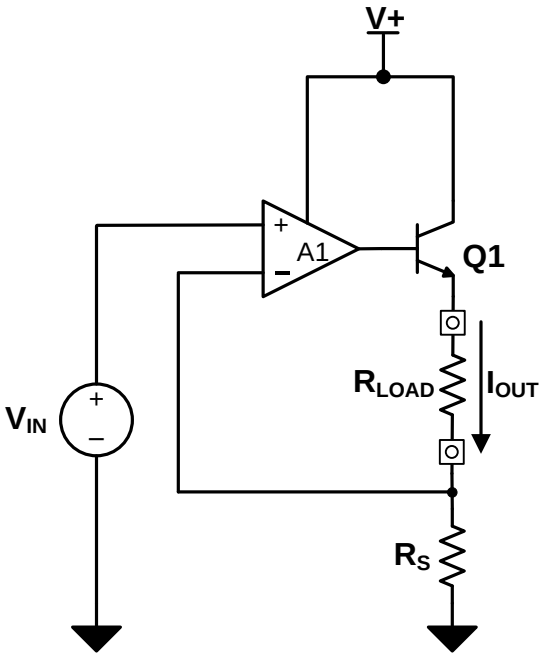

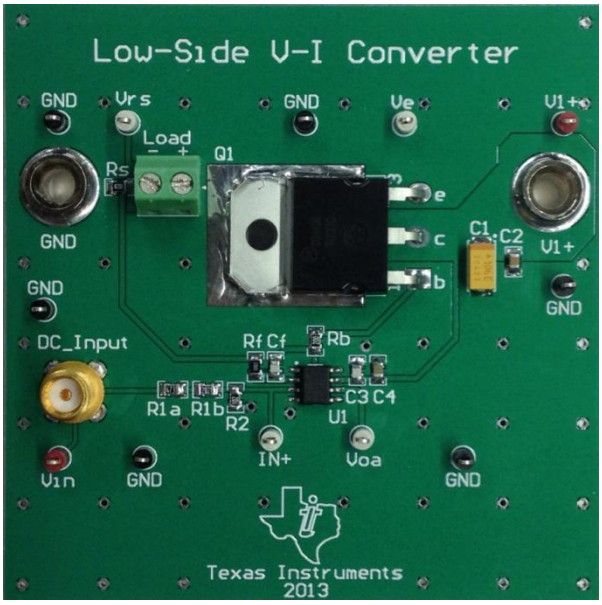

1 Design Summary

The design requirements are as follows:

- Supply Voltage: 12 V dc
- Input: 0-5 V dc
- Output: 0-500 mA dc

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulated, and Measured Performance

	Goals	Simulated	Measured
Offset (%FSR)	0.1	<0.001	<0.001
Gain Error (%FSR)	1	0.579	0.846
Load Compliance (V)	10	10.27	11.07

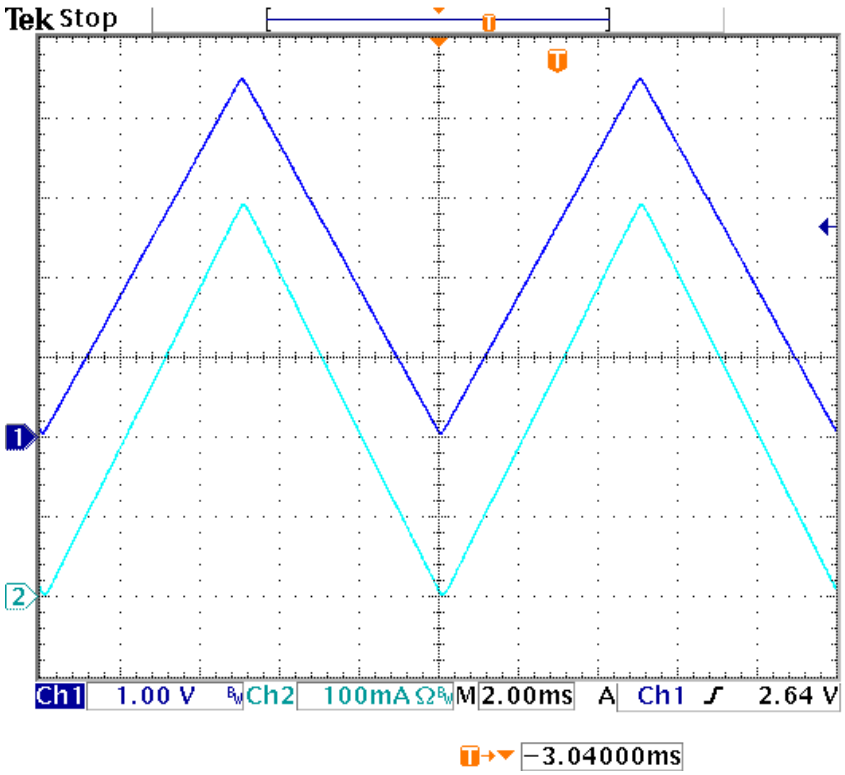

Figure 1: Measured Transfer Function

2 Theory of Operation

A more complete schematic for this design is shown in Figure 2. The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, the input resistor divider network, and the current sensing resistor, R_S.

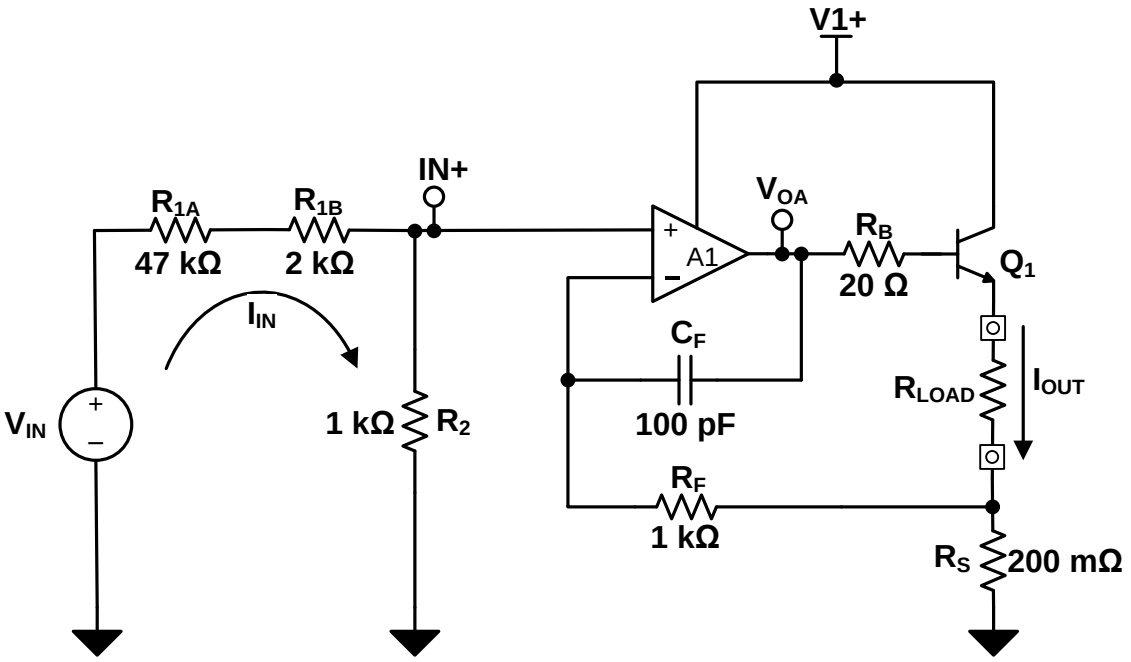

Figure 2: Complete Circuit Schematic

The transfer function for this design is defined in Equation 1.

$$\text{Gain} = \frac{I_{OUT}}{V_{IN}} = \frac{R_2}{R_S(R_1 + R_2)} \quad (1)$$

2.1 R_s

The sense resistor, R_S, is placed in series with the load and will develop a voltage drop proportional to the current through the load. This sense voltage is fed back into the inverting input of the op amp. Through negative feedback, the op amp will control the current that flows through the BJT such that it sets the voltage at the inverting node (IN-) equal to the voltage applied to the non-inverting node (IN+), achieving the V-I transfer function.

The voltage drop across R_S subtracts from the load compliance voltage and was limited to 100 mV at full-scale to maximize the load compliance voltage. Limiting the voltage drop to 100mV also limits the power dissipated in the sense resistor to 50 mW at full-scale output reducing self-heating effects.

$$R_S = \frac{100mV}{500mA} = 200m\Omega \quad (2)$$

2.2 R_1 and R_2

By limiting the maximum voltage at the inverting terminal to 100 mV at full-scale, the voltage at the non-inverting terminal is also limited to 100 mV. In order to use this circuit with a standard voltage input range of 0-5 V dc, a resistor divider is implemented between the input voltage and the non-inverting input. Resistor values were calculated to ensure that only 100 µA of current would be drawn from the input source at full-scale. Using standard resistor values may require the use of multiple resistors in series (i.e. R_{1A} and R_{1B}) to realize the calculated ratio below.

R_2 is sized based on the desired input current and input voltage at IN+:

$$IN+ = 100\,mV = 100\,uA \times R_2 \tag{3}$$

$$R_2 = 1\ k\Omega \tag{4}$$

R_1 is calculated such that the resistor divider produces 100 mV with a full-scale input of 5 V:

$$IN+ = V_{IN}\left(\frac{R_2}{R_1 + R_2}\right) \tag{5}$$

$$100\,mV = 5\,V\left(\frac{1k\Omega}{R_1 + 1k\Omega}\right) \tag{6}$$

$$R_1 = 49\,k\Omega \tag{7}$$

By setting the voltage across the sense resistor, V_{RS}, equal to the voltage applied to IN+, one can derive the transfer function for linear operation of the current source as shown in the equations below.

$$I_{OUT} = \left(\frac{V_{RS}}{R_S}\right) \tag{8}$$

$$Gain = \frac{I_{OUT}}{V_{IN}} = \frac{R_2}{R_S(R_1 + R_2)} \tag{9}$$

2.3 R_{1B}

The voltage drop across the base resistor, R_B will subtract from the maximum compliance voltage of this design. Therefore, R_B is sized such that it only subtracts 100 mV of headroom across the output stage at full-scale. For a transistor with a β of 100, the TIP33 is expected to pull approximately 5 mA of base current when I_{OUT} nears the full-scale current of 500 mA.

$$R_B = \frac{100\ mV}{5\ mA} = 20\,\Omega \tag{10}$$

2.4 R_F and C_F

The feedback components R_F and C_F provide compensation to this circuit to ensure stability during input or load transients. The compensation works by removing the BJT gain from the control loop at higher frequencies by providing feedback to the inverting input directly from the amplifier output through C_F instead of at the BJT emitter through R_F. The frequency that this occurs is roughly based on the RC time constant formed from R_F and C_F. The values in this circuit were chosen such that frequency is within the usable bandwidth of the amplifier, but above 100 kHz so the response wasn't too over-damped. The value of R_F should be sized much larger than the load resistance but not so large that the op amp input bias current flowing through it creates a large offset voltage.

The transient response of this circuit is examined in Section 6.4. Based on the small-signal response of the amplifier and load outputs, it is clear that the selected values for R_F and C_F provide adequate stability for a purely resistive load.

R_F and/or C_F can be increased to provide additional compensation in order to accommodate applications with inductive loads. As the RC time constant is increased, it is important to evaluate the step-response of the system as the circuit settling time will increase as well.

R_B also provides compensation to the circuit. The user should refrain from making R_B too large since it will limit the voltage headroom across the output stage. Consequently, this reduces the maximum full-scale load that the circuit can drive before reaching compliance (see Section 6.5 on Compliance Voltage). For a more detailed study on op amp stability please refer to Reference 1.

2.5 Summary

This circuit's operation is dependent on the appropriate sizing of R_S, R_1, R_2, and R_B. The output current that passes through R_S creates the voltage potential that is fed into the inverting input of the OPA735. The sense voltage is limited to 100 mV at full-scale in order to minimize power dissipation across R_S. This is accomplished by limiting the voltage at the non-inverting terminal to 100mV using a proper resistor divider to divide down the dc input voltage without drawing more than 100 µA from the source. R_B is kept small so as to reduce the voltage headroom lost across the output stage.

3 Component Selection

3.1 Operational Amplifier

For a successful design, one must pay careful attention to the DC characteristics of the op amp chosen for the application. To meet the performance goals, this application will benefit from an op amp with **low offset voltage, low temperature drift, and rail-to-rail output.**

The OPA735 CMOS operational amplifier is a high-precision device with 5 µV of offset and 0.05uV/C of drift and is optimized for single-supply operation with output swing to within 50mV of the positive rail.

Using auto-zeroing techniques, the OPA735 provides low initial offset voltage and near-zero drift over temperature. Low offset voltage and low drift will reduce the offset error in the system, making these devices appropriate for precise DC control. The rail-to-rail output stage of the OPA735 will allow for the full headroom across the load.

Other amplifier options for this application are the chopper-stabilized OPA188 or OPA333 as further discussed in Section 7.

3.2 NPN Transistor

The TIP33 NPN transistor chosen for this design is rated for a continuous collector current of 10A and a maximum collector-emitter voltage of 40V. Choosing a transistor that exceeds the requirements of the circuit will dissipate heat more effectively and allow for operation without an external heat-sink. The TIP33 has a rated base-emitter voltage of 1.6 V at 3 A and a small-signal gain (β) of 100.

3.3 Passive Component Selection

The critical passive components for this design are the resistors that are part of the transfer function: R_{1A} and R_{1B}, R_2, and R_S.

To meet the design requirements of 1% FSR gain error, the tolerance of these resistors must be selected appropriately. R_{1A}, R_{1B}, and R_2 were chosen with 0.1% tolerance as these parts were easier to obtain while keeping the design cost-effective. R_S was chosen to be 1% as the price for low-tolerance 200 mΩ resistors was significantly higher. Although the design performance will benefit from using the most precise components available, cost is a tradeoff that each designer must evaluate individually.

Other passive components in this design may be selected for 1% or greater because they will not directly affect the transfer function of this design.

4 Simulation

The TINA-TI™ schematic shown in Figure 3 includes the circuit values obtained in the design process.

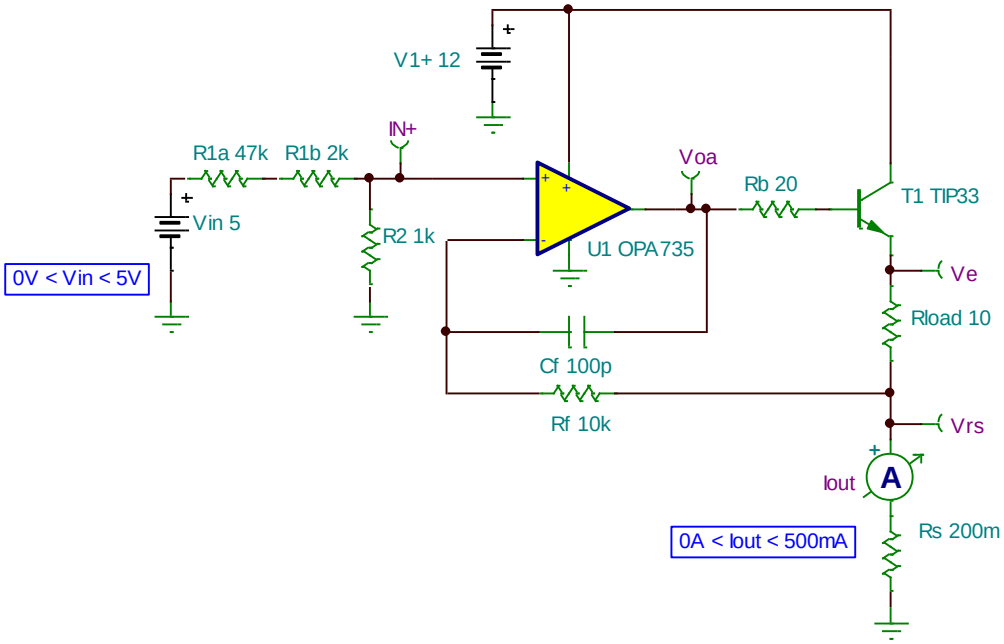

Figure 3: TINA-TI™ Simulation Schematic

4.1 DC Transfer Function

The dc transfer function results of the simulation are shown in Figure 4. The simulation results showed an offset current of -14.78 pA and a full-scale current of 499.94 mA. These results do not include the tolerance of the passive components and help analyze amplifier and active device accuracy.

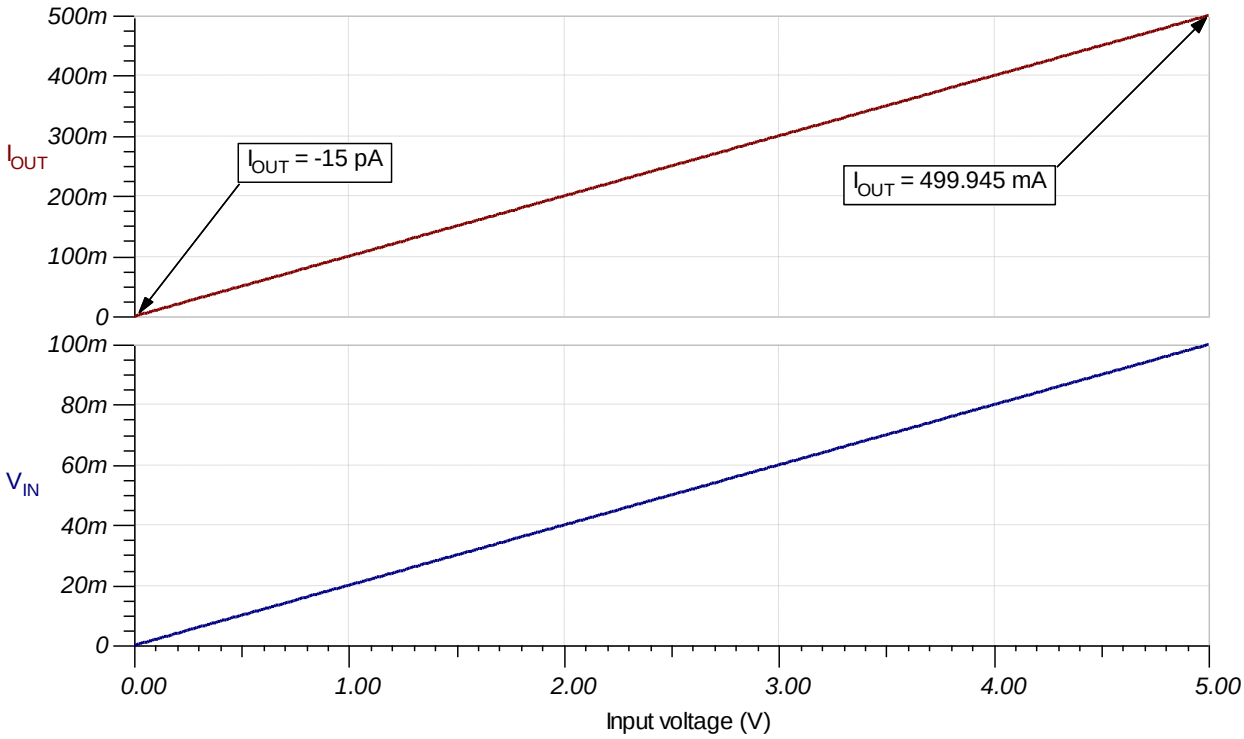

Figure 4: Simulated Full-Scale Transfer Function

A 20-sweep Monte-Carlo simulation was run with the actual component tolerances to produce more realistic results. The results are shown in Table 2 and Figure 5.

Table 2: Average Monte-Carlo DC Transfer Results

	Min	Max	Average	Std. Dev. (σ)
I_{OUT} Offset (pA)	-14.778	-14.762	-14.778	0.006
Full-Scale I_{OUT} (mA)	498.205	501.641	499.904	0.9654
Full-Scale I_{OUT} |Error| (mA)	0.0573	1.795	0.193	n/A

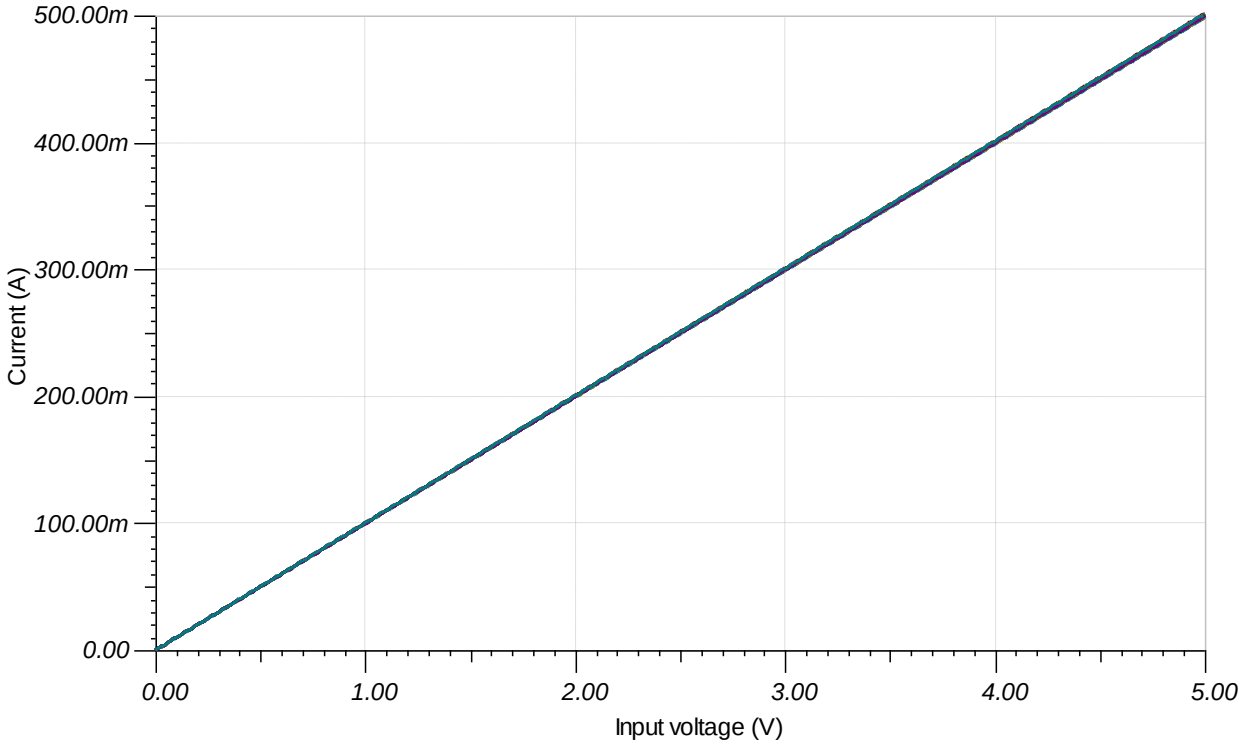

Figure 5: Simulated Monte-Carlo Full-Scale Transfer Function

The full-scale gain error was calculated using three standard deviations of the full-scale load current, which should encompass roughly 99.7% of the designs (3-σ).

$$\text{Gain Error}(\%) = \frac{3 \times \sigma}{\Delta I_{OUT}(\text{Ideal})} \times 100 = \left(\frac{2.896}{500} \right) \times 100 = 0.579\% \quad (11)$$

4.2 Step Response

The small-signal stability of the system was verified by applying a step response to the input of the op amp that caused the output to change by roughly 100 mV. The results are shown in Figure 6.

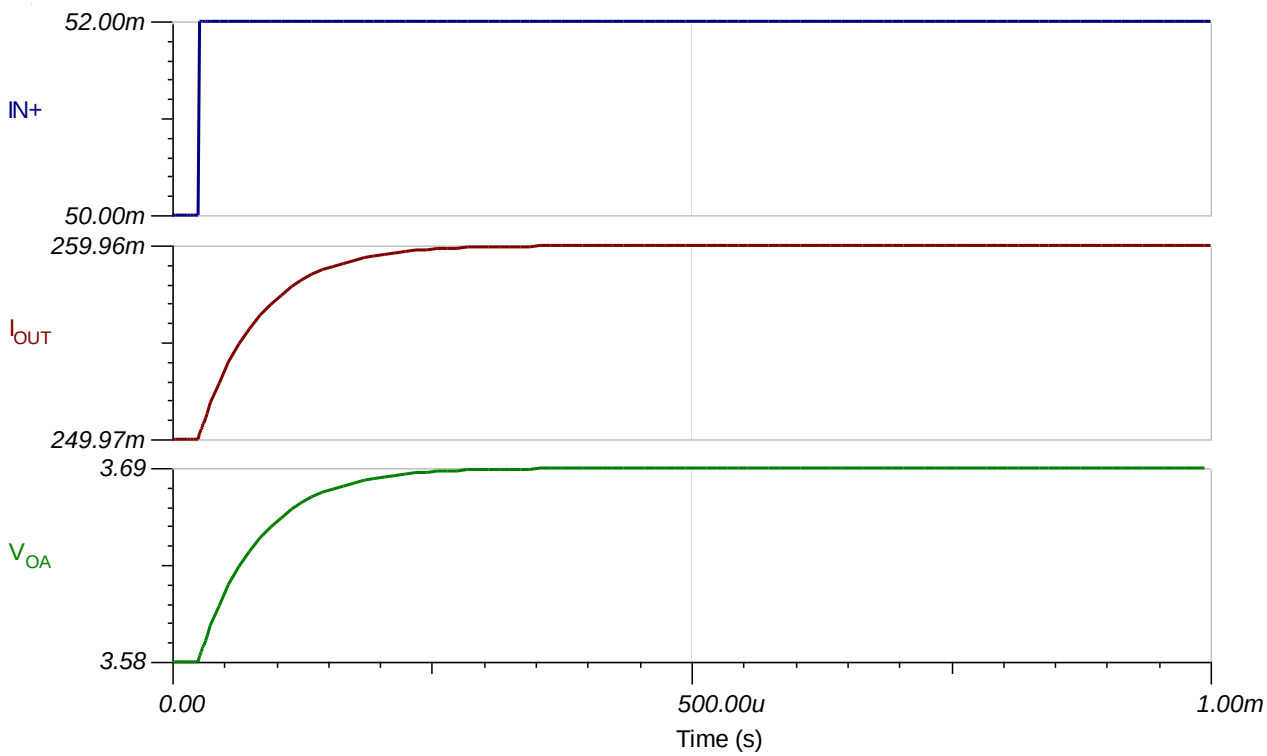

Figure 6: Small-Signal Step Response Simulation

4.3 Compliance Voltage

To test the maximum load compliance voltage and load resistance, the output was set to full-scale (500 mA) and the load resistor, R_{LOAD}, was swept from 0 Ω - 25 Ω. It was found that the output compliance voltage was 10.27 V and the maximum output resistance was 20.55 Ω.

Simulation also verifies that the V_{OA} of the amplifier is the limiting factor in compliance voltage as further discussed in Section 6.5.

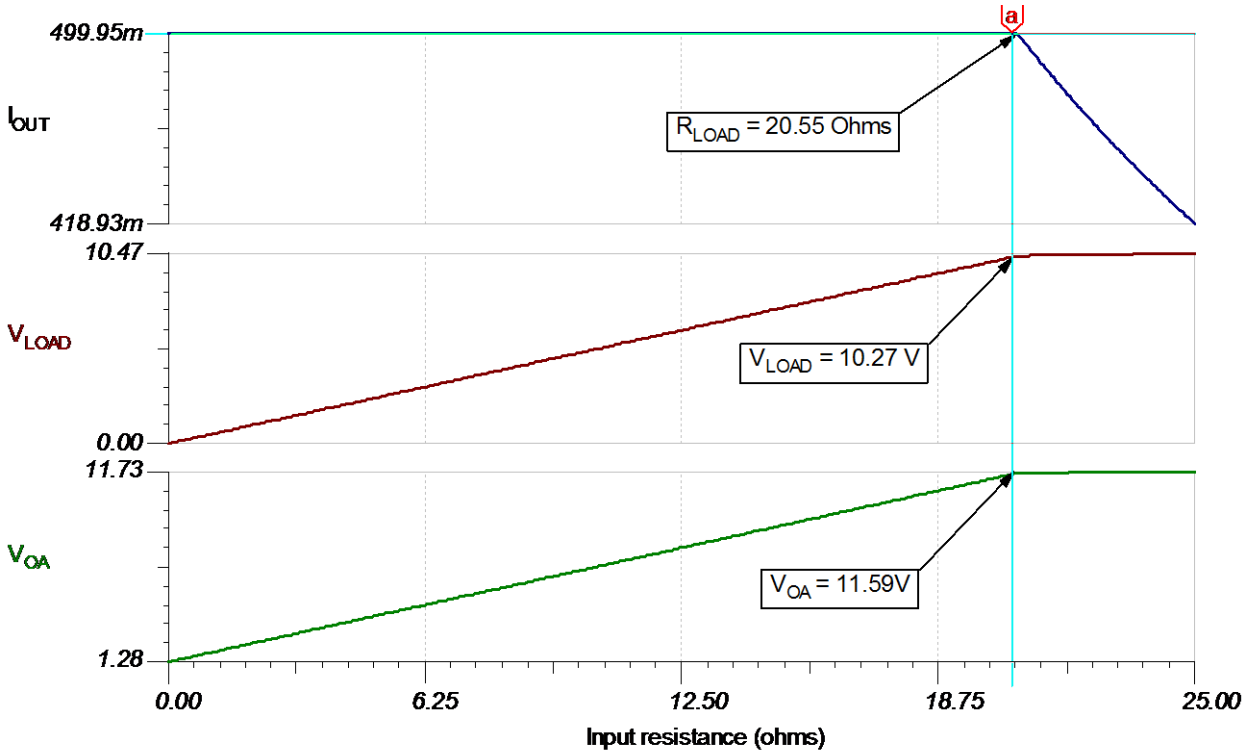

Figure 7: Maximum Load Impedance and Compliance Voltage Simulation

4.4 Simulated Result Summary

The simulation results are compared against the design goals in Table 3.

Table 3: Simulated Result Summary

	Goals	Simulated
I_{OUT} Offset (%FSR)	0.1	<0.0001
I_{OUT} Gain Error (%FSR)	1	0.386
Load Compliance (V	10	10.27

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.1 and 0.

5.1 PCB Layout

For optimal performance in this design, much importance is placed on the high-current path from V1+ to the GND through the transistor, load, and sense resistor.

Since the full-scale output current in this design is 500 mA and the full-scale sense voltage is only 100 mV, even small amounts of PCB resistance in series with the sense resistor will create error voltages that cause gain errors in the circuit transfer function. To avoid this situation, a 4-wire Kelvin connection is used to separate the high-current path through R_S from the path used to sense the voltage drop across it.

The high-current path through the BJT and the load is made with wide traces in order to reduce PCB trace resistance and facilitate current flow. Keeping the high-current traces wide near the NPN transistor will allow for the heat to dissipate away from the IC, lowering the device temperature. The layout for the design is shown in Figure 8.

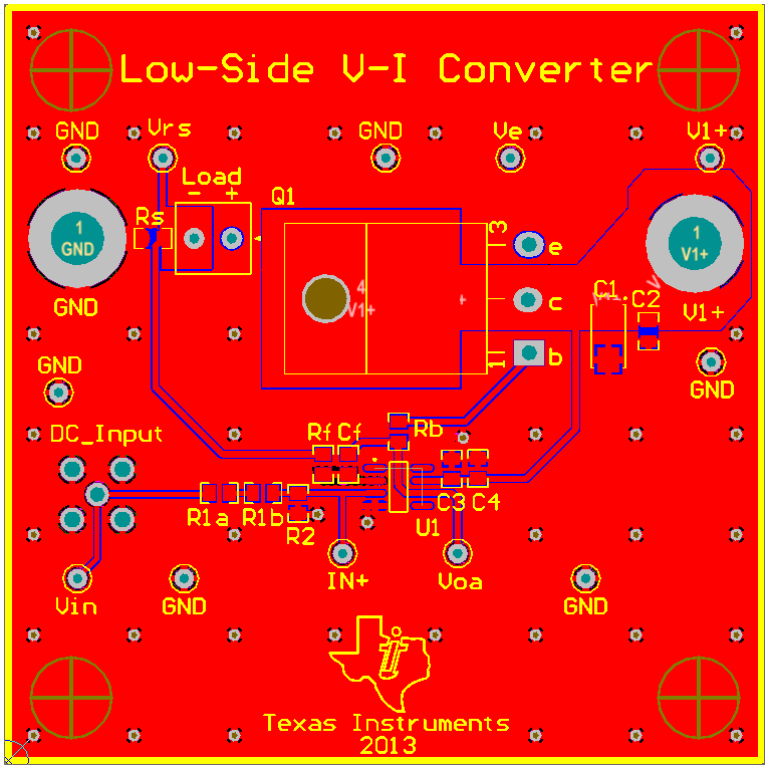

Figure 8: Altium PCB Layout

In addition to these rules, please reference and abide by general PCB layout guidelines.

6 Verification and Measured Performance

6.1 Transfer Function

Data was collected by sweeping V_{IN} from 0-5 V dc while measuring the output current, I_{OUT}. Figure 9 displays a plot of I_{OUT} versus V_{IN}.

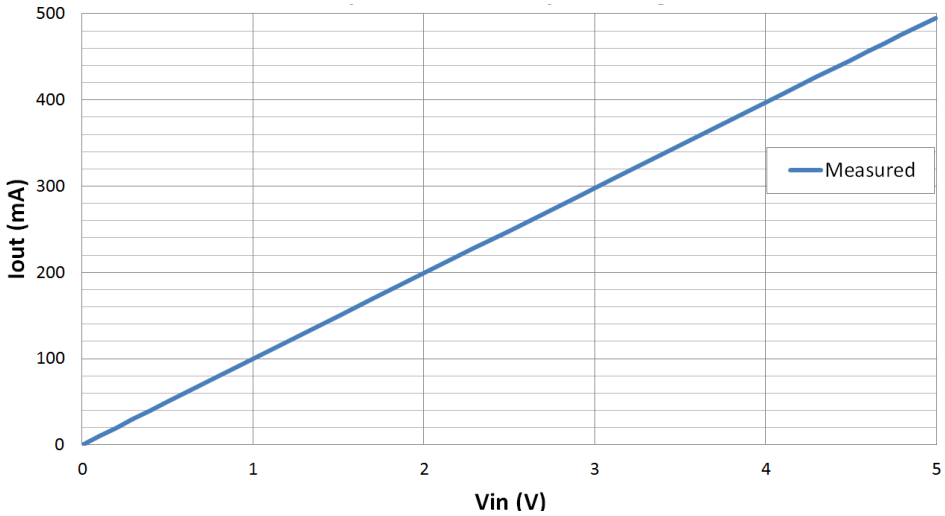

Figure 9: Measured I_{OUT} vs V_{IN}

6.2 Offset Error

Due to the input low offset voltage and rail-to-rail output of the OPA735, the offset error in this circuit is negligible. With V_{IN} at the zero-scale input of 0V, an offset error of only 12pA was observed.

6.3 Gain Error

To observe the errors in the transfer function more clearly, Figure 10 shows the full-scale percent error in I_{OUT} plotted as a function of V_{IN}. A slight 2nd order effect can be seen as the sense resistor began to heat up near the full-scale currents. This could be minimized by using a lower temperature coefficient (TC) sense resistor.

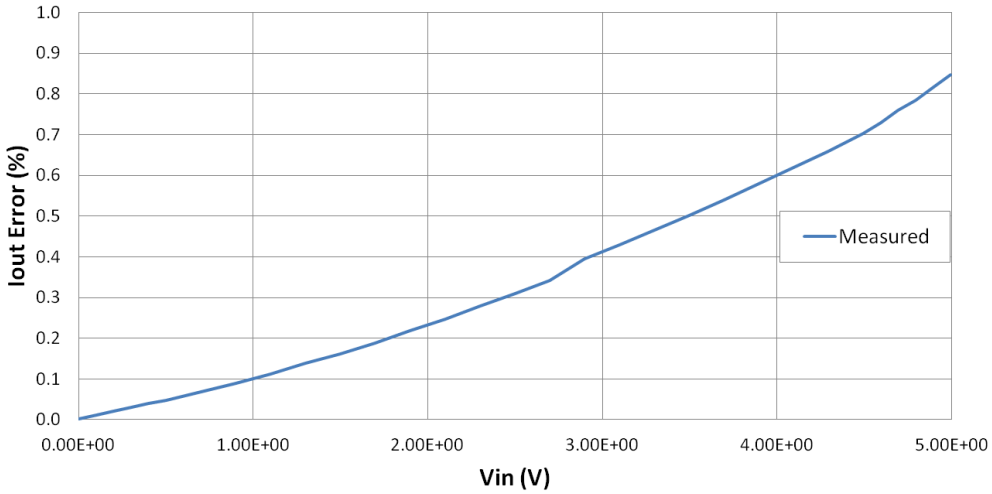

Figure 10: Measured I_{OUT} Error(%FSR) vs. V_{IN}

Although the desired output span was from 0-500 mA, the gain errors in the circuit limited the output to a maximum of 495.1 mA. The gain error was calculated over the operating range of the circuit as shown in Equation 12.

$$\text{Gain Error}(\%) = \frac{\Delta I_{OUT}(\text{Ideal}) - \Delta I_{OUT}(\text{Measured})}{\Delta I_{OUT}(\text{Ideal})} = -0.846\% \quad (12)$$

Resistor tolerances in the input resistor divider, the output sense resistor, and parasitic PCB resistances create gain errors in the circuit. The accuracy of this design is largely limited to the tolerance of the sense resistor, R_S. In this case, the R_S used in the design has a tolerance of 1%. Parasitic PCB resistances are likely the reason that the measured gain error was higher than the simulated gain error.

6.4 Transient Response

The operation of the design was verified over the full-scale input range. A 0-5 V triangle wave input was fed into the system at 100 Hz while measuring the output current with an ac/dc current probe. The results are shown in Figure 11.

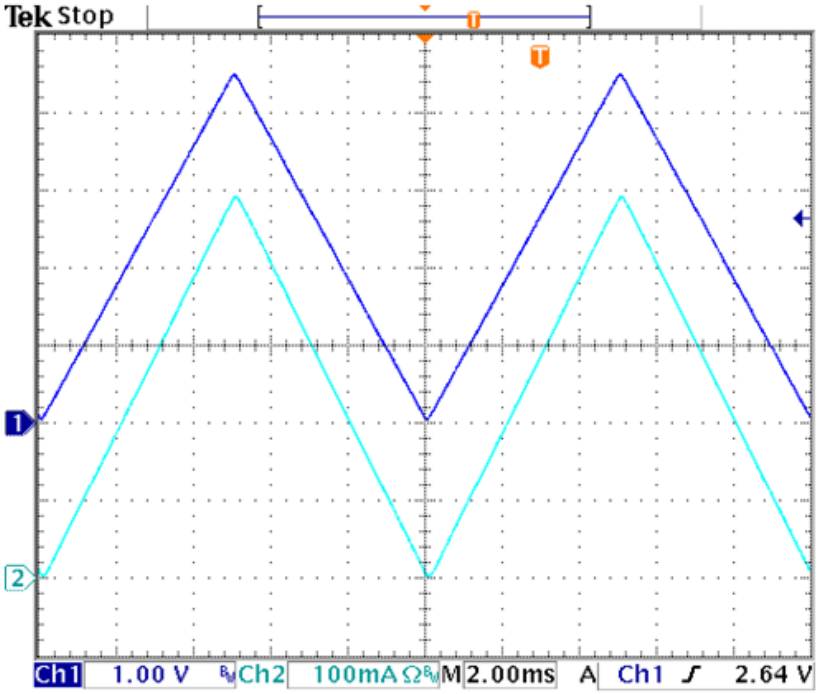

Figure 11: Measured I_{OUT} vs. Full-Scale V_{IN}

The large-signal settling time of the system was also tested to determine how quickly the output settles from a full-scale input transient. Figure 12 shows a 1 kHz, 0-5 V square wave input, which produced an output current through the load that settled in a little over 200µs.

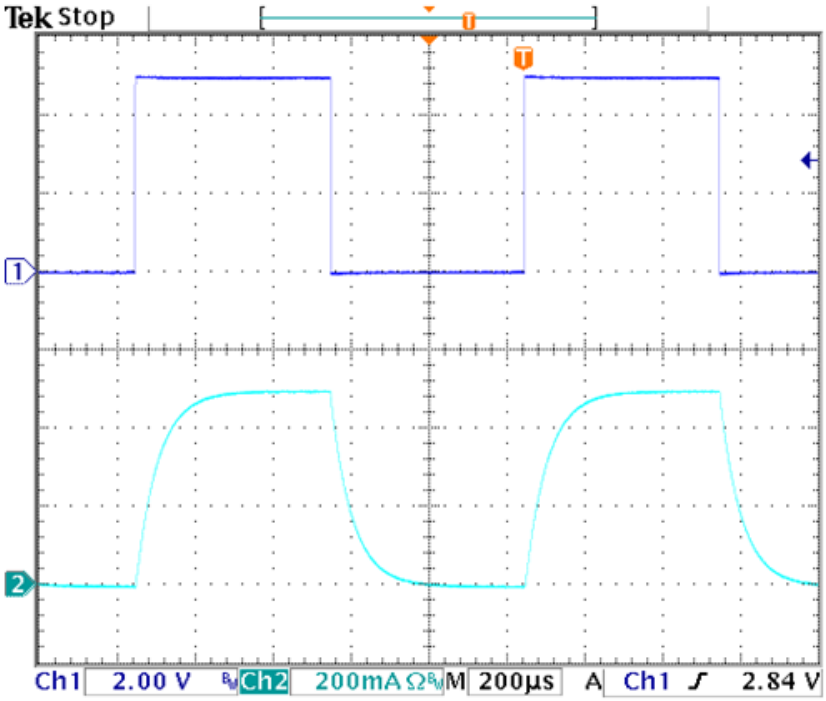

Figure 12: I_{OUT} Full-Scale Step Response

The small-signal response is indicative of the stability of the current source. An unstable design would present unwanted overshoot, ringing, and long settling times. This would require better compensation in the feedback network by adjusting R_B, R_F, and C_F.

In Figure 13, a 1 kHz, 200 mVpp square wave input was centered around mid-scale. This produced approximately 200 mVpp of change in the op amp's output and 20 mApp of change in output current through the load. As there was minimal overshoot and ringing, this circuit is considered largely over-damped and stable.

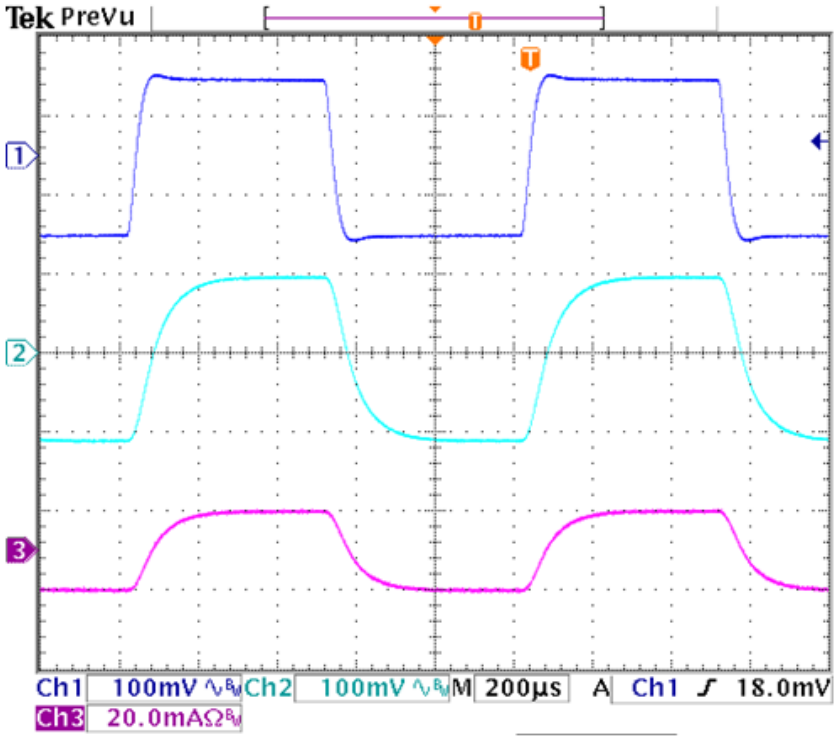

Figure 13: Small-Signal Step Response

6.5 Compliance Voltage

This current source will operate correctly as long as the voltage across the load resistance does not exceed the compliance voltage of the design. The maximum load impedance that this design can successfully drive is determined by analyzing the path from the op amp output to the emitter of the BJT, including the maximum output of the amplifier, the voltage drop across the sense resistor, and the base-emitter voltage ,V_{BE}, of the transistor at full-scale output.

The datasheet specifies that the output of the op amp, V_{OA}, has an output voltage swing within 50 mV of the positive rail at light loads. Therefore, the circuit should be designed under the assumption that V_{OA} cannot exceed 11.95 V. The voltage drop across the R_B resistor was designed to be 100 mV, and the V_{BE} of the BJT is 1.6 V. The maximum voltage that should be expected at the emitter of the BJT at full-scale output current can be calculated as shown in the following equations.

$$V_E(max) = V_{OA} - (V_B + V_{BE}) \tag{13}$$

$$V_E(max) = 11.95\,V - (100\,mV + 1.6\,V) = 10.25\,V \tag{14}$$

The emitter voltage V_E must remain less than 10.25 V in order for the op amp to output the appropriate output voltage at full-scale. This means that the maximum allowable load impedance can be calculated as shown in the following equation.

$$V_E = V_{LOAD} + V_{RS} = I_{OUT} \times (R_{LOAD} + R_S) \tag{15}$$

$$10.25\,V = 500\,mA \times (R_{LOAD} + 200\,m\Omega) \tag{16}$$

$$R_{LOAD} = 21.94\,\Omega \tag{17}$$

The increase in measured compliance voltage compared to the calculated values was due to better swing-to-rail performance from the OPA735 and a smaller BJT V_{BE} voltage of 0.75V.

Although it was not the case in this design, in some instances the saturation voltage of the BJT may be the limiting factor in the load compliance voltage.

6.6 Measured Result Summary

The measured results are compared against the design goals in Table 4.

Table 4: Measured Result Summary

	Goals	Measured
I_{OUT} Offset (%FSR)	0.1	<0.0001
I_{OUT} Gain Error (%FSR)	1	0.846
Load Compliance (V)	10	11.07

7 Modifications

Other amplifier options for this application are the chopper-stabilized OPA188 or OPA333. The OPA188 offers a wider supply voltage range of 36V for applications that may require larger current outputs or compliance voltages. For designs with supply voltages less than +5.5V, the OPA333 offers unmatched offset, drift, and quiescent current performance. Other amplifiers provide lower quiescent current or higher bandwidths. Table 5 provides a few options with key specifications for this design.

If this design is to be used over a wide temperature range, it is also recommended to select low TC devices in addition to low tolerances for the critical components. This design will produce significant amounts of heat when operating near the full-scale output current. Devices with low TC will tend to fluctuate less over changes in temperature and provide more consistent results.

For higher current designs that require high accuracy, consider using a 4-lead Kelvin connected sense resistor for R_S that will help further minimize errors due to PCB parasitic resistance. Care should be taken to ensure that the BJT and other components in the design are not overstressed in modifying the design for higher voltages or larger output currents.

Table 5: Alternate Op Amps

Amplifier	Max Supply Voltage (V)	Max Offset Voltage (uV)	Max Offset Drift (uV/°C)	Bandwidth (MHz)	Quiescent Current (uA)
OPA333	5.5	5	0.05	0.35	25
OPA335	5.5	5	0.05	2	350
OPA320	5.5	150	5	20	1750
OPA188	36	25	0.085	2	475
OPA277	36	20	0.15	1	825

8 Potential Application

Using the OPA735 in low-side V-I converter configuration rewards the user with the ability to provide an accurately controlled, linear current source with minimal transfer error. An example application for this topology is precise LED current control as shown in Figure 14.

Depending on the available power supply and the amount of headroom across the output stage, one could easily string multiple LEDs in series between the emitter of the transistor and the sense resistor, R_S. Adjusting the current flow through the LEDs directly controls their brightness level. The input and output stages of the circuit can be reconfigured within the limitations of the OPA735 to accommodate other input voltage and output current ranges to fit your specific design requirements.

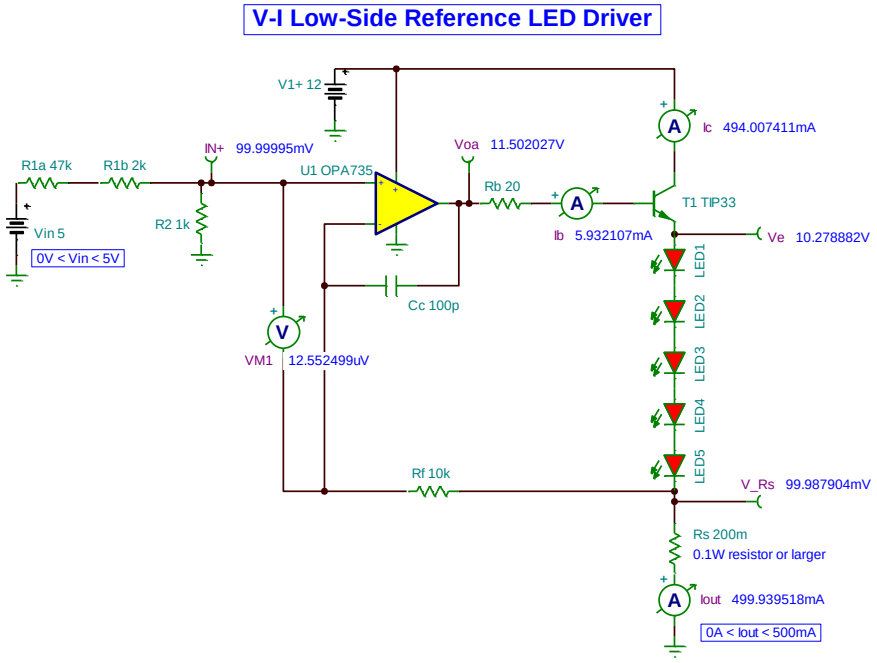

Figure 14: LED Driver Application Circuit

9 About the Authors

Ryan Andrews graduated from the University of Rhode Island in August 2011, where he earned a B.S. in Biomedical Engineering and a B.A. in Spanish. He joined Texas Instruments in February 2012 through the Applications Rotation Program, working with the Analog Centralized Applications and the Precision Analog – Linear teams. In March 2013, Ryan joined the Precision Analog – Delta-Sigma team in Dallas.

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

10 Acknowledgements & References

1. *Green, Tim, Operational Amplifier Stability Parts 1-11, November 2008, Available: http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_050712*

2. *R. Mark Stitt, Implementation and Applications of Current Sources and Current Receivers, Available: www.ti.com/lit/an/sboa046/sboa046.pdf*

Appendix A.

A.1 Electrical Schematic

The Altium electrical schematic for this design can be seen in Figure 15.

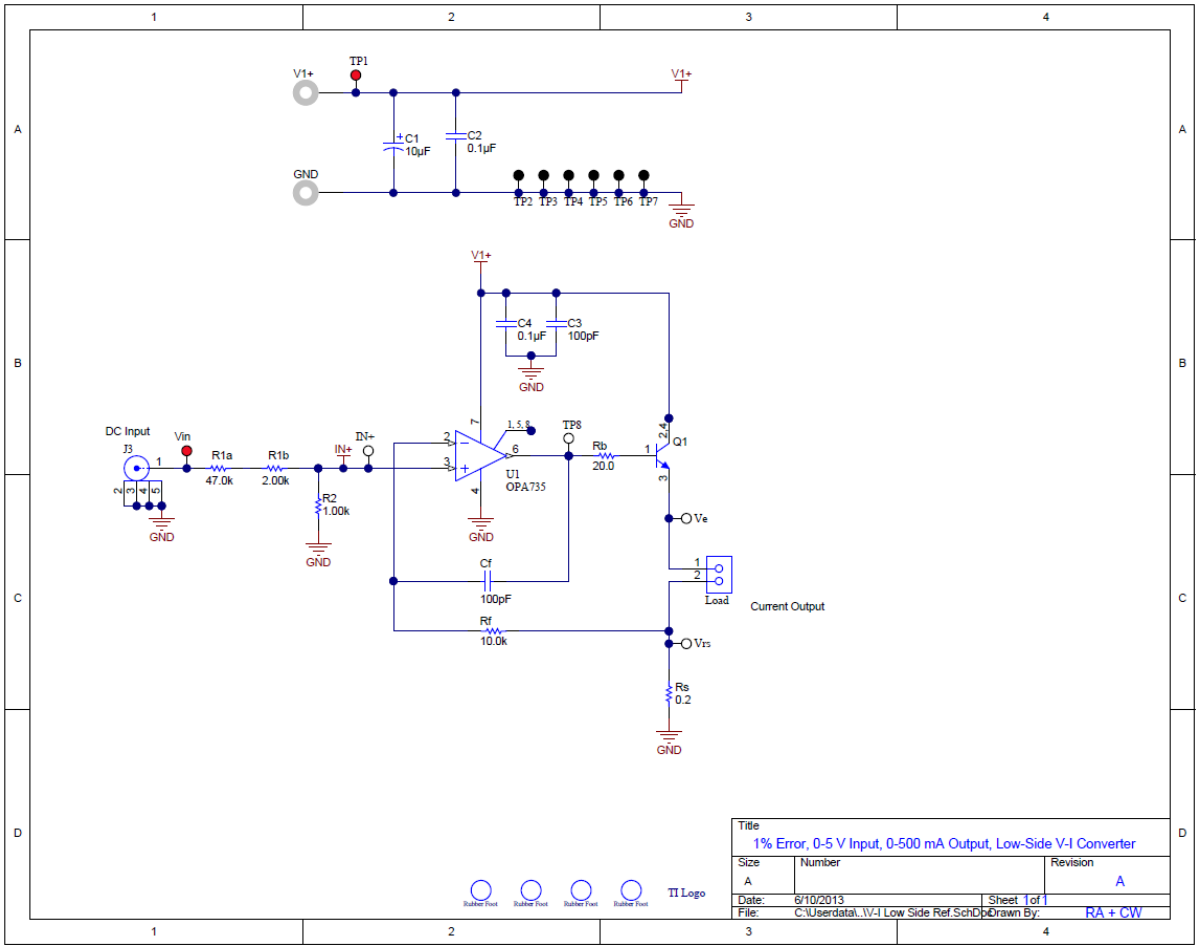

Figure 15: Altium Schematic

A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure 16.

Line #	Quantity	Value	Designator	Description	Manufacturer	PartNumber	Supplier Part Number 1
1	1	10uF	C1	CAP, TANT, 10uF, 25V, +/-10%, 0.3 ohm, 6032-28 SMD	AVX	TPSC106K025R0300	478-3360-1-ND
2	1	0.1uF	C2	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0805	MuRata	GRM21BR71E104KA01L	490-1673-1-ND
3	2	100pF	C3, C5	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0805	Kemet	C0805C101J5GACTU	399-1122-1-ND
4	1	0.1uF	C4	CAP, CERM, 0.1uF, 50V, +/-5%, X7R, 0805	AVX	08055C104JAT2A	478-3352-1-ND
5	1		J1	Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4	575-4K-ND
6	1		J2	Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4	575-4K-ND
7	1		J3	Connector, TH, SMA	Emerson Network Power	142-0701-201	J500-ND
8	1		J4	Conn Term Block, 2POS, 3.81mm PCB	Phoenix Contact	1727010	277-1947-ND
9	1		Q1	TRANS NPN 10A 100V HI PWR TO218	ON Semiconductor	TIP33CGOS-ND	TIP33CG
10	1	20R	R1	RES, 20.0 ohm, 0.5%, 0.1W, 0805	Susumu Co Ltd	RR1220Q-200-D	RR12Q20DCT-ND
11	1	47.0k	R2	RES, 47.0k ohm, 0.1%, 0.125W, 0805	Susumu Co Ltd	RG2012P-473-B-T5	RG20P47KBCT-ND
12	1	2.00k	R3	RES, 2.00k ohm, 0.1%, 0.125W, 0805	Susumu Co Ltd	RG2012P-202-B-T5	RG20P2.0KBCT-ND
13	1	1.00k	R4	RES, 1.00k ohm, 0.1%, 0.125W, 0805	Susumu Co Ltd	RG2012P-102-B-T5	RG20P1.0KBCT-ND
14	1	10.0k	R5	RES, 10.0k ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW080510K0FKEA	541-10.0KCCT-ND
15	1	0.2	R6	RES 0.2 OHM 1/4W 1% 0805 SMD	Stackpole	CSR0805FKR200	CSR0805FKR200CT-ND
16	2	Red	TP1, TP9	Test Point, TH, Miniature, Red	Keystone	5000	5000K-ND
17	6	Black	TP2, TP3, TP4, TP5, TP6, TP7	Test Point, TH, Miniature, Black	Keystone	5001	5001K-ND
18	4	White	TP8, TP10, TP11, TP12	Test Point, TH, Miniature, White	Keystone	5002	5002K-ND
19	1		U1	IC OPAMP CHOP R-R 1.6MHZ 8SOIC	Texas Instruments	OPA735AID	296-17995-ND

Figure 16: Bill of Materials

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