DAC8803/14 EVM

This user's guide describes the characteristics, operation, and use of the DAC8803/14 EVM – a multi-device, 14- to 16-bit, SSI, analog-to-digital converter evaluation module. A complete circuit description as well as schematic diagram and bill of materials are included.

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1 EVM Overview

1.1 Features

- Evaluation board for the 14-/16-bit current output, multiplying quad DAC8803 or DAC8814
- On-board ±10-V reference and buffer circuits
- High-speed serial interface
- Modular design for use with a variety of DSP and microcontroller interface boards

1.2 Introduction

The DAC8803/14 is a quad, 16-bit, serial input, current output DAC operating from a single 5-V power supply. This converter provides excellent linearity (±1 LSB INL), low glitch, low noise, and fast settling (0.3 µs typ. to ±0.1% of full-scale output) over the specified temperature range of –40°C to 85°C. Four external buffer and DPDT switches are provided on the EVM to allow unipolar and bipolar output operation.

The modular EVM form factor allows for direct evaluation of the DAC performance and operating characteristics. This EVM is compatible with the 5-6K Interface (SLAU104) and HPA-MCU Interface (SLAU106) Boards from Texas Instruments and additional 3rd party boards such as the HPA449 demonstration board from SoftBaugh, Inc. (www.softbaugh.com) and the Speedy33™ from Hyperception, Inc. (www.hyperception.com).

Speedy33 is a trademark of Hyperception, Inc.

2 Analog Interface

For maximum flexibility, the DAC8803/14 EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient ten pin dual row header/socket combination at J1. This header/socket provides access to the analog output pins of the DAC through the on-board buffer amplifiers. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Pin Number	Signal	Description
J1.2	Vout DACd	Controlled by W2; DACd output – range depends on the position of SW4 and W8
J1.4	Vout DACd	
J1.6	Vout DACa	Controlled by W4; DACa output – range depends on the position of SW3 and W7
J1.8	Vout DACa	
J1.10	Vout DACb	Controlled by W1; DACb output – range depends on the position of SW2 and W6
J1.12	Vout DACb	
J1.14	Vout DACc	Controlled by W3; DACc output – range depends on the position of SW1 and W5
J1.16	Vout DACc	
J1.18	REF(–)	Unused
J1.20	Ext. Ref.	External reference voltage input; selected with shunt on W10, pins 2-3
J1.15	Unused	
J1.1–J1.19 (odd)	AGND	Analog ground connections (except J1.15)

2.1 EVM Output Voltage

Switches SW1 through SW4 provide a means to allow unipolar or bipolar output operation of the DAC8803/14 EVM. When the slide switch is to the right, the output voltage on J1.x is ±VREF. With the 10-V on-board reference, this means the output voltage is –10 VDC to +10 VDC. When the switch is to the left, the output from the buffer is 0 V to +10 VDC or 0 V to –10 VDC depending on the position of the associated reference jumper. In the factory default condition, a –10-V reference, derived from the combination of U1 and U5, is applied to all four DACs via jumpers W5 through W8 and the output voltage is 0 V to –10 V. A +10-V reference voltage, derived through U1 and U6 (W5 through W8 with shunt to the left) produces a negative output voltage.

For a wider dynamic output range, the EVM can be configured to use an external reference in one of two ways. The user can remove the shunts at W5 through W8 and apply a reference source to the center pin associated with a specific DAC reference input. In this case, an external reference of up to ±10 V may be applied to the associated jumper.

An alternate method is to apply an external reference to J1 pin 20. This allows the on-board buffer (U6) to drive all four DAC reference inputs simultaneously when the shunt on W10 covers pins 2-3. J1 pin 20 can accept bipolar inputs. Keep in mind that the external reference must be supplied by a clean source for best performance.

3 Digital Interface

The DAC8803/14 EVM is designed for easy interfacing to multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient ten-pin dual row header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the DAC8803/14 EVM. Consult Samtec at www.samtec.com or 1-800-SAMTEC-9 for a variety of mating connector options.

Pin Number	Signal	Description
J2.1	MSB	MSB Bit set during a reset pulse (RS) or at system power on if tied to ground or VDD – GPIO input.
J2.3	SCLK	Serial clock input
J2.5	Unused	
J2.7	$\overline{CS}$	Chip select to the DAC. Tied to the frame sync for DSP host systems and STE for SPI host systems.
J2.9	Unused	
J2.11 - B	SDI	Serial data input to the primary DAC. J2-B is located on the bottom side of the PWB.
J2.11 - T	SDO	Serial data output to the secondary DAC. J2-T is located on the bottom side of the PWB and facilitates daisy chain operation.
J2.13	Unused	
J2.15	Unused	
J2.17	$\overline{LDAC}$	Load DAC – Active low signal, enables DAC output updates – jumper configurable (see schematic). When $\overline{LDAC}$ is low, the DAC latch is simultaneously updated with the content of the input register. Can be controlled by GPIO or tied low via W2.
J2.19	$\overline{RS}$	Reset pin, active low. Input register and DAC registers are set to all zeros or half-scale code (8000h) determined by the voltage on the MSB pin. Register data = 8000h when MSB = 1.

4 Power Supplies

The DAC8803/14 EVM board requires ±12 V and +5 VDC for the analog section. The ±12-V supplies power the reference (U1), it's buffer op-amp (U6), and the inverting reference buffer (U5). The output buffers (U2 and U3) also use the dual ±12-V supplies. The +5VA or +5VD input supplies the main DAC device (U4). Power to the main DAC device is selected by the shunt jumper at W9. By default, the +5VD supply is is used to power the device (shunt covers pins 1-2); +5VA can be used when the shunt is installed on pins 2-3. Supply current to the DAC can be monitored by placing a current meter across the appropriate pins of W9.

Table 1 shows the pinout of J3.

Table 1. Pinout of J3

Signal	Pin Number		Signal
+12V to +15V	1	2	–12V to –15V
+5VA	3	4	–5VA
DGND	5	6	AGND
Unused	7	8	Unused
Unused	9	10	+5VD

4.1 Stand-Alone Operation

When used as a stand-alone EVM, the analog power can be applied to J3 pins 1, 2, and 10, referenced to J3 pin 6. Optimal performance of the EVM requires a clean, well-regulated power source.

Control signals may be applied to J2 as described in section 3 and the device data sheet. J2-B pin 11, located on the bottom side of the PWB, applies the input serial data to the DAC. SDO from the main device is located on J2-T (top side connector) pin 11, allowing the possibility to stack two EVMs together in order to achieve daisy chain mode of operation. The signal found on J2-T pin 11 is the serial data input to J2-B pin 11 with a sixteen clock cycle delay.

4.2 Reference Voltage

The DAC8803/14 can be configured to use the on-board reference/buffer circuits (U1, U5 and U6) or an external reference applied to pin 20 of J1. Jumpers W5 through W8 control the on-board reference source. In the factory default position (shunt on W5 through W8 and W10 pins 1-2), a –10-V reference is supplied by U5. Moving the shunts at W5 through W8 to pins 2-3 applies the on-board +10-V reference to the DAC.

Jumper W10 must be configured so that it's associated shunt is located on pins 2-3 in order to use a common external reference voltage. An external reference source is buffered by U6 and requires W5 through W8 to have their shunts covering pins 2-3. When using an external reference, be sure to use a clean source that is within the data sheet specifications.

5 EVM Operation

5.1 Analog Output

The analog output is applied directly to J1 (top and bottom side). It can be further applied to optional amplifier and signal conditioning modules when used in conjuction with compatible interface boards, such as the HPA-MCU Interface (SLAU106). The analog output range is dependent on the configuration of the EVM and the reference applied to the DAC installed on the board. Consult section 4.2 of this users guide and the DAC8803/14 data sheet to determine the maximum analog output range.

5.2 Digital Control

The digital control signals can be applied directly to J2 (top or bottom side). The DAC8803/14 EVM can also be connected directly to a DSP or microcontroller interface board such as the 5-6K Interface Board or the HPA-MCU Interface Board. Refer to the product folder for the DAC8803/14 for a current list of compatible interface and/or accessory boards.

5.3 Load DAC ($\overline{LDAC}$)

The $\overline{LDAC}$ signal is found on J2.17. When used with one of the interface boards mentioned above, this signal is typically controlled through a timer function or GPIO. $\overline{LDAC}$ may be held low if desired by placing a shunt jumper across J2 pins 17 and 18.

5.4 Daisy Chain Mode

Up to two DAC8803/14 EVMs can be used together in order to facilitate the daisy chain mode of operation. The top and bottom side connectors of J2 have signal configurations that allow a second EVM to be mounted in a stacked arrangement. The data out of J2.11 on the top side is delayed by 16 clock cycles. When using daisy chain mode of operation, it is important to remember that data only shifts through the device while $\overline{CS}$ is held low. Jumpers W1 through W4 allow the outputs of the individual DACs in the stack to have their own output voltage pin. Refer to the schematic and section 4 for details.

5.5 Default Jumper Locations

The following table provides a list of the jumpers and switches located on the EVM and their factory default conditions.

Jumper	Shunt Position	Jumper Description
W1 - W4	1-2	Control which pin on J1 receives the DAC output voltage. Allows up to eight outputs (total) when using daisy chain features and two EVMs.
W5 - W8	1-2	Control the application of +10V or –10V to the reference pin of DACa through DACd. –10V is the default.
W9	1-2	Selects +5VD as the voltage source for DAC power. Voltage source should be applied to J3, pin 10.
W10	1-2	Selects the on-board reference voltage via U1 and U6. External reference is buffered by U6 when W10 is shunted pins 2-3.

6 EVM BOM, Layout and Schematic

6.1 Bill of Materials

The following table contains a complete bill of materials for the modular DAC8803/14 EVM. Layout information and a schematic diagram are also provided for reference.

Table 2. Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C1 C7 C9 C13	4.7 µF, 0805, Ceramic, Y5V, 16V	TDK	C2012Y5V1C475Z
C6	1 µF, EIA 3216, Tantalum, 20V	AVX	TAJA105K020R
C8 C10 C11 C12 C14 C16 C18 C19 C20	0.1 µF, 0603, Ceramic, X7R, 25V, 10%	TDK	C1608X7R1E104K
C17	0.01 µF, 0603, Ceramic, X7R, 50V, 10%	TDK	C1608X7R1H103K
J1 J2T (Top Side)	10 Pin, dual row, SMT header (20 pos)	Samtec	TSM-110-01-T-DV
J1 J2B (Bottom Side)	10 Pin, dual row, SMT socket (20 pos)	Samtec	SSW-110-22-F-D-VS
J3 (Top Side)	5 Pin, dual row, SMT header (10 pos)	Samtec	TSM-105-01-T-DV
J3B (Bottom Side)	5 Pin, dual row, SMT socket (10 pos)	Samtec	SSW-105-22-F-D-VS
R5 R6 R7 R9 R10 R11 R12 R13 R14 R8 R15 R16 R17 R18 R19 R20 R22 R23	10 kΩ 0603	Yageo America	9C06031A1002JLHFT
R1 R2 R3 R4 R24	0 Ω, 0603	Yageo America	9C06031A0R00JLHFT
R21	1 kΩ, 0603	Yageo America	9C06031A1001JLHFT
SW1 SW2 SW3 SW4	DPDT Switch	E Switch	EG2209
TP1	Turret type test point	Mill-Max	2348-2-01-00-00-07-0
U1	REF102	TI	REF102AU
U2	OPA4227	TI	OPA4227UA
U3	OPA4277	TI	OPA4277UA
U4	DAC8803 or DAC8814	TI	DAC8803IDB or DAC8814ICDB
U5	INA105	TI	INA105KU
U6	OPA227	TI	OPA227UA
W1 W2 W3 W4 W5 W6 W7 W8 W9 W10	3 Pin, 2 mm header	Samtec	TMM-103-03-T-S

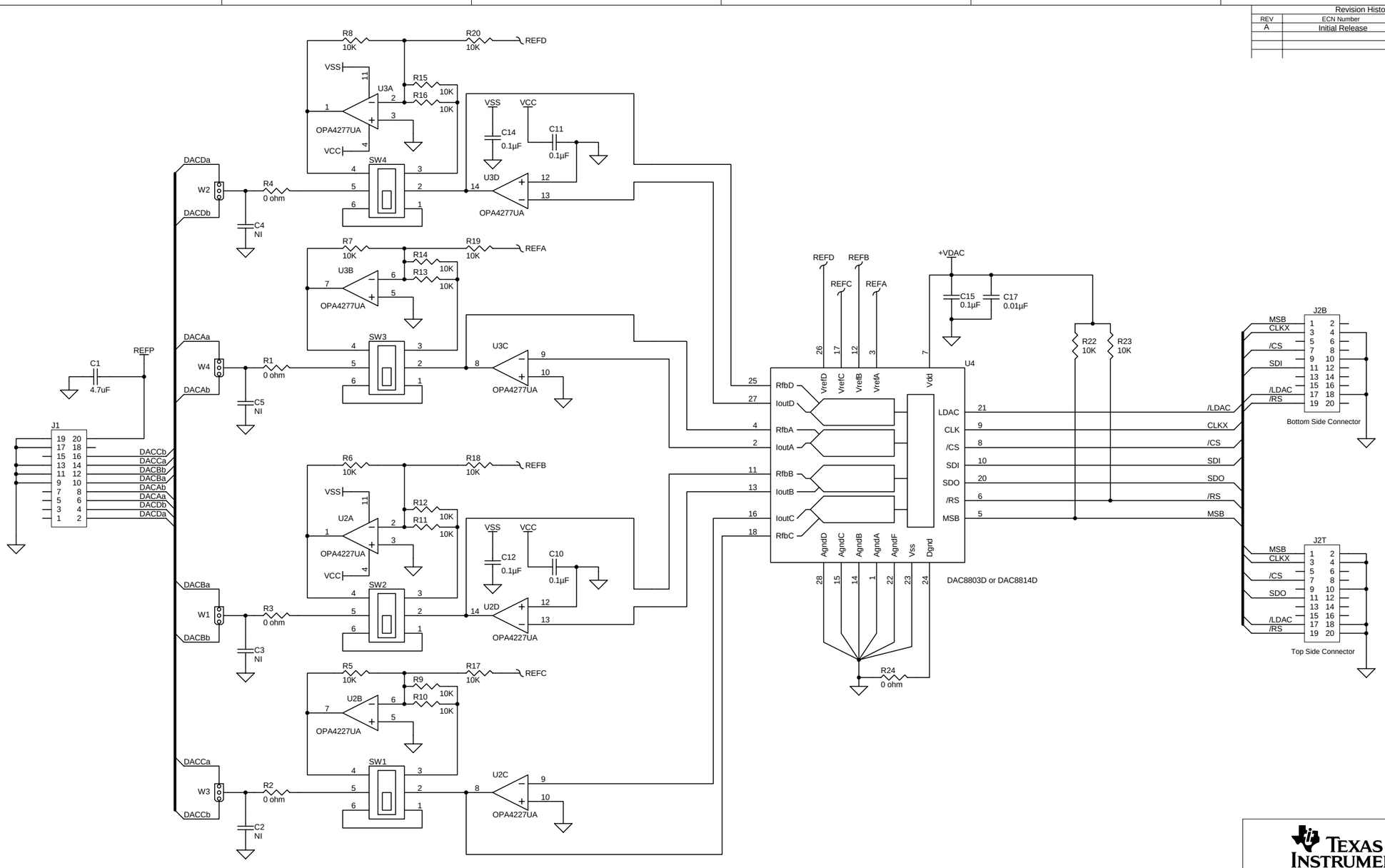
6.2 Layout

Gerber files are available on request. Contact the Product Information Center at (972) 644-5580.

6.3 Schematic

The schematic diagram is provided on the following pages.

Revision History		
REV	ECN Number	Approved
A	Initial Release	TH



TEXAS INSTRUMENTS

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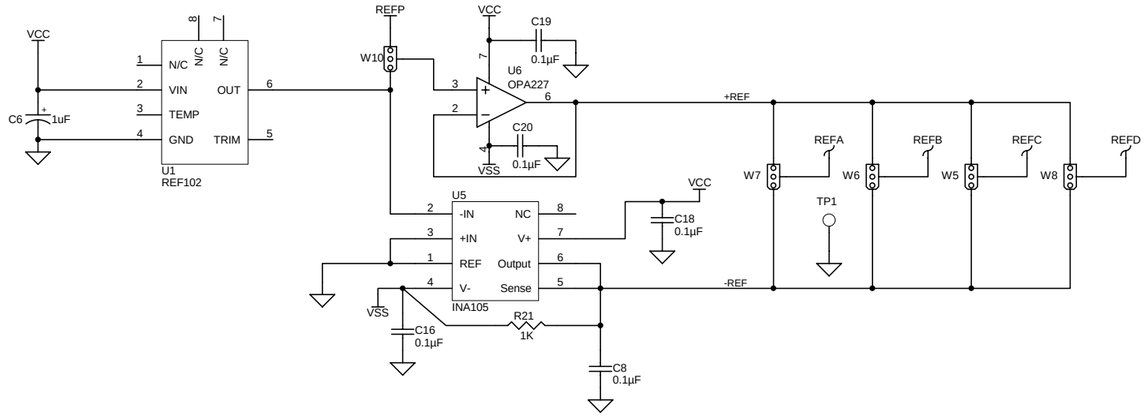
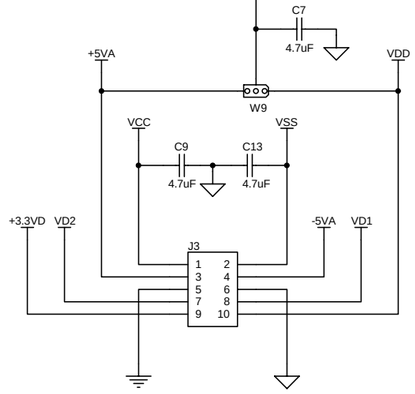
Title:	DAC8803_14 EVM
Engineer: T. Hendrick	DOCUMENTCONTROL # 6478165 REV: A
Drawn By: T. Hendrick	
FILE: DAC8803_14_SH1.Sch	DATE: 23-May-2006 SIZE: SHEET: 1 OF: 2





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Title: DAC8803_14 EVM			
Engineer: T. Hendrick			
Drawn By: T. Hendrick	SIZE: B	DATE: 23-May-2006	REV: A
FILE: 6478165			SHEET: 2 OF: 2

7 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this booklet by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

EVM Compatible Device Data Sheets:	**Literature Number:**
DAC8803	SBAS340
DAC8814	SBAS338

App Notes/Additional Literature from Texas Instruments:	**Literature Number:**
Op Amps for Everyone	SLOD006
5-6K Interface Board	SLAU104
Single and Bipolar Supply Signal Conditioning Boards	SLAU105
HPA-MCU Interface Board	SLAU106

Third Party Tools:	**Vendor Website:**
HPA449 Development Board (MSP430 Tools)	www.softbaugh.com
Speedy 33 (DSP Tools)	www.hyperception.com
TI Analog Adapter Board (For Xilinx FPGAs)	www.avnet.com

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of +15 V to -15 V and the output voltage range of +10 V to -10 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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