Texas Instruments

ADS8383EVM

User's Guide

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Data Acquistion

SLAU119

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ±6 V and the output voltage range of 0 V and 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the ADS8383 18-bit, 500 kHz parallel interface analog to digital converter evaluation board. A complete circuit description as well as schematic diagram and bill of materials is included.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 – EVM Overview
- ❏ Chapter 2 – Analog Interface
- ❏ Chapter 3 – Digital Interface
- ❏ Chapter 4 – Power Supply Requirements
- ❏ Chapter 5 – Using the EVM
- ❏ Chapter 6 − ADS8383EVM BOM, Layout and Schematic

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Data Sheets:	**Literature Number:**
ADS8383	SLAS005
REF3040	SBVS032
REF3020	SBVS032
SN74AHC138	SCLS258
SN74AHC245	SCLS230
SN74AHC1G04	SCLS318
THS4031	SLOS224

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Contents

Figures

Tables

Chapter 1

EVM Overview

This chapter contains the features of the ADS8383EVM.

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1.1 Features

- Full-featured evaluation board for the high-speed ADS8383 18-bit, single channel, parallel interface SAR type analog to digital converters.
- Onboard signal conditioning
- Onboard reference
- Input and output digital buffer
- Onboard decoding for stacking multiple EVMs

Chapter 2

Analog Interface

The ADS8383 analog-to-digital converter has both a positive and negative analog input pin. The EVM provides ground for the negative input close the device via SJP3, or allows a user-furnished ground wire. The negative input pin has a range of –200 mV up to 200 mV, and is shorted on the EVM via SJP3. A signal for the positive input pin can be applied at connector P1, pin 2 (shown in Table 2−1), or applied to the center pin of SMA connector J2.

Table 2−1. Analog Input Connector

Description	Signal Name	Connector.Pin#		Signal Name	Description
Pin tied to Ground	AGND	P1.1	P1.2	+	Noninverting Input Channel
Reserved	N/A	P1.3	P1.4	N/A	Reserved
Reserved	N/A	P1.5	P1.6	N/A	Reserved
Reserved	N/A	P1.7	P1.8	N/A	Reserved
Pin tied to Ground	AGND	P1.9	P.10	N/A	Reserved
Pin tied to Ground	AGND	P1.11	P1.12	N/A	Reserved
Reserved	N/A	P1.13	P1.14	N/A	Reserved
Pin tied to Ground	AGND	P1.15	P1.16	N/A	Reserved
Pin tied to Ground	AGND	P1.17	P1.18	N/A	Reserved
Reserved	N/A	P1.19	P1.20	REF+	External Reference Input

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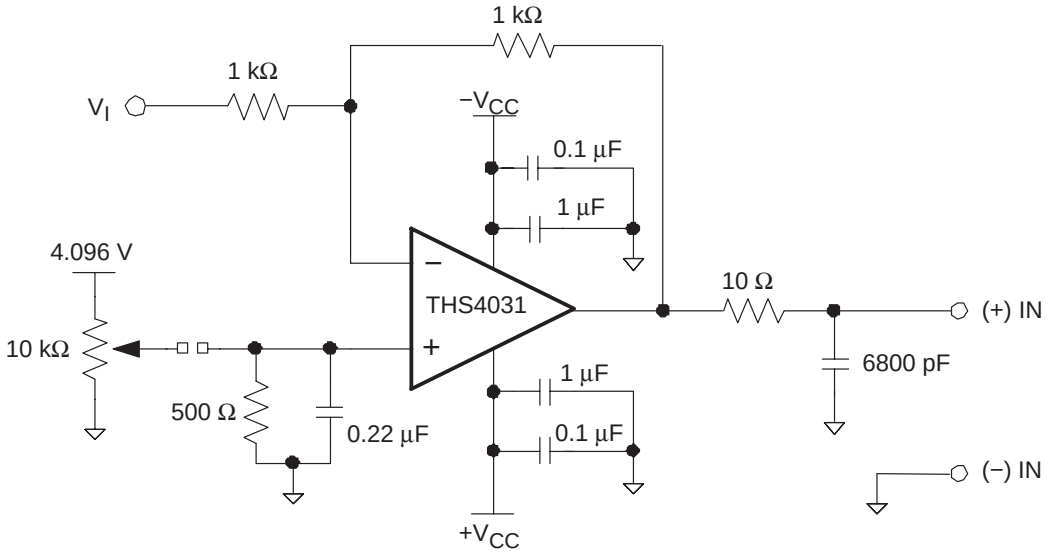
2.1 Signal Conditioning

The factory recommends the analog input to any SAR type converter be buffered and low-pass filtered. It is important to note that the input buffer circuit of the ADS8383EVM, shown in Figure 2−1, utilizes the THS4031 configured as an *inverting* gain of one. The amplifier is not stable in a *conventional* a gain-of-one configuration. The THS4031 was selected for it's low noise, high slew rate and fast settling time. The low pass filter resistor and capacitor values were selected such that ADS8383EVM would meet the 100 kHz AC performance specifications listed in the data sheet. The series resistor works in conjunction with the capacitor to filter the input signal, but also isolates the amplifier from the 6800 pF capacitive load. The capacitor to ground at the input of the A/D works in conjunction with the series resistor to filter the input signal, and acts like a charge reservoir. This external filter capacitor works with the amplifier to charge the internal sampling capacitor during sampling mode.

The EVM has a provision to offset the input voltage by adjusting R23, a 10-kΩ potentiometer.

Figure 2−1. Input Buffer Circuit



2.2 Reference

The ADS8383EVM provide an onboard 4.096-V reference circuit. The EVM also has the provision for users to supply a reference voltage via connecter P1 pin 20. This reference voltage may be filtered by installing amplifier U1. The converter itself has onboard reference buffer, therefore it is not necessary to buffer externally. The reference buffer circuit on the EVM is not populated with an amplifier. The EVM allows users to select from two reference sources. Set SJP1 and SJP2 to select onboard reference voltage (REF3040) or a user-supplied reference voltage via P1 pin 20. See Table 2−2 for jumper settings. See Chapter 6 for the full schematic.

Table 2−2. Solder Short Jumper Setting

Reference Designator	Description	Jumper Setting	
		1−2	2−3
SJP1	Select REF3040 output for reference voltage	Installed†	Not installed
	Select buffered reference voltage	Not installed	Installed
SJP2	Select U3, REF3040, as 4.096V reference	Installed†	
	Buffer User supplied reference voltage	Not Installed	Installed
SJP3	Short (−)IN pin to ground	Installed†	N/A
SJP4	Apply offset voltage to A/D buffer	Not Installed	N/A
SJP5	Set amplifier U1 negative supply to ground	Installed	
	Set amplifier U1 negative supply to $-V_{CC}$	Not Installed	Installed†
SJP6	Set amplifier U2 negative supply to ground	Installed	Not Installed
	Set amplifier U2 negative supply to $-V_{CC}$	Not Installed	Installed†

† Factory set condition

Chapter 3

Digital Interface

The ADS8383EVM is designed for easy interfacing to multiple platforms. Samtec part numbers SSW−110−22−F−D−VS−K and TSM−110−01−T−DV−P provide a convenient dual row header/socket combination at P2 and P3. Consult Samtec at www.samtec.com or 1−800−SAMTEC−9 for a variety of mating connector options.

Table 3−1. Pinout for Parallel Control Connector P2

Connector.Pin	Signal	Description
P2.1	$\overline{DC}\_\overline{CS}$	Daughter card Board Select pin
P2.3		
P2.5		
P2.7	A0	Address line from processor
P2.9	A1	Address line from processor
P2.11	A2	Address line from processor
P2.13		
P2.15		
P2.17		
P2.19	$\overline{INTc}$	Set jumper W3 to select BUSY or inverted signal to be applied to this pin.

Note: All even numbered pins of P2 are tied to DGND.

Read ($\overline{RD}$) and conversion start ($\overline{CONVST}$) signals to the converter can be assigned to two different addresses in memory via jumper settings. This allows for the stacking of up to two ADS8383EVMs into processor memory. See Table 3−2 for jumper settings. Note, the evaluation module does not allow chip select ($\overline{CS}$) line of the converter to be assigned to different memory locations. It is therefore suggested the $\overline{CS}$ line be grounded or wired to an appropriate signal of the processor.

Table 3−2. Jumper Settings

Reference Designator	Description	Jumper Settings	
		1−2	2−3
W1	Set A[2..0] = 0x1 to generate $\overline{RD}$ pulse	Installed†	Not installed
	Set A[2..0] = 0x2 to generate $\overline{RD}$ pulse	Not installed	Installed
W2	Set A[2..0] = 0x3 to generate $\overline{CONVST}$ pulse	Installed†	Not installed
	Set A[2..0] = 0x4 to generate $\overline{CONVST}$ pulse	Not installed	Installed
W3	Apply BUSY to P3 pin 19	Not installed	Installed†
	Apply inverted BUSY to P3 pin 19	Installed†	Not installed

† Factory set condition

The data bus is available at connector P3, see Table 3−3 for pin out information.

Table 3−3. Data Bus Connector P3

Connector.Pin	Signal	Description
P3.1	D0	Buffered Data Bit 0 (LSB)
P3.3	D1	Buffered Data Bit 1
P3.5	D2	Buffered Data Bit 2
P3.7	D3	Buffered Data Bit 3
P3.9	D4	Buffered Data Bit 4
P3.11	D5	Buffered Data Bit 5
P3.13	D6	Buffered Data Bit 6
P3.15	D7	Buffered Data Bit 7
P3.17	D8	Buffered Data Bit 8
P3.19	D9	Buffered Data Bit 9
P3.21	D10	Buffered Data Bit 10
P3.23	D11	Buffered Data Bit 11
P3.25	D12	Buffered Data Bit 12
P3.27	D13	Buffered Data Bit 13
P3.29	D14	Buffered Data Bit 14
P3.31	D15	Buffered Data Bit 15
P3.33	D16	Buffered Data Bit 16
P3.35	D17	Buffered Data Bit 17 (MSB)

Note: All even numbered pins of P3 are tied to DGND.

This evaluation module provides direct access to all the analog-to-digital converter control signals via connector J4, see Table 3−4.

Table 3−4. Pinout for Converter Control Connector J4

Connector.Pin	Signal	Description
J4.1	$\overline{CS}$	Chip Select pin. Active low
J4.3	$\overline{RD}$	Read pin. Active low
J4.5	$\overline{CONVST}$	Convert start pin. Active low
J4.7	BYTE	Byte select input. Used for 8-bit bus reading.
J4.9	BUS 18/$\overline{16}$	Bus size select input. Used for selecting 18-bit or 16-bit wide bus transfer.
J4.11	BUSY	Converter Status Output. High when a conversion is in progress.

Note: All even numbered pins of P4 are tied to DGND.

Chapter 4

Power Supply Requirements

The EVM accepts four power supplies.

- ❑ A dual ±Vs DC supply for the dual supply op−amps. Recommend ±6VDC supply.
- ❑ A single +5.0 V DC supply for analog section of the board (A/D + Reference).
- ❑ A single +5.0 V or +3.3 VDC supply for digital section of the board (A/D + address decoder + buffers).

There are two ways to provide these voltages.

1) Wire in the voltages at test points on the EVM. See Table 4−1.

Table 4−1. Power Supply Test Points

Test Point	Signal	Description
TP16	+BVDD	Apply +3.3 V or +5.0 V. See ADC datasheet for full range.
TP20	+AVCC	Apply +5.0 V.
TP14	+VA	Apply +6.0 V. Positive supply for amplifier.
TP18	−VA	Apply –6.0 V. Negative supply for amplifier.

2) Use the power connector J1, and derive the voltages elsewhere. The pinout for this connector is shown below. If using this connector, set W4 jumper to connect +3.3 V or +5 V from connector to +BVDD. Short between pins 1−2 to select +5 VD, or short between pins 2−3 to select +3.3 VD as the source for the digital buffer voltage supply (+BVDD).

Table 4−2. Power Connector, J1, Pin Out

Signal	Power Connector − J1		Signal
+VA(+6V)	1	2	–VA (–6V)
+5VA	3	4	N/C
DGND	5	6	AGND
N/C	7	8	N/C
+3.3VD	9	10	+5VD

Chapter 5

Using the EVM

The ADS8383EVM serves three functions

1) As a reference design
2) As a prototype board and
3) As software test platform

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5.1 As a Reference Board

As a reference design, the ADS8383EVM contains the essential circuitry to showcase the analog-to-digital converter. This essential circuitry includes the input amplifier, reference circuit, and buffers. The EVM analog input circuit is optimized for 100 kHz sine wave, therefore users may need to adjust the resistor and capacitor values of the A/D input RC circuit. In AC type applications where signal distortion is a concern, polypropylene capacitors should be used in the signal path.

5.2 As a Prototype Board

As a prototype board, the buffer circuit consists of footprint is a standard 8-pin SOIC and resistor pads for inverting and noninverting configurations. The ADS8383EVM can be used to evaluate both dual and single supply amplifiers. The EVM comes installed with a dual supply amplifier as it allows the user to take advantage of the full input voltage range of the converter. For applications that require signal supply operation and smaller input voltage range, the THS4031 can be replaced with the single supply amplifier like OPA300. Pad jumper SJP6 should be shorted between pads 1 and 2, as it shorts the minus supply pin of the amplifier to ground. Positive supply voltage can be applied via test point TP14 or connector J1 pin 1.

5.3 As a Software Test Platform

As a software test platform, connectors P1, P2, P3 plug into the parallel interface connectors of the 5−6K interface card. The 5−6K interface card sits on the C5000 and C6000 Digital Signal Processor starter kit (DSK). The ADS8383EVM is then mapped into the processor’s memory space. This card also provides an area for signal conditioning. This area can be used to install application circuit(s) for digitization by the ADS8383 analog-to-digital converter. Refer to the 5−6K interface card user’s guide (SLAU104) for more information.

For the software engineer the ADS8383EVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1” headers and sockets to wire into prototype boards. The user need only provide in 3 address lines (A2, A1, A0) and address valid line($\overline{\text{DC\_CS}}$) to connector P2. To choose which address combinations will generate $\overline{\text{RD}}$ and $\overline{\text{CONVST}}$ set jumpers as shown in Table 3−2. Recall chip select ($\overline{\text{CS}}$) signal is not memory mapped or tied to P2, therefore it must be controlled via general purpose pin or shorted to ground at J3 pin 1. If address decoding is not required, the EVM provides direct access to converter data bus via P3 and control via J3.

Chapter 6

ADS8383EVM BOM, Layout, and Schematic

This chapter contains the ADS8383EVM bill of materials, the layouts, and the schematic.

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6.1 ADS8383EVM Bill of Materials

Table 6−1 contains a complete bill of materials for the ADS8383EVM. The schematic diagram is also provided for reference. Contact the Product Information Center or e−mail dataconvapps@list.ti.com for questions regarding this EVM.

Table 6−1. ADS8383EVM Bill Of Materials

Item No.	QTY	Value	Reference Designators	Mfg	Mfg's Part Number	Description
1	2	0	R4 R21	Panasonic − ECG or Alternate	ERJ−3GEY0R00V	Resistor 0 Ω 1/16W 5% 0603 SMD
2	1	0	R1	Panasonic − ECG or Alternate	ERJ−6GEY0R00V	Resistor 0.0 Ω 1/10W 5% 0805 SMD
3	1	10	R13	Panasonic − ECG or Alternate	ERJ−6ENF10R0V	Resistor 10.0 Ω 1/10W 1% 0805 SMD
4	1	50	R24	Panasonic − ECG or Alternate	ERJ−6ENF49R9V	Resistor 49.9 Ω 1/10W 1% 0805 SMD
5	2	100	R14 R15	Panasonic − ECG or Alternate	ERJ−3EKF1000V	Resistor 100 Ω 1/16W 1% 0603 SMD
6	1	100	R25	Panasonic − ECG or Alternate	ERJ−6ENF1000V	Resistor 100 Ω 1/10W 1% 0805 SMD
7	1	499	R2	Panasonic − ECG or Alternate	ERJ−6ENF4990V	Resistor 499 Ω 1/10W 1% 0805 SMD
8	2	1k	R6 R10	Panasonic − ECG or Alternate	ERJ−6ENF1001V	Resistor 1.00 kΩ 1/10W 1% 0805 SMD
9	5	10k	R16 R17 R18 R19 R20	Panasonic − ECG or Alternate	ERJ−3EKF1002V	Resistor 10.0 kΩ 1/16W 1% 0603 SMD
10	1	10k	R7	Panasonic − ECG or Alternate	ERA−S15J103V	Resistor 10 kΩ 1/10W 1500 PPM 5%0805
11	1	NI	R3	NOT INSTALLED	NOT INSTALLED	
12	1	NI	R11	NOT INSTALLED	NOT INSTALLED	
13	4	1 nF	C3 C5 C11 C23	Kemet or Alternate	C1206C102J5GACTU	Capacitor 1000 pF 50V ceramic NPO 1206
14	1	6800 pF	C39	WIMA or Alternate	MKP2 6800/630/5	6800 pF polypropylene capacitor
15	9	0.01 µF	C21 C41 C44 C46 C48 C53 C56 C65 C50	Kemet or Alternate	C0603C103J5RACTU	Capaciator 10000 pF 50V Ceramic X7R 0603
16	2	0.01 µF	C10 C20	Kemet or Alternate	C0805C103K5RACTU	Capacitor 10000 pF 50V Ceramic X7R 0805
17	2	0.01 µF	C4 C26	Kemet or Alternate	C1206C103J5RACTU	Capacitor 10000 pF 50V Ceramic X7R 1206
18	14	0.1 µF	C25 C40 C42 C43 C47 C51 C52 C54 C55 C57 C58 C59 C64 C38	Kemet or Alternate	C0603C104K3RACTU	Capacitor 0.1 µF 25V Ceramic X7R 0603

Item No.	QTY	Value	Reference Designators	Mfg	Mfg's Part Number	Description
19	7	0.1 µF	C7 C9 C15 C22 C32 C34 C36	Kemet or Alternate	C0805C104J5RACTU	Capacitor .10 µF 50V ceramic X7R 0805
20	4	1 µF	C8 C16 C31 C37	Panasonic − ECG or Alternate	ECJ−GVB1C105K	Capacitor 1 µF 16V ceramic X5R 0805
21	2	1 µF	C2 C28	Kemet or Alternate	C1206C105K3RACTU	Capacitor 1.0 µF 25V ceramic X7R 1206
22	1	0.22 µF	C33	Panasonic − ECG or Alternate	ECJ−2VB1C224K	Capacitor 0.22 µF 16V ceramic X7R 0805
23	2	0.47 µF	C61 C63	Panasonic − ECG or Alternate	ECJ−1VF1C474Z	Capacitor 0.47 µF 16V ceramic Y5V 0603
24	1	10 µF	C62	Panasonic − ECG or Alternate	ECJ−2FF1A106Z	Capacitor 10 µF 10V ceramic F 0805
25	4	10 µF	C1 C6 C12 C19	Panasonic − ECG or Alternate	ECJ−3YB1C106M	Capacitor 10 µF 16V ceramic X5R 1206
26	5	10 µF	C14 C24 C27 C29 C49	Kemet or Alternate	T491B106K016AS	Capacitor TANT 10 µF 16V 10% SMT
27	1	22 µF	C17	Panasonic − ECG or Alternate	ECJ−3YB0J226M	Capacitor 22 µF 6.3V ceramic X5R 1206
28	4	NI	C13 C18 C45 C60	NOT INSTALLED	NOT INSTALLED	
29	3	NI	C30 C35 R5	NOT INSTALLED	NOT INSTALLED	
30	2	1K	RP1 RP3	CTS Corporation	742C163102JTR	RES ARRAY 1K OHM 16TERM 8RES SMD
31	1	100	RP2	CTS Corporation	742C163101JTR	RES ARRAY 100 OHM 16TRM 8RES SMD
32	1	1K	RP4	CTS Corporation	744C083102JTR	RES ARRAY 1K OHM 8TERM 4RES SMD
33	1	10k	R23	Bourns	3214W−1−103E	TRIMPOT 10K OHM 4MM TOP ADJ SMD
34	4	BLM21AJ601SN1L	L1 L2 L3 L4	Murata ERIE	BLM31PG601SN1L	Chip ferrite beads− 600 Ω at 100 MHz
35	1	OPA627	U1	NOT INSTALLED	NOT INSTALLED	Amplifier
36	1	THS4031	U2	Texas Instruments	THS4031IDR	100−MHz low-noise high-speed amplifier
37	1	REF3040	U3	Texas Instruments	REF3040AIDBZT	REF3040 50 ppm/°C, 50 µA in SOT23−3 CMOS voltage reference
38	1	ADS8383	U4	Texas Instruments	ADS8383IPFB	ADS8383 18-bIT 500 KSPS
39	4	SN74AHC245PWR	U5 U6 U7 U8	Texas Instruments	SN74AHC245PWR	Octal bus transceiver, 3-state
40	1	SOIC-8 Footprint	U9	NOT INSTALLED	NOT INSTALLED	Footprint for 8 pin SOIC reference that operates from +5V.
41	1	REF3020	U10	Texas Instruments	REF3020AIDBZT	REF3020 50 ppm/°C, 50 µA in SOT23−3 CMOS voltage reference
42	1	SN74AHC138PWR	U11	Texas Instruments	SN74AHC138PWR	3-Line to 8-Line decoder/ demultiplexer

Item No.	QTY	Value	Reference Designators	Mfg	Mfg's Part Number	Description
43	1	SN74AHC1G04 DBV	U12	Texas Instruments	SN74AHC1G04DBVR	Single inverter gate
44	1	5X2X.1	J1	Samtec	SSW−105−22−S−D−VS	0.025" SMT socket − bottom side of PWB
				Samtec	TSM−105−01−T−D−V−P	0.025" SMT plug − top side of PWB
45	1	SMA_PCB_MT	J2	Johnson Components Inc.	142−0701−301	Right angle SMA connector
46	1	6X2X.1	J4	Samtec	SSW−106−22−S−D−VS	0.025" SMT socket − bottom side of PWB
				Samtec	TSM−106−01−T−D−V−P	0.025" SMT plug − top side of PWB
47	1	18X2X.1_SMT_ PLUG_&_ SOCKET	P3	Samtec	SSW−118−22−S−D−VS	0.025" SMT socket − bottom side of PWB
				Samtec	TSM−118−01−T−D−V−P	0.025" SMT plug − top side of PWB
48	2	10X2X.1	P1 P2	Samtec	SSW−110−22−S−D−VS	0.025" SMT socket − bottom side of PWB
				Samtec	TSM−110−01−T−D−V−P	0.025" SMT plug − top side of PWB
49	2	SJP2	SJP3 SJP4	NOT INSTALLED	NOT INSTALLED	Pad 2 position jumper
50	4	SJP3	SJP1 SJP2 SJP5 SJP6	NOT INSTALLED	NOT INSTALLED	Pad 3 Postion jumper
51	4	3POS_JUMPER	W1 W2 W3 W4	Samtec	TSW−103−07−L−S	3 Position jumper _ 0.1" spacing
52	16	TP_0.025	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP14 TP15 TP16 TP17 TP18 TP19 TP20	Keystone Electronics	5000K–ND	Test point − single 0.025" pin

6.2 ADS8383EVM Layout

Figure 6−1. Top Layer—Layer 1

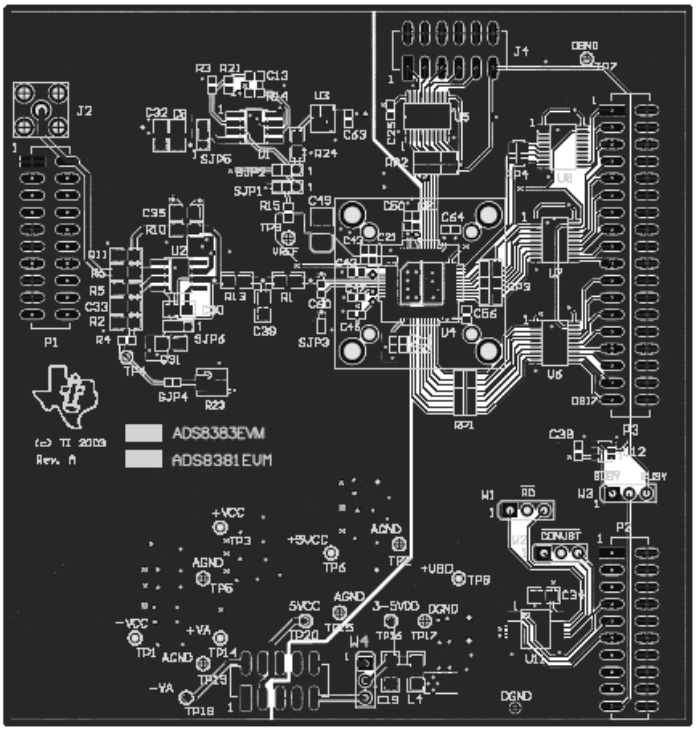


Figure 6−2. Ground Plane—Layer 2

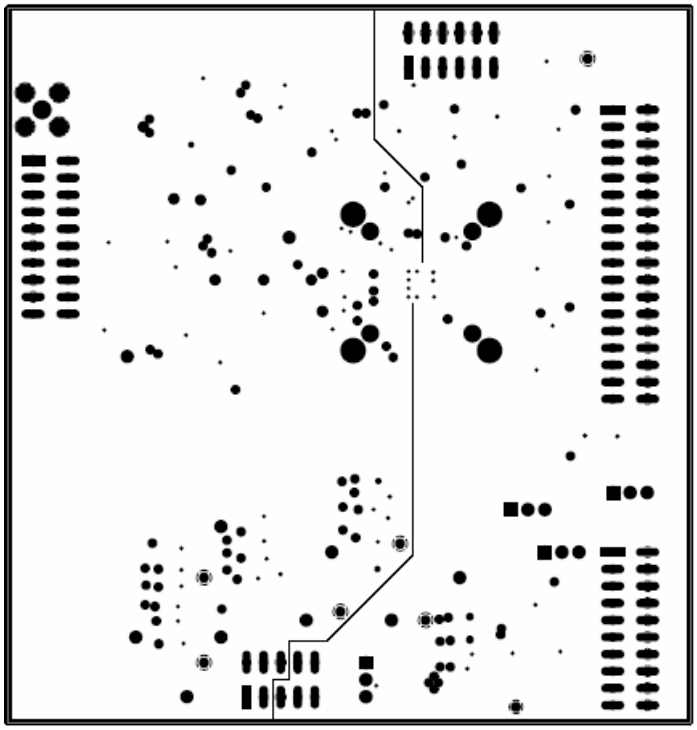


Figure 6−3. Power Plane—Layer 3

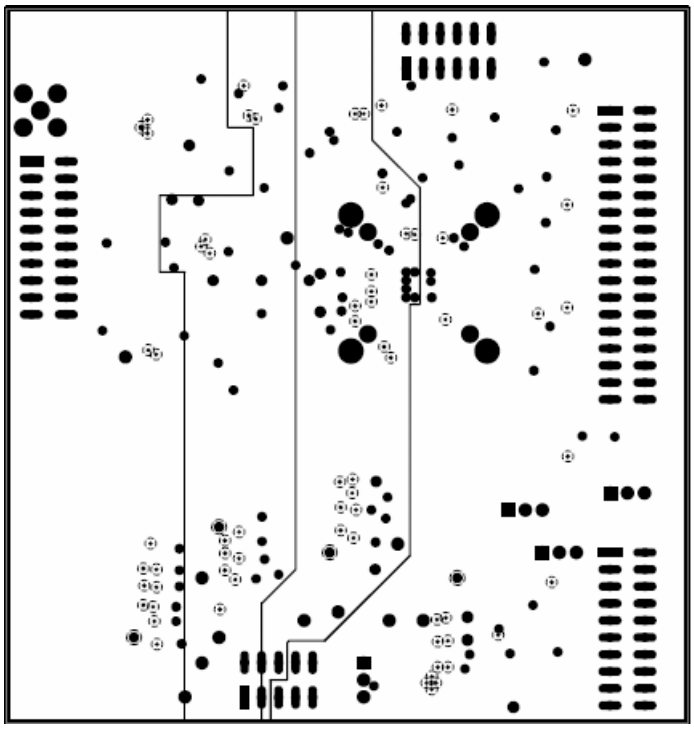
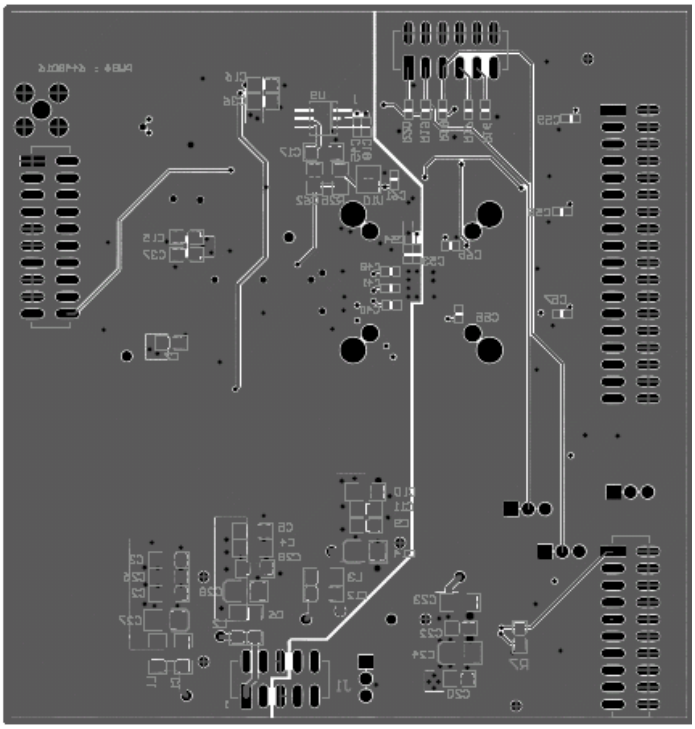


Figure 6−4. Bottom Layer—Layer 4



6.3 ADS8383EVM Schematic

The schematic follows this page.