TEXAS INSTRUMENTS

DAC8531 Evaluation Module

User's Guide

June 2001

AAP Data Acquistion (Dallas)

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and the use of the DAC8531 Evaluation Module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 – Overview
- ❏ Chapter 2 – Physical Description
- ❏ Chapter 3 – EVM Operation

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This manual may contain cautions and warnings. This information is provided for your benefit and protection. Read each caution and warning carefully.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

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Data Sheets:	**Literature Number:**
DAC8531	SBAS192
DAC8501	SBAS212
DAC7513	SBAS157
DAC7512	SBAS156
REF02	PDS–1177
TPS6734	SLVS127
OPA350	PDS–1470
OPA177	PDS–1081
SN74AHC74	SCLS255
SN74ACT10	SCAS526
SN74AHC08	SCLS236
SN74AHC1G04	SCLS318
SN74HC166	SCLS117
SN74HC163	SCLS298
Application Reports:	
TMS320C6000 EVM Daughterboard Interface	SPRA478

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Chapter 1

EVM Overview

This chapter presents a general overview of the DAC8531 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

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1.1 Features

This EVM features the DAC8531 digital-to-analog converter. It was specifically designed for the DAC8531, but can also accommodate the DAC8501, DAC7513, and DAC7512. The digital-to-analog converter device that is installed onto the board determines the version of this EVM as shown in the table below. Although this EVM is shipped from factory with the DAC8531, the table below shows the different DAC devices that can be installed as an option to the user.

Table 1–1. List of DAC Devices Supported by This EVM

EVM Version	Device Option	Channel	Installation
12-Bit	DAC7512	1	Optional
	DAC7513	1	Optional
16-Bit	DAC8501	1	Optional
	DAC8531	1	Default

Although the DAC was designed for single-supply operation, a bipolar output range is also possible by configuring the output op-amp circuit properly. This is discussed in detail in section 3.2.3. A 5-V precision voltage reference is provided as a default circuit reference for the DAC, but a connection terminal is also available as an option for an external voltage reference if desired. An 80-pin user interface connector that is SPRA711 compliant is included for the C6000 and C54X TI DSP users. A standard 20-pin header connector is also available for general microcontroller/microprocessor users. This EVM has a built-in dc test mode to easily check for board functionality, thus eliminating the arduous task of providing the digital data information for the DAC.

A 3.5 x 5 mm breadboarding area is also provided in the EVM board. This will serve as a platform for any additional circuitry needed that the user deems necessary for further evaluating the DAC onboard or other experiments.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The dc power supply range for this EVM is from 3.3 V to 5.5 V connected to the J2–2 terminal and is referenced to ground through the J2–1 terminal. If the DAC bipolar mode operation is desired, then a separate ±15 V supply is required to provide the rails for the OPA177 op-amp that is used to generate the –5 V rail of the OPA350 op-amp. The 15-V supply connects through the J1–3 terminal, and the –15-V supply connects through the J1–1 terminal. The ±15-V supply is referenced to ground through the J1–2 terminal. The EVM consumes approximately 700 mW at 5.5 V and approximately 500 mW at 3.3 V.

If this EVM is used to connect to a DSP evaluation board through the common connectors, J6 and J7, the DSP evaluation board supplies the power for the EVM through J6 and J7. The jumper W9 is provided to allow the 3.3-V and 5.5-V supply to be selected individually by the user.

Caution

If using an external power supply via J2, remove jumper W9 to avoid potential damage to the DSP circuitry. On the other hand, if a DSP evaluation board is connected through the common connectors, J6 and J7, the external power supply via J2 must be disconnected.

1.2.2 Reference Voltage

A 5-V precision reference voltage is provided through U15 or U16, whichever one is installed onboard, via jumper W14 by shorting pins 1 and 2. An adjustable 100-kΩ potentiometer, R29, is installed in series with a 20-kΩ resistor, R30, to allow the user to adjust the reference voltage to its desired settings. TP11 and TP12 are provided as well, to allow the user to connect an external reference source not to exceed 5 V dc.

Caution

When applying an external voltage reference through TP11, make sure that it does not exceed 5 V maximum. Otherwise, this will damage the U11 device, DUT.

1.3 EVM Basic Functions

The DAC8531EVM is an evaluation platform for the serial input, rail-to-rail output, 12-bit and 16-bit digital-to-analog converters listed in Table 1–1. A built-in test circuit is provided to easily check the EVM board functionality at a 20-MHz serial clock rate. The dc self-test mode is performed by correctly setting the appropriate jumpers and simply turning the SW1 switch to the on position.

Evaluating the DAC device in a more detailed manner can be accomplished with the use of any microprocessor capable of interfacing with standard SPI, QSPI, and Microwire, or DSP interfaces. A versatile three-wire serial interface is implemented to support all the standard interfaces mentioned earlier and can operate at clock rates up to 30 MHz.

The 20-pin headers, J8, J9, and J10 are provided, as a means to channel all the necessary signals needed to interface a microprocessor/microcontroller or some of TI's older DSP starter kit to the DAC8531 EVM. These headers can also be used for customizing the user's processor interface or hooking up with pattern generators. For most of TI's DSP starter kits (DSKs) that support the common connector interface, the headers J6 and J7 mounted on the bottom side of the EVM board, are used to mate with the DSK's 80-pin

common connector headers. Refer to the accompanying DSK manual for proper orientation. If the TI DSK does not map out correctly with the EVM's common connector headers, then a smart adapter, SPRA711 adapter, can be used. The smart adapter routes the necessary signals properly with ease by correctly configuring the adapter board for the DSK being used.

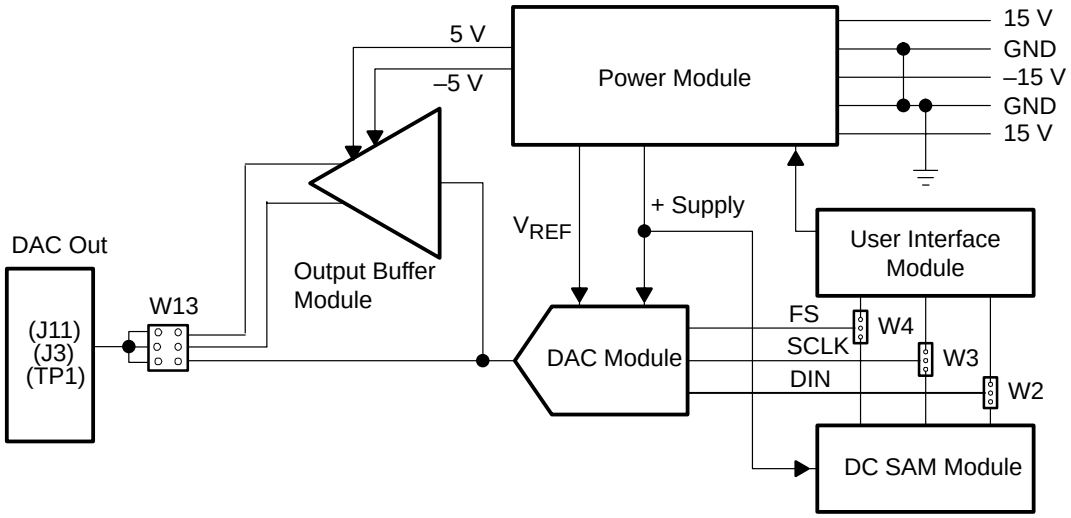
A precision reference voltage is provided onboard, which can be adjusted to the user's preference through the R29 potentiometer. This sets the effective range of the DAC's output signal.

The output of the DAC can be monitored through three different access points which are as follows: an SMA jack (J11), a test point (TP1), and also a header through pin 1 of J3. The 6-pin header, W13, provides different flavors of the DAC output, but requires the output op-amp, U12, to be configured correctly first for the desired waveform characteristic. Shorting pins 1 and 2 of W13 may allow the user to monitor the raw output of the DAC.

A bipolar mode of operation is integrated into the EVM board through the output op-amp, U12. This option to operate in bipolar mode yields a rail-to-rail output voltage range of ±5 V maximum. Although the op-amp, U12, circuit is originally intended for bipolar operation, a single supply option can also be implemented by properly configuring the jumpers.

A block diagram of the EVM is shown in Figure 1–1.

Figure 1–1. EVM Block Diagram



Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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2.1 PCB Layout

The EVM is constructed on a four-layer printed circuit board using a copper-clad FR-4 laminate material. The printed circuit board has a dimensions of 147,828 mm (5.82 inch) × 86,106 mm (3.39 inch), and the board thickness is 1,57 mm (0.062 inch). Figures 2–1 through 2–9 show the individual artwork layers.

Figure 2–1. Top Assembly

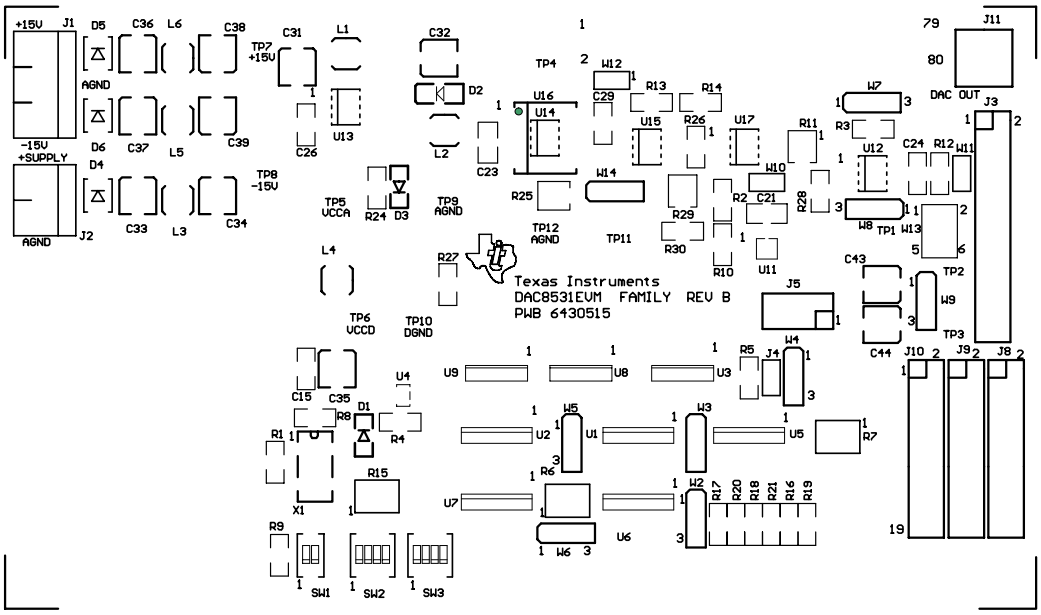


Figure 2–2. Bottom Assembly

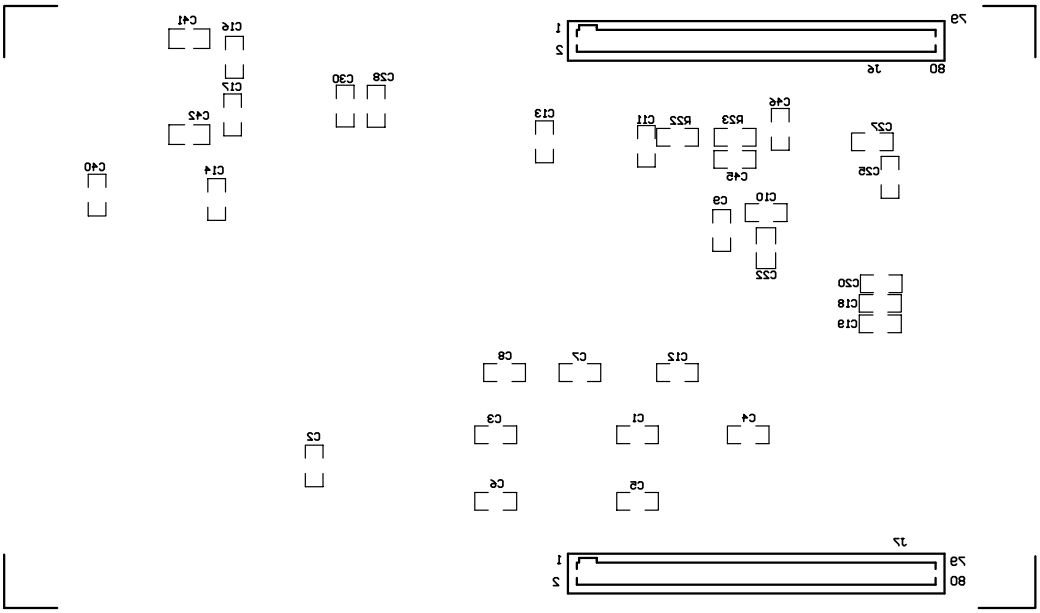


Figure 2–3. Layer 1 (Silkscreen Top)

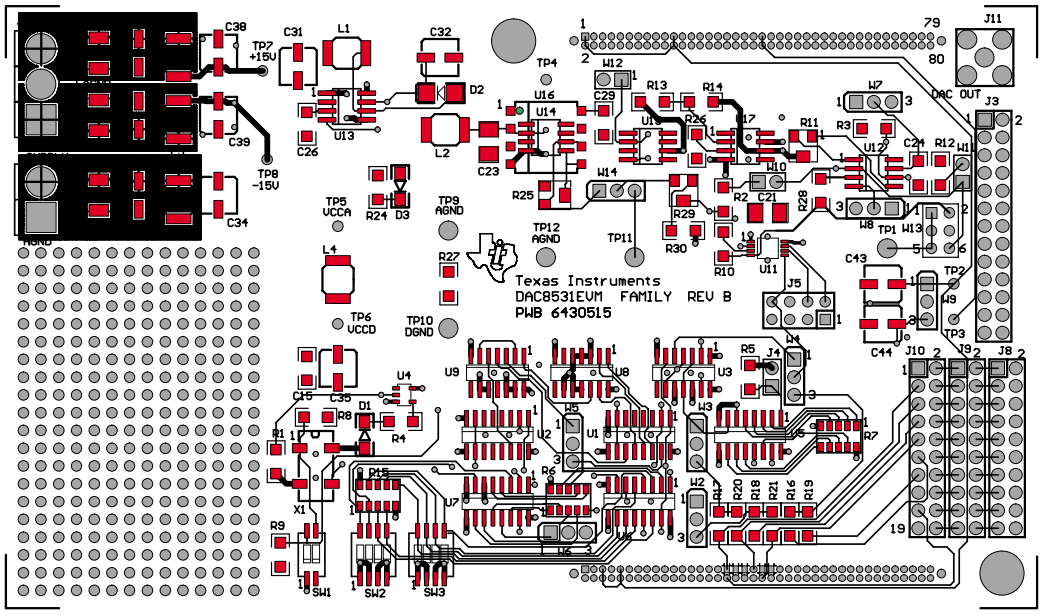


Figure 2–4. Layer 2 (Ground Plane)

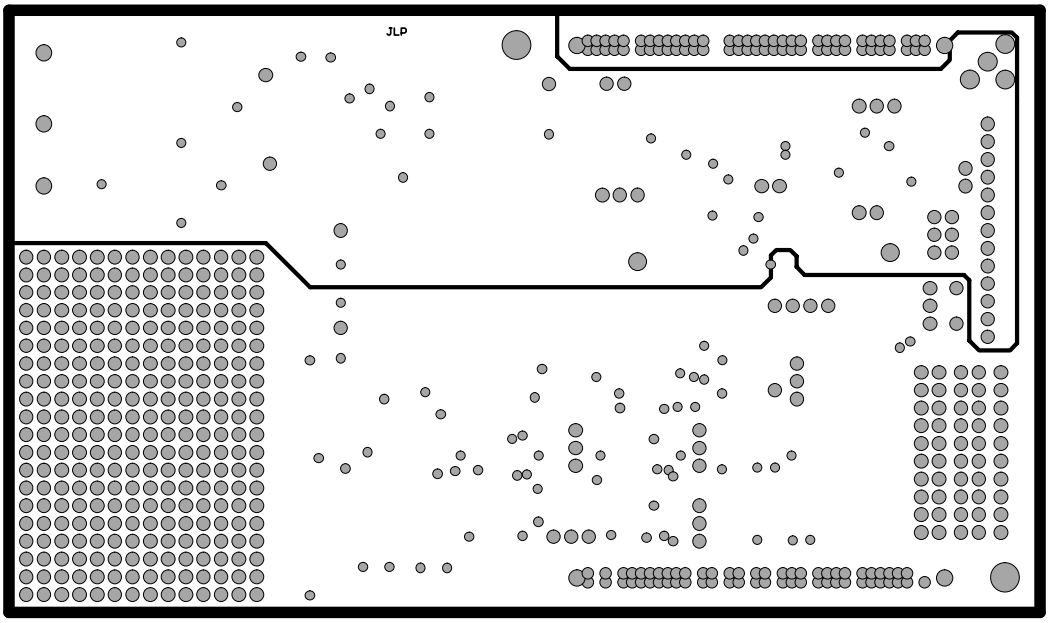


Figure 2–5. Layer 3 (Power Plane)

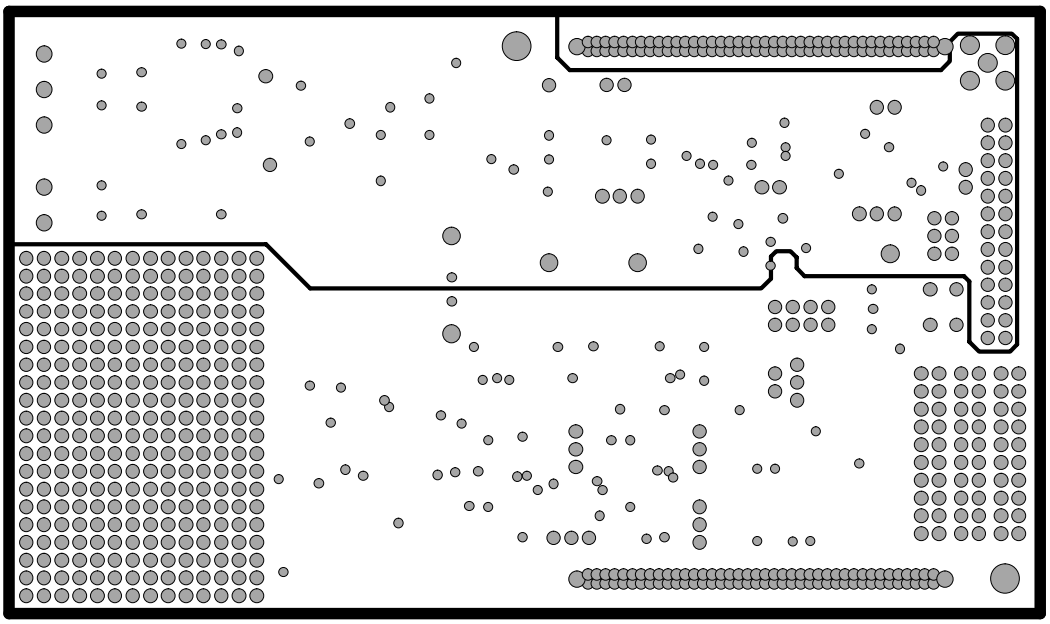


Figure 2–6. Layer 4 (Silkscreen Bottom)

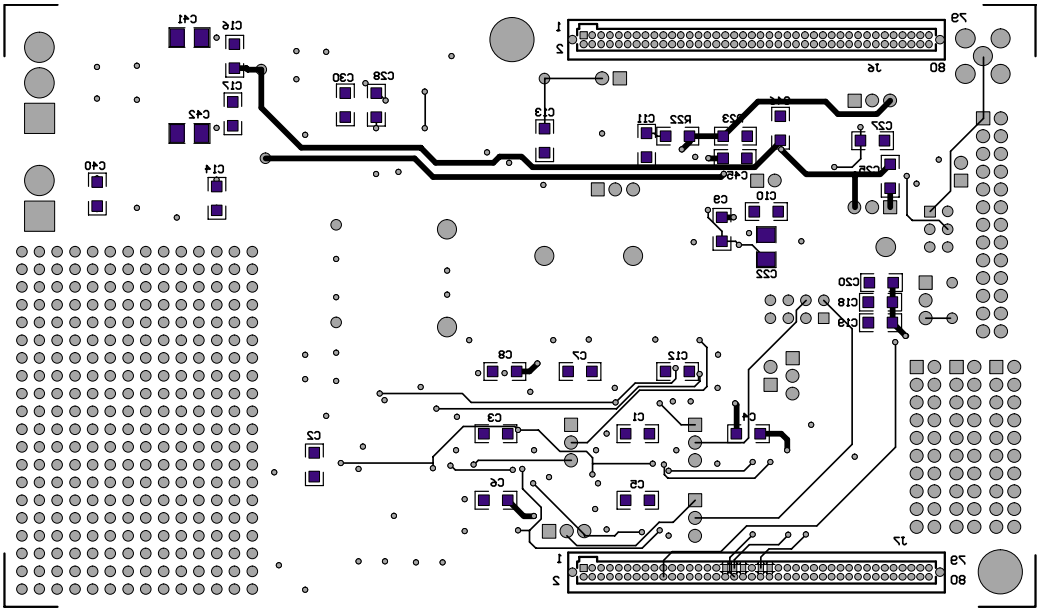


Figure 2–7. Top Paste

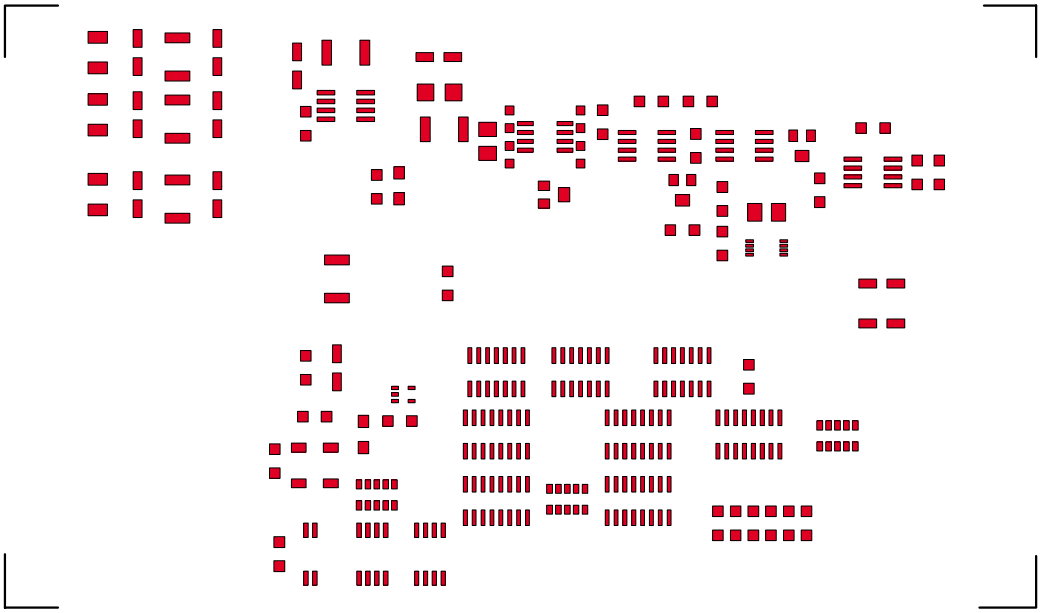


Figure 2–8. Bottom Paste

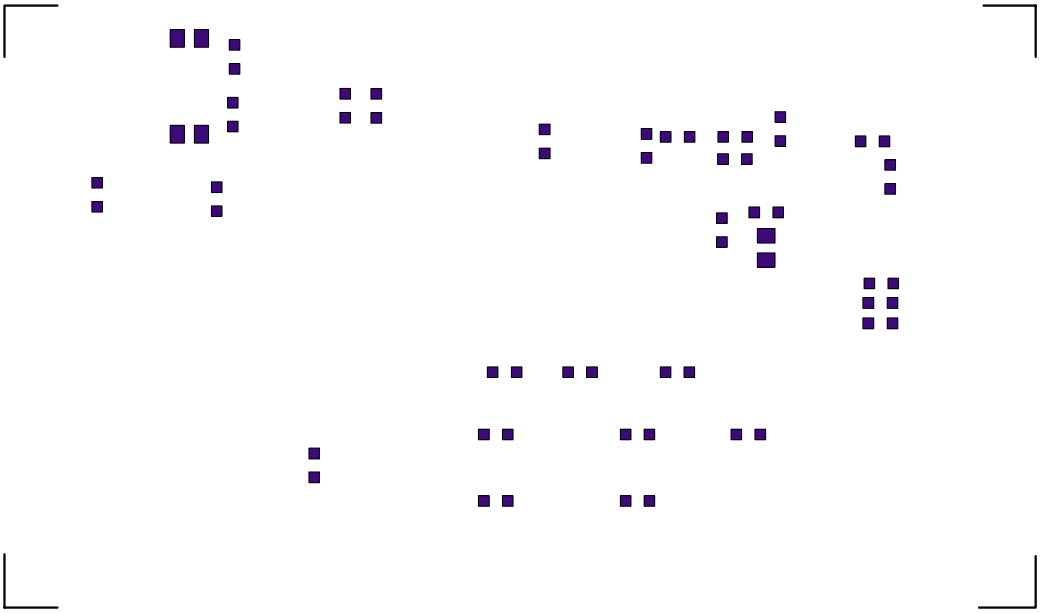
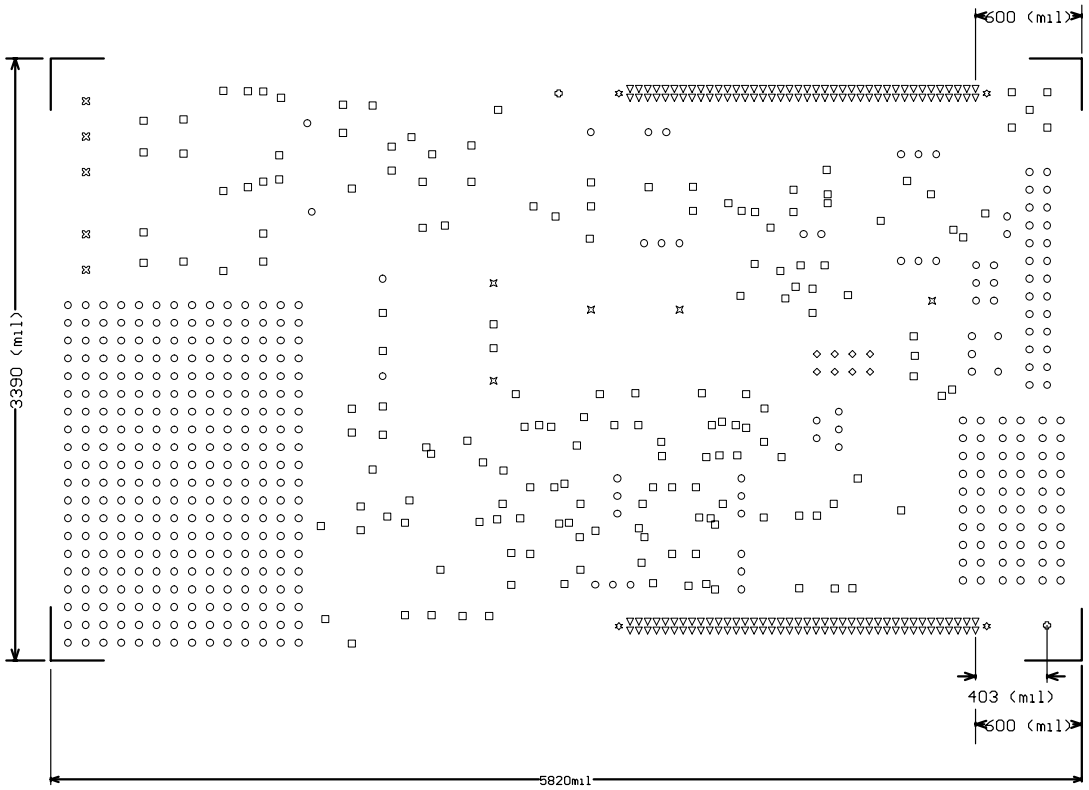


Figure 2–9. Drill Layer (Mechanical Specifications)



□	165	13mil	0.3302mm	PTH
▽	160	25mil	0.635mm	PTH
◇	8	35mil	0.889mm	PTH
○	414	37mil	0.9398mm	PTH
⊠	5	52mil	1.3208mm	PTH
✡	4	53mil	1.3462mm	PTH
⌑	5	62mil	1.5748mm	PTH
□	5	67mil	1.7018mm	PTH
✡	2	125mil	3.175mm	PTH
	768	Total		

Notes:
1) PWB to be fabricated to meet or exceed IPC-6012, Class 2 standards and workmanship shall conform to IPC-A-600, Class 2—current revisions.
2) Board material and construction to be UL approved and marked on the finished board.
3) Laminate material: copper-clad FR-4
4) Copper weight: 1 oz finished—all layers
5) Finished thickness: 0.062 ±0.010 inch
6) Minimum plating thickness in through holes: 0.001 inch
7) SMOBC/HASL
8) LPI soldermask both sides using appropriate layer artwork: color = purple
9) LPI silkscreen as required: color = white
10) Vendor information to be incorporated on back side whenever possible.
11) Minimum copper conductor width is 6 mils
Minimum conductor spacing is 6 mils
Minimum annular ring is 5 mils

2.2 Bill of Materials

Table 2–1. Parts Lists

Item No.	Qty.	Designator	Description	Manufacturer	Part Number
1	22	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C45, C46	0.1-µF Multilayer ceramic capacitor	Panasonic or equivalent	ECJ3VB1C104K
2	3	C24, C25, C26	0.1-µF Multilayer ceramic capacitor	Panasonic or equivalent	ECU-V1H103KBM
3	3	C27, C28, C29	1-nF Multilayer ceramic capacitor	Panasonic or equivalent	ECU-V1H102JCH
4	4	C30, C40, C41, C42	1-µF Multilayer ceramic capacitor	Panasonic or equivalent	ECJ3YB1C105K
5	3	C21, C22, C23	10-µF Multilayer ceramic X5R capacitor	Kemet or equivalent	C1210C106K8PAC
6	2	C43, C44	33-µF Aluminum electrolytic capacitor, size B	Panasonic or equivalent	ECEV1CA100SR
7	9	C31, C32, C33, C34, C35, C36, C37, C38, C39	10-µF Aluminum electrolytic capacitor, size C	Panasonic or equivalent	ECEV1AA330SR
8	1	D1	Lumex SM LED, amber	Lumex or equivalent	CMD15-21VYC/TR8
9	1	D3	Lumex SM LED, green	Lumex or equivalent	CMD15-21VGC/TR8
10	1	D2	40-V, 400-mV Schottky diode (1N5817M)	Diodes, Inc. or equivalent	1N5817M
11	1	D4	5-V VBR transient voltage suppressors SMTZ	General Semiconductor Inc. or equivalent	SMBJ5.0A
12	2	D5, D6	15-V VBR transient voltage suppressors SMTZ	General Semiconductor Inc. or equivalent	SMBJ15A
13	1	J1	3-Terminal screw connector	Lumberg or equivalent	KRMZ3
14	1	J2	2-Terminal screw connector	Lumberg or equivalent	KRMZ2
15	1	J3	26-Pin IDC header	Samtec or equivalent	TSW-113-07-L-D
16	4	J4, W10, W11, W12	2-Position jumper, 0.1 inch spacing	Samtec or equivalent	TSW-102-07-L-S
17	1	J5	4-Pin dual row header	Samtec or equivalent	TSW-104-07-L-D
18	2	J6, J7	80-Pin 0.050 inch centers connector	Samtec	TFM-140-31-S-D-A
19	3	J8. J9, J10	20-Pin IDC header	Samtec or equivalent	TSW-104-07-L-D
20	1	J11	SMA Jack (alternate parts: MaCom #5002-5003-10/ Amphenol #901-144)	Lighthorse Technologies Inc. or equivalent	LTI-SASF54GT
21	1	L1	15-µH Inductor DO1608C-series, Coil Craft	Coil Craft/Inductor Warehouse or equivalent	DO1608C-153
22	5	L2, L3, L4, L5, L6	4.7-µH Inductor DO1608C-series, Coil Craft	Coil Craft/Inductor Warehouse or equivalent	DO1608C-472
23	3	R10, R27, R28	0-Ω, 1/4-W 1206 chip resistor	Panasonic or equivalent	ERJ-8GEY0R00V
24	6	R16, R17, R18, R19, R20, R21	33-Ω, 1/4-W 1206 chip resistor	Panasonic or equivalent	ERJ-8GEYJ330V

Table 2–1. Parts List (Continued)

Item No.	Qty.	Designator	Description	Manufacturer	Part Number
25	2	R4, R24	510-Ω, 1/4-W 1206 chip resistor	Panasonic or equivalent	ERJ-8GEYJ511V
26	1	R5	1-kΩ, 1/4-W, 1206 chip resistor	Panasonic or equivalent	ERJ-8GEYJ102V
27	3	R6, R7, R15	4.7-kΩ, Panasonic EXB-A/CTS 745 Series	Panasonic or equivalent	EXBA10P472J
28	1	R26	4.99-kΩ, 1/4-W 1206 chip resistor	Panasonic or equivalent	ERJ-8ENF4991V
29	8	R1, R2, R3, R8, R9, R12, R13, R14	10-kΩ, 1/4-W 1206 chip resistor	Panasonic or equivalent	ERJ-8ENF1002V
30	1	R25	10-kΩ, Bourns 32X4W series 5T Pot	Bourns or equivalent	3214W-103E
31	1	R30	20-kΩ, 1/4-W 1206 chip resistor	Panasonic or equivalent	ERJ-8ENF2002V
32	1	R23	100-kΩ, 1/4-W 1206 chip resistor	Panasonic or equivalent	ERJ-8ENF1003V
33	2	R11, R29	100-kΩ, Bourns 32X4W series 5T Pot		3214W-104E
34	1	R22	150-kΩ, 1/4-W 1206 chip resistor	Panasonic or equivalent	ERJ-8ENF1503V
35	1	SW1	2-Position, 4-pin SPST slide switch	C&K/CTS or equivalent	TD02H0SK1
36	2	SW2, SW3	4-Position, 8-pin SPST slide switch	C&K/CTS or equivalent	TD04H0SK1
37	7	TP2, TP3, TP4, TP5, TP6, TP7, TP8	Test point, single 0.025 inch pin	Keystone Electronics or equivalent	5000
38	5	TP1, TP9, TP10, TP11, TP12	Turrent terminal test point	Cambion or equivalent	180-7337-02-05
39	2	U1, U2	SYN 4-bit CNT	Texas Instruments Incorporated	SN74HC163D
40	1	U3	Dual D PET FF RS CR	Texas Instruments Incorporated	SN74AHC74D
41	1	U4	Single inverter	Texas Instruments Incorporated	SN74AHC1G04DBVR
42	3	U5, U6, U7	8-Bit parallel in, serial out shift register	Texas Instruments Incorporated	SN74HC166D
43	1	U8	Triple 3-input positive-NAND gate	Texas Instruments Incorporated	SN74ACT10D
44	1	U9	Quad NAND gate	Texas Instruments Incorporated	SN74HC08DR
45	1	U11	DAC8531	Texas Instruments Incorporated	DAC8531E
46	1	U12	Operational amplifier	Texas Instruments Incorporated	OPA350UA
47	1	U13	TPS6734ID	Texas Instruments Incorporated	TPS6734ID

Table 2–1. Parts List (Continued)

Item No.	Qty.	Designator	Description	Manufacturer	Part Number
48	2	U14, U15	5-V Precision voltage reference	Texas Instruments Incorporated	REF02AU
49	1	U16	5-V Thaler precision voltage regulator	Thaler Corporation	VRE3050JS
50	1	U17	Operation amplifier	Texas Instruments Incorporated	OPA177GS
51	1	W13	3-Pin dual row header	Samtec or equivalent	TSW-103-07-L-D
52	9	W2, W3, W4, W5, W6, W7. S8, W9. S14	3-Position jumper, 0.01 inch spacing	Samtec or equivalent	TSW-103-07-LS
53	1	X1	20-MHz Epson programmable oscillator – 8002JC series	Epson or equivalent	SG-8002JC20.0M-PHBS
54	0	DDB	DAC8531 EVM schematic file	Texas Instruments Incorporated	6430514
55	0	PCA	DAC8531 EVM printed-circuit assembly	Texas Instruments Incorporated	6430516
56	1	PWB	DAC8531 EVM family printed wiring board	Texas Instruments Incorporated	6430515

Chapter 3

EVM Operation

This chapter covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

Refer to the DAC8531 data sheet, SBAS192, for information about the serial interface and other related topics.

The EVM board is factory tested and configured in such a way that it should work immediately in stand-alone dc mode with just the slide of a switch.

Topic **Page**

3.1 Stand-Alone DC Mode Test

The stand-alone mode (SAM) test is performed only in dc mode to quickly verify the EVM board for proper functionality. Apply a dc power source of 3.3 V to 5 V with the +supply connecting to J2–2 and referenced to J2–1. The power indicator light, D3, should illuminate (green) once the power is applied.

To put the EVM board into stand-alone (or self-test) mode, the SW1B and SW1A switches must be on. The self-test indicator light, D1, should also illuminate to indicate that the EVM board is now in self-test mode.

3.1.1 Factory Default

The EVM board is set from the factory to the configuration listed in the table below to operate with a single supply and unity gain buffer output through U12.

Table 3–1. Factory Default Jumper Setting

Reference	Jumper Position	Function
W2	1–2	Serial data input from SAM circuit to the DAC data input pin, DIN
W3	1–2	Serial clock from SAM circuit to the DAC serial clock input pin, SCLK
W4	1–2	Frame sync signal from SAM circuit to the DAC sync input pin, SYNC
W5	1–2	SAM frame sync (FS) enabled for 24 SCLK cycles
W6	1–2	SAM data enabled for 24-bit serial data stream
W7	1–2	+Supply rail for U12 (signal conditioning circuit)
W8	1–2	GND for U12
W9	OPEN	EVM power supply is not provided by the DSP starter kit (see Note).
W10	OPEN	U12 is configured for unity gain.
W11	OPEN	U12 is configured for unity gain.
W12	OPEN	Bipolar supply is not selected.
W13	3–4	DAC output signal is conditioned and directed to J11, J3–1, and TP1 output terminals.
W14	1–2	Adjustable onboard reference voltage is selected.
J4	OPEN	Enable parallel load of data inputs for U5, U6, and U7

Note: Jumper must be removed if external power is applied to avoid damaging the DSP Starter Kit.

3.1.2 Test Mode Operation

Briefly mentioned earlier, the switch bank SW1 provides control for the stand-alone mode of operation. Switch SW1B controls the start and stop of the SAM serial clock and SW1A controls the go signal for the SAM circuitry. When both switches are on, the self-test indicator light (yellow) turns on.

Switch banks SW2 and SW3 provides the two control bits and the six MSB data bits for the 16-bit DAC. SW2A and SW2B is the control bit generator, which allows the DAC to be programmed into four separate modes of operation, see Table 3–2. SW2A and SW2B maps out to PD1 (DB17) and PD0 (DB16) respectively of the DAC data input register (16-bit version). Figure 3–1 shows

the complete mapping of the respective switches to the data input register for either DAC8531 or DAC8501. SW3A and SW3B maps out to PD1 (DB13) and PD0 (DB12) respectively of the DAC data input register (12-bit version). Figure 3–2 shows it for the 12-bit version (DAC7512/13).

Table 3–2. Modes of Operation for the DAC8531

PD1	PD0	Operating Mode
0	0	Normal operation
0	1	Power down mode with output of 1 kΩ to GND
1	0	Power down mode with output of 100 kΩ to GND
1	1	High-Z

Figure 3–1. Switch SW2 and SW3 Mapping to the Data Input Register (16-Bit Version)

DB23 DB0

X	X	X	X	X	X	PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	SW2 A	SW2 B	SW2 C	SW2 D	SW3 A	SW3 B	SW3 C	SW3 D	0	0	0	0	0	0	0	0	0	0
						CONTROL BITS		DATA BITS															

Since there are only six switches (six MSBs) available to control the data bits, the maximum value that the data bits can be programmed to is limited to 0xFC00, which does not exactly match the full-scale range of the 16-bit DACs. This is intended purely for testing purposes and is done to limit the component count and save space, but still effectively shows that the DAC EVM is properly functioning.

For the 12-bit version, there are only two bits available to control the data bits but is sufficient enough to check its functionality.

Figure 3–2. Switch SW3 Mapping to the Data Input Register (12-Bit Version)

DB23 DB0

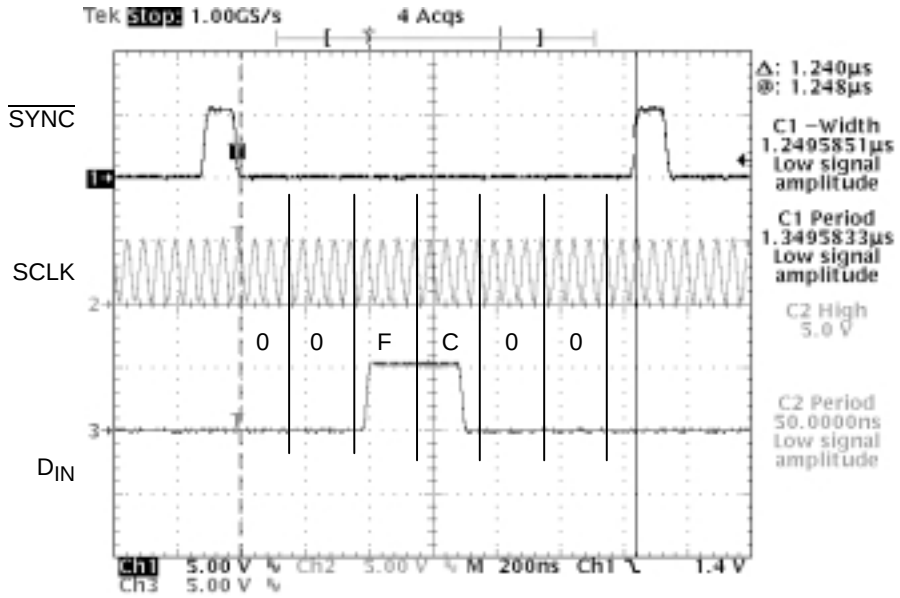
X	X	X	X	X	X	D17	D16	D15	D14	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	SW2 A	SW2 B	SW2 C	SW2 D	SW3 A	SW3 B	SW3 C	SW3 D	0	0	0	0	0	0	0	0	0	0
						Not used for 12-bit version				CONTROL BITS		DATA BITS											

In general, the 16-bit version and the 12-bit version are identical in operation with the exception of the number of SCLK periods and the size of their shift and data registers. With this in mind, this users guide will focus primarily on the 16-bit DAC operation only.

The self-test mode only provides a 20-MHz SCLK for serial data transfers and emulates a DSP standard serial interface. The write sequence is initiated by asserting the SYNC line low and is held low for a period of 25 SCLKs. The serial data is clocked into the 24-bit shift register, MSB first from the D_{IN} line, on the falling edge of SCLK. The last data bit is clocked in on the 24th falling edge (or 16th falling edge for a 12-bit DAC) of SCLK and the DAC is updated. At this point, the SYNC line is disabled for three SCLK cycles and the write sequence

is again repeated. The timing diagram of the write sequence is shown in Figure 3–3.

Figure 3–3. Write Sequence Timing Diagram



The output of the DAC can be displayed with the use of an oscilloscope by probing either of the output terminals J11, J3-1, and TP1. Figure 3–4 shows the normal output for the first power up of the EVM from the factory (default configuration). This figure shows the zero-scale output of the DAC. Channel 1 presents the DAC output through a unity gain signal conditioning op-amp, U12. Channel 2 is the DAC output straight out of U11, pin 4, for comparison.

Figure 3–4. Zero-Scale Output

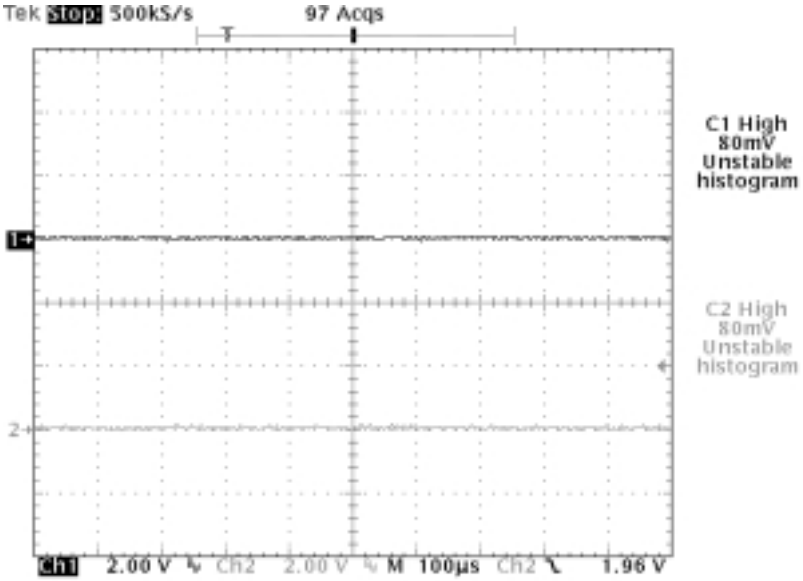


Figure 3–5 shows the half-scale output of the DAC as the switches are configured to send the data of 0x008000 to the DAC. Channel 1 presents the

DAC output through a unity gain signal conditioning op-amp, U12, and channel 2 is the DAC output straight out of U11, pin 4, for comparison.

Figure 3–5. Half-Scale Output

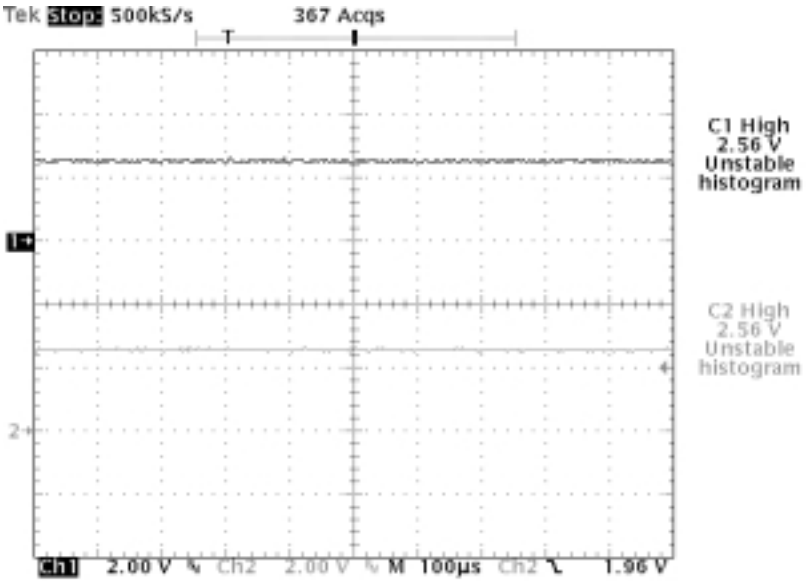
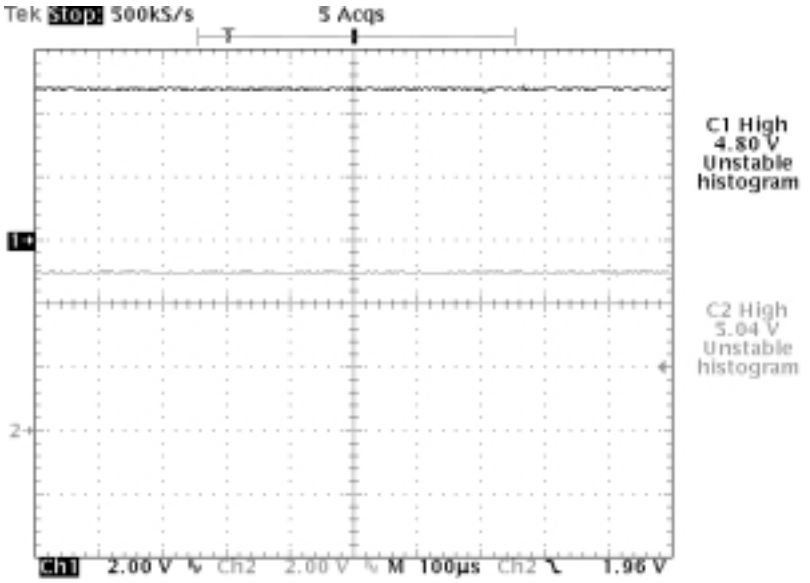


Figure 3–6 shows the full-scale output of the DAC as the switches are configured to send the data of 0x00FC00 to the DAC. Channel 1 presents the DAC output through a unity gain signal conditioning op-amp, U12, and channel 2 is the DAC output straight out of U11, pin 4, for comparison.

Figure 3–6. Full-Scale Output



3.2 Host Processor Interface

This section describes the operation using a host processor, such as a DSP or a microcontroller, to interface with the EVM. The daughterboard connectors,

J6 and J7, are incorporated into the EVM for direct plug-in to a DSP development board or starter kit that supports a common connector interface. However, J8, J9, and J10 headers are provided to allow the user to customize their interface cable to suit their system configuration. If the DSP development board or starter kit is used to interface with the EVM board through the common connector, then supply power to the EVM must be selected through W9. A voltage supply of 5 V or 3.3 V can be selected depending on the overall system's requirement.

When operating the EVM in the host processor mode of testing, make sure to slide the switches, SW1A and SW1B, to the off position. This will ensure that the clock and all other digital devices onboard are idled and will not emit switching noise or any other noise related to the digital parts onboard.

3.2.1 Signal Interface

There are three signals that are essential in the successful operation of the DAC, which will be covered in detail in this section. These three serial interface signals are SCLK, $\overline{\text{SYNC}}$, and D_{IN}, and are compatible with SPI™, QSPI™, Microwire™, and most DSP serial interfaces.

3.2.1.1 Serial Clock (SCLK)

The serial input clock, SCLK, has a maximum frequency of 30 MHz to be compatible with high-speed processors. The DSP development board or starter kit when mated with the EVM through the daughterboard connector must provide the external clock source.

The external clock source signal is fed through J7 pin 33 and is routed to the DAC, U11, pin 6, through W3 by shorting pins 2 and 3. The header, J10, pin 3 can also be used to feed the external clock source when using another type of processor or microcontroller that does not support the common connector scheme, but supports the serial interface protocol.

3.2.1.2 Synchronization Signal ($\overline{\text{SYNC}}$)

The $\overline{\text{SYNC}}$ signal synchronizes the stream of data with the serial clock and marks the start of the write sequence. When the $\overline{\text{SYNC}}$ line is brought low, the first falling edge of SCLK is the start of the valid data. The $\overline{\text{SYNC}}$ line must be held low for at least 24 SCLK cycles for the write sequence to complete, and the DAC is updated on the 24th falling edge of SCLK.

If the $\overline{\text{SYNC}}$ line is brought high before the 24th falling edge of SCLK, the shift register is reset and the write sequence is terminated or becomes invalid. The DAC is not updated as well. In essence, this can serve as an interrupt signal to the DAC.

The external $\overline{\text{SYNC}}$ signal is fed through J7, pin 35, and is routed to the DAC, U11 pin 5, through W4 by shorting pins 2 and 3. The header, J10, pin 11 can also be used to feed the external $\overline{\text{SYNC}}$ signal when using another type of processor or microcontroller that does not support the common connector scheme, but supports the serial interface protocol.

For the lowest power operation of the device, the $\overline{\text{SYNC}}$ line should be idled low between write sequences because the $\overline{\text{SYNC}}$ buffer draws more current when the $\overline{\text{SYNC}}$ signal is high than it does when it is low. Just before another write sequence is desired, the $\overline{\text{SYNC}}$ line must be brought high for a minimum of 33 ns so that a falling edge of the $\overline{\text{SYNC}}$ can initiate the next write sequence.

3.2.1.3 Serial Data Input (D_{IN})

The serial data input is clocked into the 24-bit shift register from the D_{IN} line on the falling edge of SCLK. The data is shifted in starting with the MSB and only 18 of the 24 bits are valid. The first 6 MSB are ignored and bits 17 (PD1) and 16 (PD0) are extracted to determine the DACs mode of operation (see Table 3–2). The remaining 16 bits are data bits which are transferred to the DAC register on the 24th falling edge of SCLK.

The external D_{IN} signal is fed through J7, pin 36, and is routed to the DAC, U11, pin 7, through W2 by shorting pins 2 and 3. The header, J10, pin 7, can also be used to feed the external D_{IN} signal when using another type of processor or microcontroller that does not support the common connector scheme, but supports the serial interface protocol.

3.2.2 Host Processor Operation

The host processor basically drives the DAC, so the DACs proper operation depends on the successful configuration between the host processor and the EVM board, and of course a properly written code to run the DAC.

The EVM incorporates four different options for the DAC output through an operational amplifier, U12. This requires some jumper setting configuration, particularly around the op-amp (U12) circuitry, and other required equipment needed. Each option is discussed individually in the next subsections.

Regardless, the raw output of the DAC can be probed through W13 pin 2 so that it can be compared with the output of U12 if necessary. The output terminals J11, J3-1 and TP1 can be used to monitor the raw output of the DAC by shorting pins 1 and 2 of W13.

3.2.2.1 Unity Gain Output (Default Mode)

The EVM is shipped with the unity-gain output as its default configuration mode. The buffered output should closely match the raw output of the DAC with maybe some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match their desired wave shape by simply desoldering R3 and C27 and replacing it with the desired values. Also R3 and C27 can be eliminated altogether and a 0-Ω resistor soldered in replacement of R3, if desired.

Table 3–3 shows the jumper settings relating to the unity gain configuration of the output buffer.

Table 3–3. Unity Gain Output Jumper Settings

Reference	Jumper Setting	Function
W7	1–2	+ Rail of the op-amp supplied by V_{CCA}
W8	1–2	– Rail of the op-amp tied to analog GND
W10	Open	Disconnect V_{REF} from negative input of op-amp
W11	Open	Disconnect negative input of op-amp from GND
W13	3–4	Buffered output of DAC is channeled to the output terminals

3.2.2.2 Output Gain of Two

If the EVM is operating at 3.3 V and there is a need for the DAC output to maintain a 5-V peak level, than this configuration can be implemented. Table 3–4 shows the proper jumper settings for a 2× gain output of the DAC.

Table 3–4. Gain of Two Output Jumper Settings

Reference	Jumper Setting	Function
W7	2–3	Select 5 V for the positive rail supply of the op-amp if W12 is closed
W8	1–2	Negative rail of the op-amp tied to analog GND
W10	Open	Disconnect V_{REF} from negative input of op-amp
W11	Close	Provides a 2× gain output for the op-amp
W12	Close	Supplies the constant 5 V to the positive rail of the op-amp if W7, pins 2 and 3, are shorted together
W13	3–4	Buffered output of DAC is channeled to the output terminals

The reference voltage must be set such that the output voltage range of the DAC does not exceed the positive rail supply of the op-amp, U12. Otherwise the output of the op-amp, U12, will be clipped.

V_{CCA} can be used also to supply the positive rail of the op-amp by shorting pins 1 and 2 of W7. With this configuration, the effective output of the op-amp will be at a maximum of V_{CCA}. The reference voltage must also be set to $V_{CCA}/2$.

3.2.2.3 Capacitive Load Driving

Another output configuration option is to drive a wide range of capacitive loads. However, all op-amps under certain conditions may become unstable depending on the op-amp configuration, gain, and load value. These are just a few factors that can affect op-amp stability performance and should be considered during implementation.

In unity gain, the OPA350 op-amp, U12, performs very well with very large capacitive loads. Increasing the gain enhances the amplifier’s ability to drive even more capacitance, and by adding a load resistor improves the capacitive load drive capability. Table 3–5 shows the jumper setting configuration for a capacitive load drive.

Table 3–5. Capacitive Load Drive Output Jumper Settings

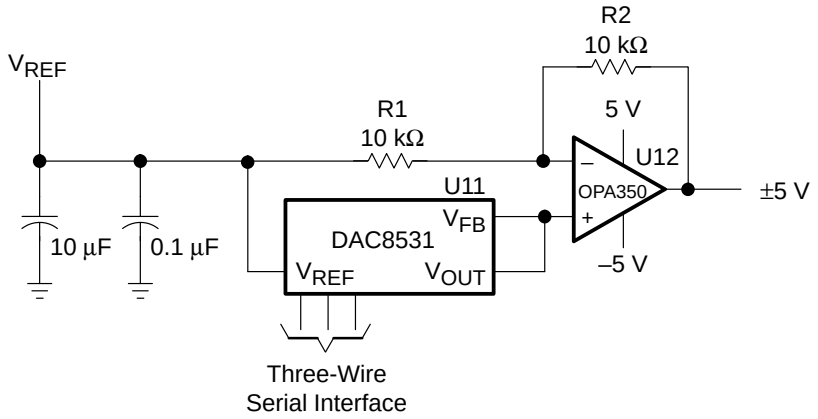
Reference	Jumper Setting	Function
W7	2–3	Select 5 V for the positive rail supply of the op-amp if W12 is closed
W8	1–2	Negative rail of the op-amp tied to analog GND
W10	Open	Disconnect V_{REF} from negative input of op-amp
W11	Open (see Note)	Disconnect R12 (see Note)
W12	Close	Supplies the constant 5 V to the positive rail of the op-amp if W7, pins 2 and 3, are shorted together
W13	5–6	Buffered output of DAC is channeled to the output terminals

Note: If there is a need to incrementally adjust the capacitive load output, replace R12 with a capacitor with the desired capacitance value and close W11.

3.2.3 Bipolar Operation Using the DAC8531

Although the DAC8531 has been designed for single-supply operation, the bipolar output of operation is implemented using the circuit shown in Figure 3–7. The output of the circuit is an output voltage range of $\pm V_{REF}$. The rail-to-rail operation at the amplifier output is achievable using an OPA350 as the output amplifier.

Figure 3–7. Bipolar Operation With the DAC8531



The EVM requires an additional ±15-V power supply to provide the supply rails for the OPA177 op-amp, U17. The ±15-V supply is provided through the J1 connector of the EVM. The 15 V is attached to J1-3 terminal and the –15 V is attached to J1-1 terminal. The ±15-V supplies are referenced to J1-2 terminal.

The OPA177 op-amp is specifically used to generate the –5-V supply voltage for the negative rail of the OPA350 op-amp circuit, U12.

The bipolar configuration is accomplished by following the correct jumper settings according to Table 3–6.

Table 3–6. Bipolar Operation Output Jumper Settings

Reference	Jumper Setting	Function
W7	2–3	Select 5 V for the positive rail supply of U12 if W12 is closed
W8	2–3	Select –5 V for the negative supply rail of U12 if W12 is closed
W10	Closed	Connect V_{REF} to the negative input of op-amp for negative biasing
W11	Open	Disconnect R12
W12	Close	Supplies the constant 5 V to the positive rail of U12 and is also fed into the negative input of U17 to generate an output voltage of –5 V.
W13	3–4	Buffered output of DAC is channeled to the output terminals

An example in Figure 3–8 shows the sinusoid signal in channel 1 being amplified within the range of $\pm V_{REF}$ shown in channel 2. The reference voltage, V_{REF}, is set to 5 V, which is then supplied to the negative input of U12 to bias the circuit to its negative rail. This provides an output of ±5 V with 0000h corresponding to a –5-V output and FFFFh corresponding to 5-V output.

The output voltage for any input code can be calculated as follows:

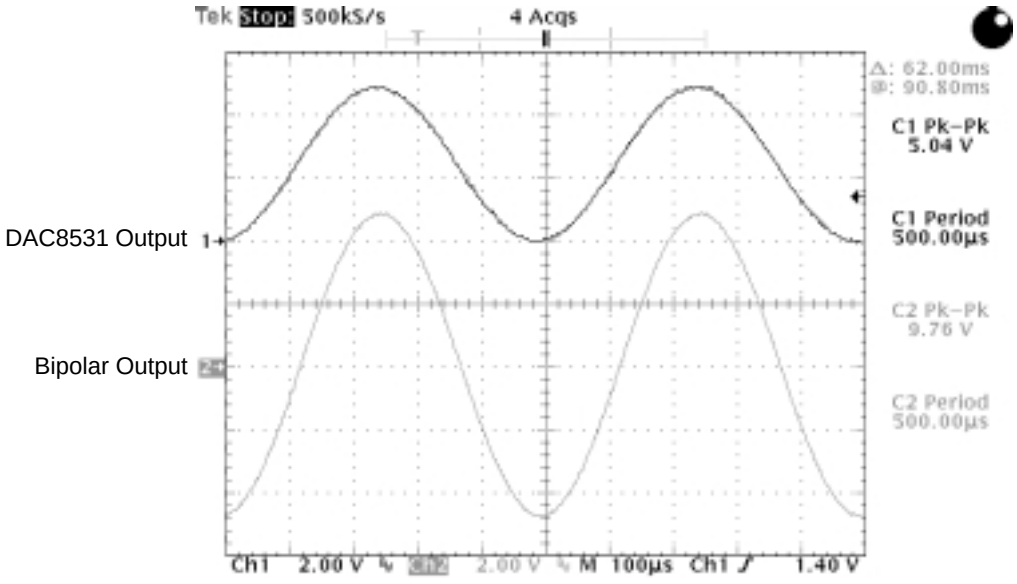
$$V_O = \left[V_{REF} \times \left(\frac{D}{65536} \right) \times \left(\frac{R1 + R2}{R1} \right) - VREF \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 – 65536).

With V_{REF} = 5 V, R1 = R2 = 10 kΩ:

$$V_O = \left(\frac{10 \times D}{65536} \right) - 5\ V$$

Figure 3–8. DAC8531 Bipolar Output of Operation



Similarly, adjusting the V_{REF} voltage to any desired value less than 5 V produces a voltage output range of $\pm V_{REF}$.

3.3 Jumper Setting

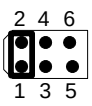
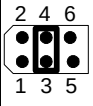
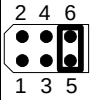
The table below lists the function of each jumper on the EVM.

Table 3–7. Jumper Setting Function

Reference	Jumper Setting	Function
W2		Enables the stand-alone mode SDI to route to the DAC8531 D_{IN} pin.
		Enables the user interface SDI to route to the DAC8531 D_{IN} pin
W3		Enables the stand-alone mode SCLK to route to the DAC8531 SCLK pin.
		Enables the user interface SCLK to route to the DAC8531 SCLK pin.
W4		Enables the stand-alone mode FS to route to the DAC8531 SYNC pin.
		Enables the user interface FS to route to the DAC8531 SYNC pin.
W5		Generates a SYNC signal for stand-alone mode after 24 SCLK cycles (default mode).
		Generates a SYNC signal for stand-alone mode after 16 SCLK cycles (used only for 12-bit DACs described in table 1–1).
W6		Provides 24-bit serial data for stand-alone mode when DAC8531 or DAC8501 is installed in the EVM.
		Provides 16-bit serial data for stand-alone mode when DAC7512 or DAC7513 is installed in the EVM.
W7		Supplies V_{CCA} to the positive rail of U12.
		Supplies a constant 5 V to the positive rail of U12 provided W12 is closed.
W8		Ties the negative rail of U12 to AGND.
		Supplies a constant –5 V to the negative rail of U12 provided W12 is closed and a ±15 V supply is applied to the EVM board through J1 terminal.
W9		EVM board is powered by a 3.3-V supply from the DSP through a common connector if a DSK is used. Read caution in Section 1.2.1 when setting jumper.
		EVM board is powered by a 5-V supply from the DSP through a common connector if a DSK is used. Read caution in Section 1.2.1 when setting jumper.

Legend:  Indicates the corresponding pins that are shorted or closed.

Table 3–7. Jumper Setting Function (Continued)

Reference	Jumper Setting	Function
W10		Disconnects V_{REF} from the negative input terminal of U12.
		Allows V_{REF} to be routed to the negative input terminal of U12 for bipolar operation.
W11		Disconnect the negative terminal of U12 to AGND.
		Allow a 2× gain output in unipolar mode.
W12		Disconnects 12-V supply to U15 or R22 and R23 voltage divider circuit.
		Connects 12-V supply to U15 or R22 and R23 voltage divider circuit.
W13		Routes the raw output of the DAC8531 to the TP1 test point, J3-1, and J11 output terminals.
		Routes the output of U12 to the TP1 test point, J3-1 and J11 output terminals. Used for unipolar and bipolar modes of operation.
		Routes the output of U12 to the TP1 test point, J3-1 and J11 output terminals. Used for capacitive load driving.
W14		Routes the adjustable onboard reference voltage to the DAC8531 V_{REF} pin.
		Routes the adjustable user supplied reference voltage to the DAC8531 V_{REF} pin.

Legend:  Indicates the corresponding pins that are shorted or closed.

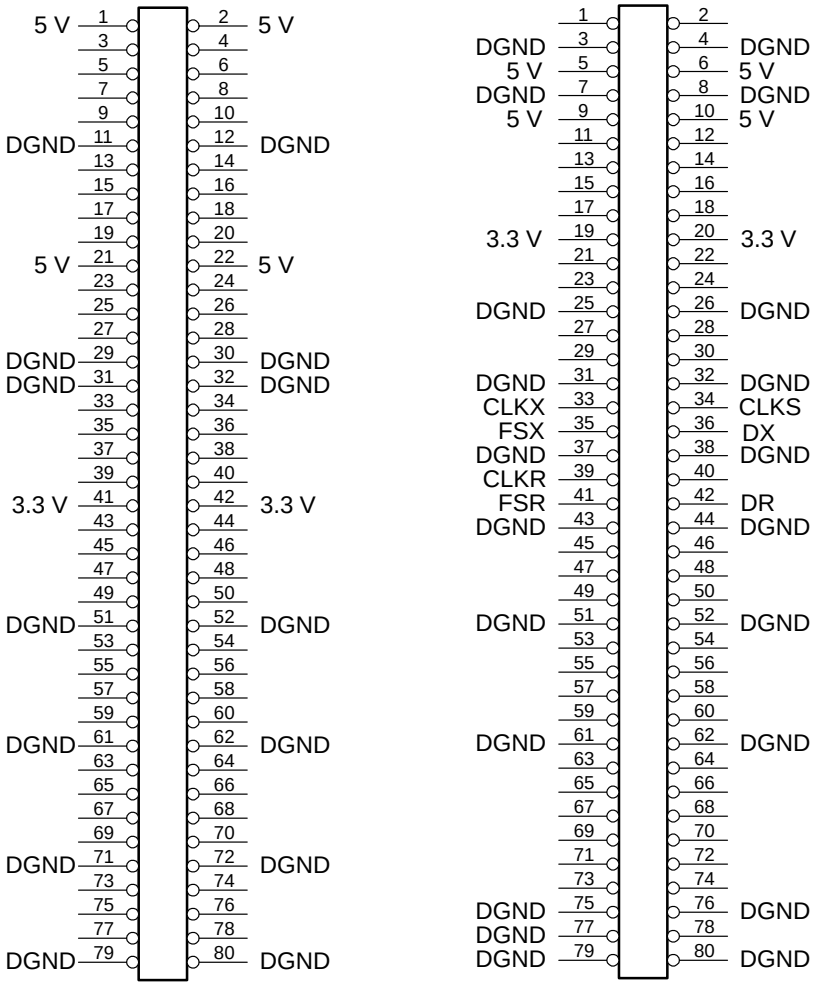
3.4 I/O Signal Mapping

Figure 3–9 and Figure 3–10 shows the I/O signals with respect to their connectors/headers.

3.4.1 Daughterboard Connector Signal Mapping

Figure 3–9 describes the essential signals from the DSK boards that are brought out through the common connectors which mates with the daughterboard connectors J6 and J7.

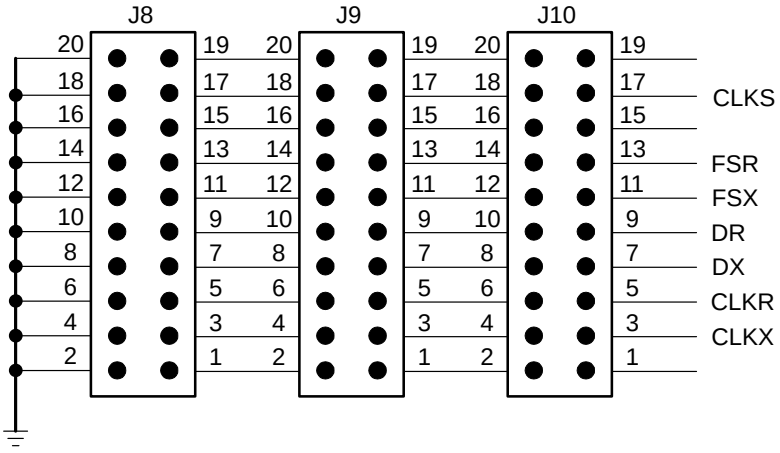
Figure 3–9. Daughterboard Connector Signal Mapping



3.4.2 DSP and Microcontroller Connector Signal Mapping

Figure 3–10 describes the essential signals for the serial interface using a host processor DSP or microcontroller. Basically, three headers J8, J9, and J10 are used so that the user can build a customized 20-pin ribbon cable to plug into the J9 header and easily route the signals using the wire wrap and jumper method. This can be achieve by properly identifying the signals from the 20-pin custom cable and connecting each to the corresponding signals indicated in the odd-numbered pins of header J10.

Figure 3–10. DSP and Microcontroller Signal Mapping



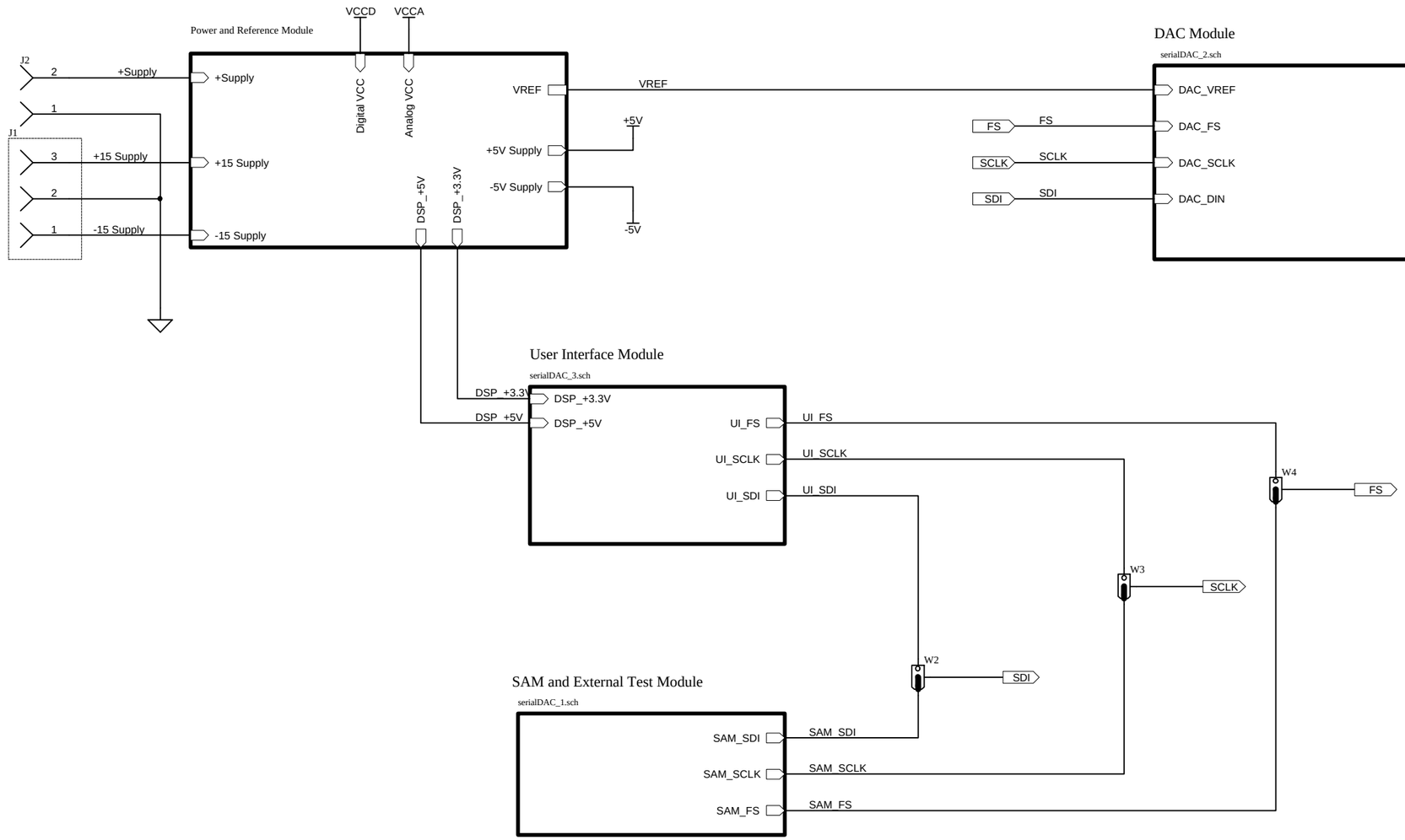
3.4.3 DAC Output Connector

The DAC output is routed to the J3 pin 1 header as well as the J11 SMA jack.

3.5 Schematic Diagram

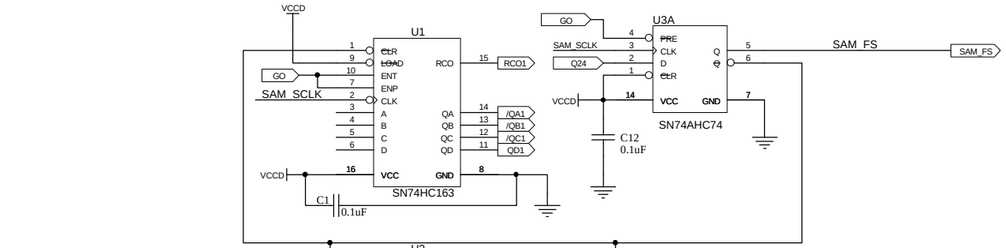
The following pages show the complete schematic diagram of the DAC8531 evaluation module board.

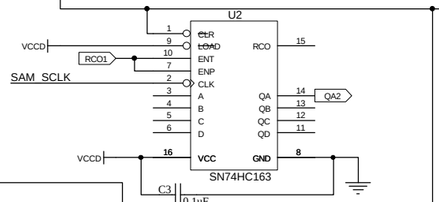
Revision History		
REV	ECN Number	Approved

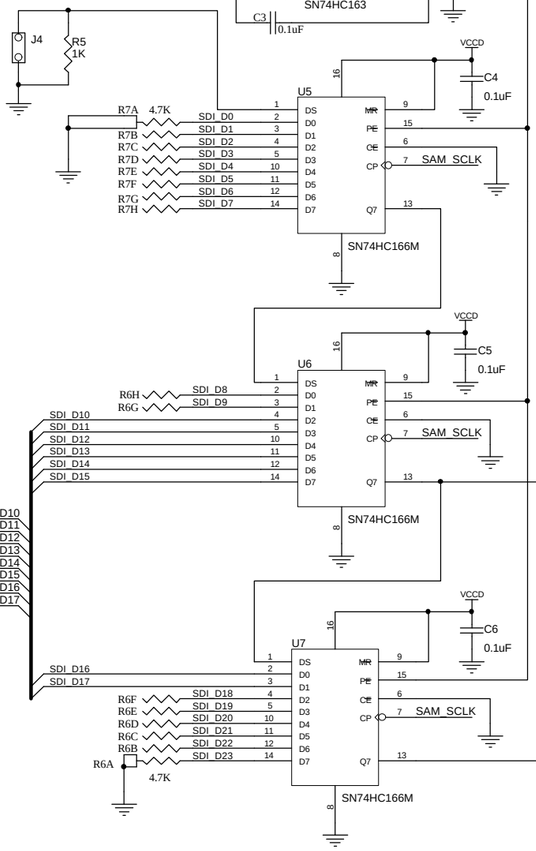


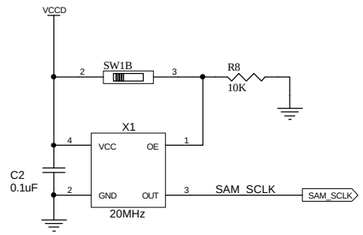
	12500 TI Blvd. Dallas, Texas 75243		
Title: DAC8531 EVM Block Diagram			
Engineer: Joselito Parguian			
Drawn By: Joselito Parguian	SIZE: B	DATE: 19-Apr-2001	REV: B
FILE: Serial DACevm.ddb	6430514		SHEET: 1 OF: 5

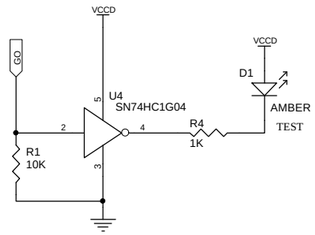
Revision History		
REV	ECN Number	Approved

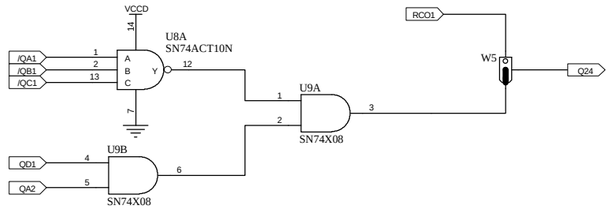


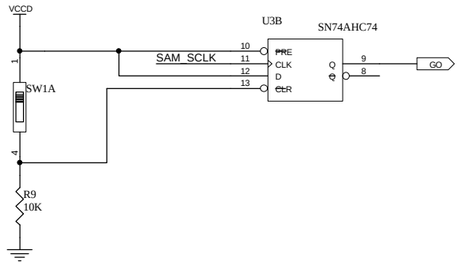


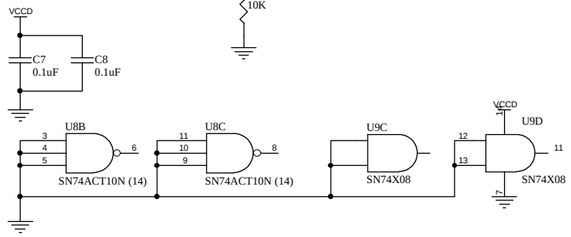












Engineer: Joselito Parguian	Title: DAC8531 EVM SAM and External Test Module		
Drawn By: Joselito Parguian	SIZE: B	DATE: 19-Apr-2001	REV: B
FILE: Serial EVM.prj	6430514		SHEET: 2 OF: 5

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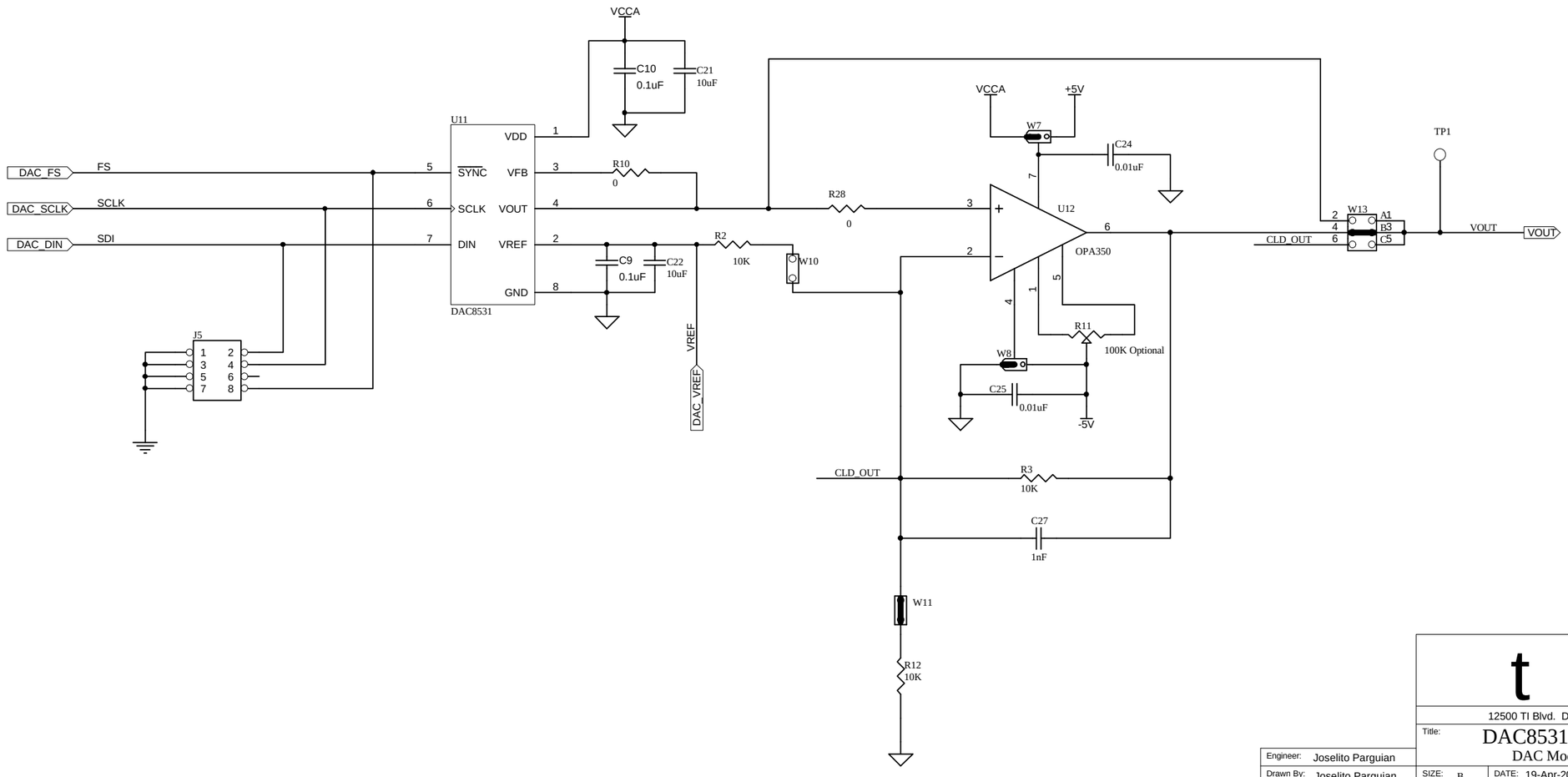
Revision History		
REV	ECN Number	Approved



Engineer: Joselito Parguian			
Drawn By: Joselito Parguian	SIZE: B	DATE: 19-Apr-2001	REV: B
FILE: Serial EVM.prj	6430514		SHEET: 3 OF: 5

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Title: DAC8531 EVM
DAC Module

TMS320 Common Connector Interface

Note:
Switch ON = 1

16-bit Control Bits

16-bit MSB

12-bit Control Bits

12-bit MSB

VCCD

SW2A SW2B SW2C SW2D SW3A SW3B SW3C SW3D

R15A R15B R15C R15D R15E R15F R15G R15H

SDI_D10 SDI_D11 SDI_D12 SDI_D13 SDI_D14 SDI_D15 SDI_D16 SDI_D17

UI_FS UI_SCLK UI_SDI

R16 R17 R18 33

R19 R20 R21 NI

FSX CLKX DX

FSR CLKR DR

DSP_+5V DSP_+3.3V

J6 J7 TFM-140

TP2 TP3

CLKX FSX CLKR FSR

CLKS DX DR

J8 J9 J10

CLKS FSR FSX DR DX CLKR CLKX

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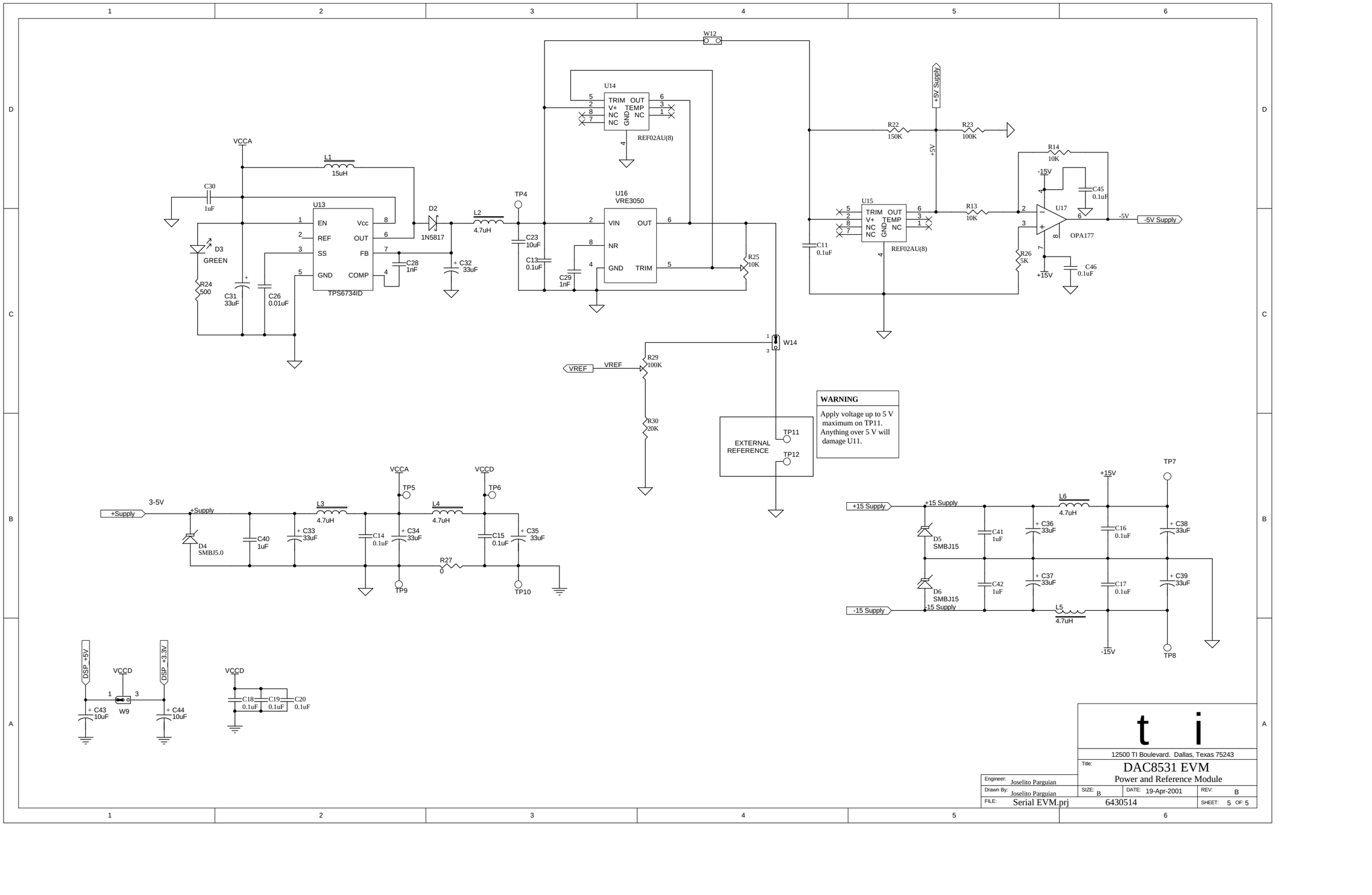
Title: DAC8531 EVM
User Interface Module

Engineer: Joselito Parguian
Drawn By: Joselito Parguian
FILE: Serial EVM.prj

SIZE: B
DATE: 19-Apr-2001
REV: B
6430514
SHEET: 4 OF: 5


W12
U14
TRIM OUT
V+ TEMP
NC GND NC
NC
REF02AU(8)
+5V Supply
R22
150K
R23
100K
+5V
R14
10K
-15V
C45
0.1uF
U15
REF02AU(8)
R13
10K
U17
OPA177
-5V
-5V Supply
C11
0.1uF
R26
5K
C46
0.1uF
+15V
VCCA
L1
15uH
C30
1uF
U13
EN
Vcc
REF
OUT
SS
FB
GND
COMP
TPS6734ID
D3
GREEN
R24
500
C31
33uF
C26
0.01uF
C28
1nF
D2
1N5817
L2
4.7uH
TP4
U16
VRE3050
VIN
OUT
NR
GND
TRIM
C23
10uF
C13
0.1uF
C29
1nF
R25
10K
W14
VREF
R29
100K
R30
20K
EXTERNAL
REFERENCE
TP11
TP12
WARNING
Apply voltage up to 5 V maximum on TP11. Anything over 5 V will damage U11.
VCCA
VCCD
TP5
TP6
3-5V
+Supply
L3
4.7uH
L4
4.7uH
D4
SMBJ5.0
C40
1uF
C33
33uF
C14
0.1uF
C34
33uF
C15
0.1uF
C35
33uF
R27
0
TP9
TP10
TP7
+15V
+15 Supply
L6
4.7uH
D5
SMBJ15
C41
1uF
C36
33uF
C16
0.1uF
C38
33uF
D6
SMBJ15
C42
1uF
C37
33uF
C17
0.1uF
C39
33uF
-15 Supply
L5
4.7uH
-15V
TP8
DSP +5V
DSP +3.3V
VCCD
W9
C43
10uF
C44
10uF
C18
0.1uF
C19
0.1uF
C20
0.1uF
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12500 TI Boulevard. Dallas, Texas 75243
Title:
DAC8531 EVM
Power and Reference Module
Engineer: Joselito Parguian
Drawn By: Joselito Parguian
SIZE: B
DATE: 19-Apr-2001
REV: B
FILE: Serial EVM.prj
6430514
SHEET: 5 OF: 5

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