Analog Engineer's Circuit

High-Voltage Gain Stage Design Circuit for DAC81401

Design Goals

DAC V_{OUT}			Gain Stage		External Supply	
Range	**MIN**	**MAX**	**MIN**	**MAX**	**HV+**	**HV–**
0 V–20 V	0 V	20 V	0 V	80 V	0 V	82 V
±10 V	–10 V	+10 V	–40 V	+40 V	–41 V	+41 V

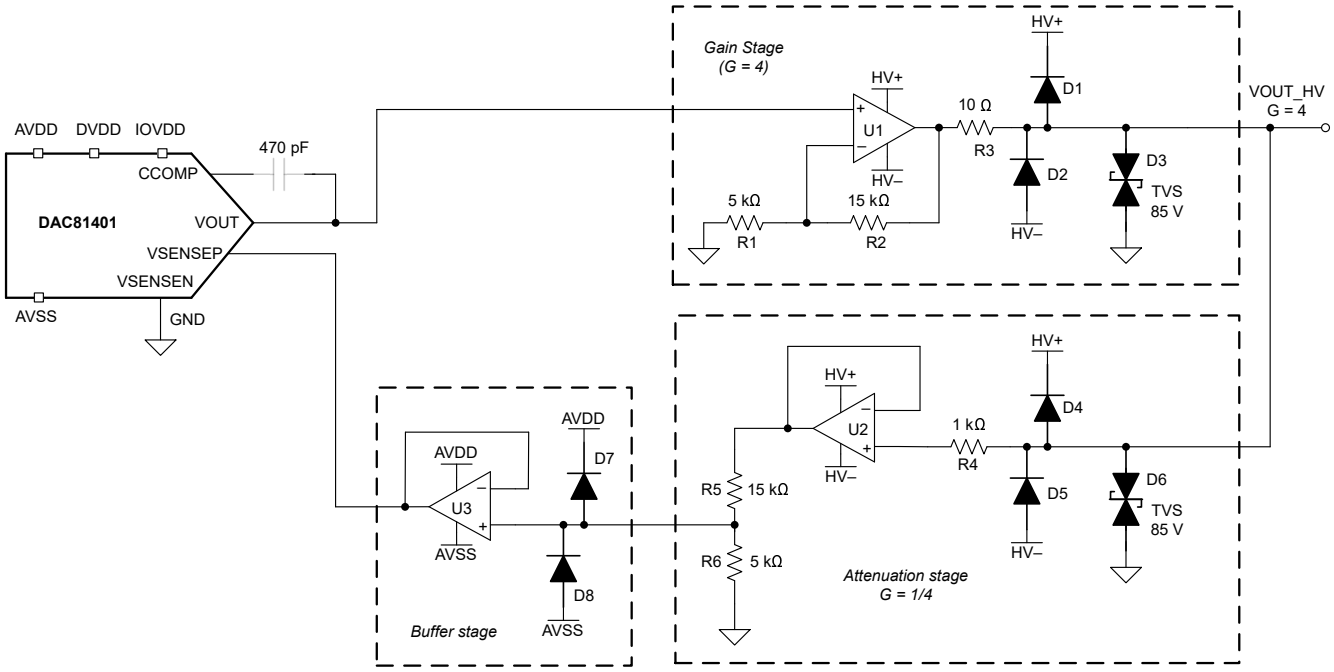
Objective: Design a high-voltage gain (4 ×) stage in a closed loop system for the DAC81401.

Design Description

This high-voltage gain stage design circuit for the DAC81401 is capable of providing output voltage ±40 V or 0 V to 80 V. This system design consists of four blocks as listed below and shown in *High-Voltage Gain Stage Circuit Block Diagram*.

- DAC81401 output stage
- High-voltage gain (4 ×) stage with protection diodes and TVS
- Attenuation stage
- Buffer stage with protection diodes

The DAC81401 output voltage is amplified by the gain stage by a factor of 4. The gain stage output is attenuated by the attenuation stage by a factor of 4. This attenuated output voltage is buffered and connected to the VSENSEP pin of the DAC81401 to close the loop.



High-Voltage Gain Stage Circuit Block Diagram

Key Components

- U1,U2 – OPA593: 85-V, low offset, low noise, 10 MHz, 250-mA output current precision operational amplifier
- U3 – OPA189: 36-V, low offset, low drift, low noise, 14-MHz precision operational amplifier
- D1, D2, D4, D5, D7, D8 – Schottky diode 100 V, 150 mA, 0.7-V forward voltage, fast switching
- D3, D6 – 85-V standoff voltage, high current, bidirectional TVS
- R1, R2 – low temperature coefficient and high accuracy (< 0.01%) thin film resistors
- R5, R6 – low temperature coefficient and high accuracy (< 0.01%) thin film resistors
- R3, R4 – normal thin film resistor

DAC81401 Output Stage

The DAC81401 output (V_{OUT}) is capable of providing from –20 V to +40 V. However, some applications (test and measurement, factory automation and control) requires even higher voltages. The high-voltage gain stage design is useful in these applications.

V_{OUT} is expressed by using the next two equations.

For unipolar mode:

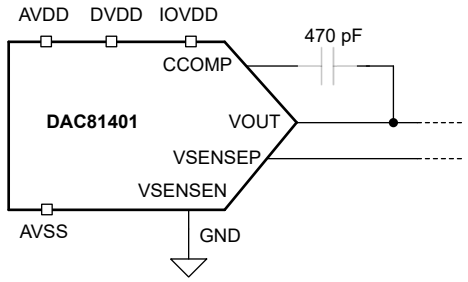
$$V_{OUT} = V_{REFIO} \times GAIN \times \frac{CODE}{2^N}$$

For bipolar mode:

$$V_{OUT} = V_{REFIO} \times GAIN \times \frac{CODE}{2^N} - GAIN \times \frac{V_{REFIO}}{2^N}$$

where:

- CODE is the decimal equivalent of the code loaded to the DAC register
- N is the bits of resolution; 16-bits for DAC81401
- V_{REFIO} = 2.5 V is the reference voltage (internal or external)
- GAIN is the gain factor for each of the DAC814101 output voltage range, GAIN = 8 is recommended for this design



DAC81401 Output Stage Block Diagram

Compensation Capacitor

A 470-pF compensation capacitor is optional and the CCOMP pin can be left floating. This compensation capacitor is only needed if the load capacitor at the DAC81401 VOUT node is greater than 2 nF.

Adding the compensation capacitor increases the output settling time and slows the output voltage transient.

Gain Stage

The gain stage amplifies the DAC output voltage by 4 ×. This gain stage utilizes the OPA593 (U1) which supports an output voltage range of 85 V for single supply or ±42.5 V for bipolar supply. At the gain stage output (VOUT_HV), 0 V to 80 V or ±40 V can be obtained by programming the DAC output range to, 0 V to 20 V or ±10 V, respectively. For a given gain stage output (VOUT_HV), the DAC output can be calculated with the next two equations.

For unipolar mode:

$$\mathrm{CODE} = \frac{\left(\frac{\mathrm{VOUT\_HV}}{4}\right) \times 2^{\mathrm{N}}}{\mathrm{V_{REFIO}} \times \mathrm{GAIN}}$$

For bipolar mode:

$$\mathrm{CODE} = \frac{\left(\frac{\mathrm{VOUT\_HV}}{4} + \mathrm{GAIN} \times \frac{\mathrm{V_{REFIO}}}{2^{\mathrm{N}}}\right) \times 2^{\mathrm{N}}}{\mathrm{V_{REFIO}} \times \mathrm{GAIN}}$$

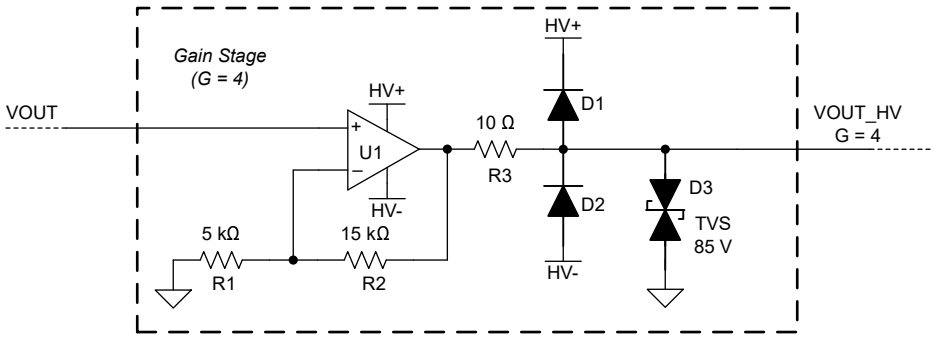
And for a given DC code, the gain stage output voltage can be calculated with the following equations.

For unipolar mode:

$$\mathrm{VOUT\_HV} = 4 \times \left(\mathrm{V_{REFIO}} \times \mathrm{GAIN} \times \frac{\mathrm{CODE}}{2^{\mathrm{N}}}\right)$$

For bipolar mode:

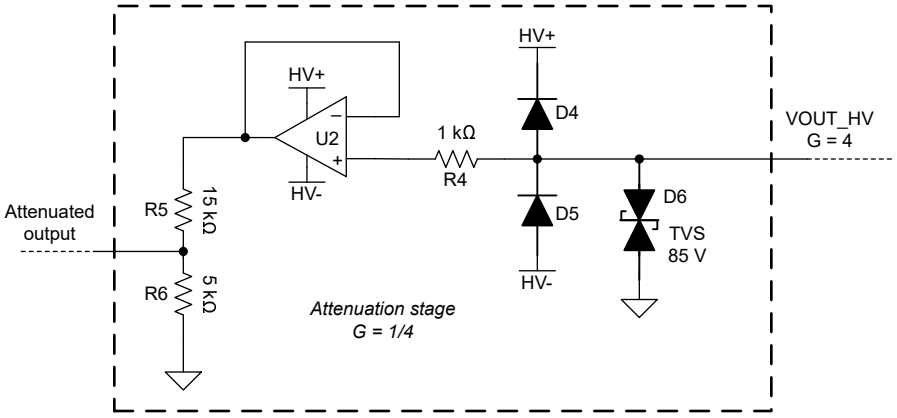
$$\mathrm{VOUT\_HV} = 4 \times \left(\mathrm{V_{REFIO}} \times \mathrm{GAIN} \times \frac{\mathrm{CODE}}{2^{\mathrm{N}}} - \mathrm{GAIN} \times \frac{\mathrm{V_{REFIO}}}{2^{\mathrm{N}}}\right)$$



Gain Stage Block Diagram

Attenuation Stage

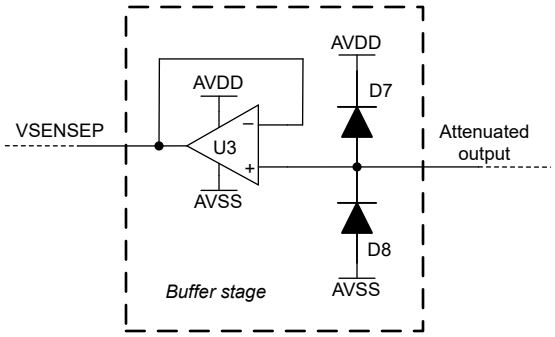
To avoid any unintended voltage drop due to load current (IR drop), VOUT and VSENSEP are connected close to the load, and the voltage value for the VSENSEP and VOUT is same. To remove the IR drop, the gain stage output voltage is – first buffered (U2) and then attenuated by a factor of 4 with resistor divider R5 and R6.



Attenuation Stage Block Diagram

Buffer Stage

The VSENSEP pin has an input impedance of about 50 kΩ and the resistor divider voltage cannot be connected directly or loading causes a voltage error. This voltage output is first buffered (U3) and then connected to the VSENSEP pin of DAC81401 to close the internal feedback loop with VOUT.



Buffer Stage Block Diagram

Design Accuracy

The gain stage output has an error contributed by mostly from:

- Offset voltage of U1 (OPA593): ±100 µV offset voltage of OPA593 has a small error contribution to the static device performance. The error contribution from offset voltage is calculated to be 0.00025 %FSR using the following equation, considering a 40-V span for the gain stage output.

$$\text{error (\%FSR)} = \frac{\text{offset voltage}}{\text{gain stage voltage span}} \times 100$$

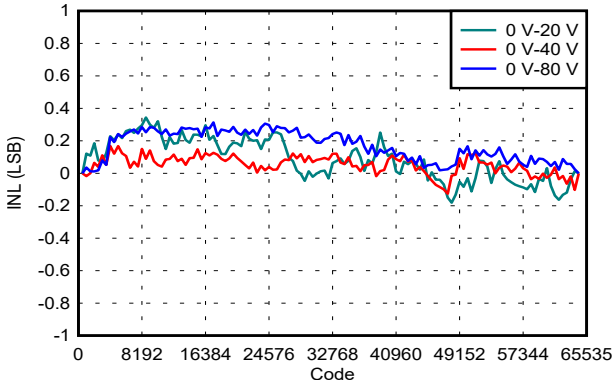
- Gain resistors R1 and R2 : Mismatch in ratio of R1 and R2 causes a gain error at the gain stage output. The error contribution due to mismatch in the ratio R1 and R2, is calculated to be 0.02 %FSR using the following equation.

$$\text{error (\%FSR)} = \left(1 - \frac{(1 \pm \Delta R2)}{(1 \pm \Delta R1)}\right) \times 100$$

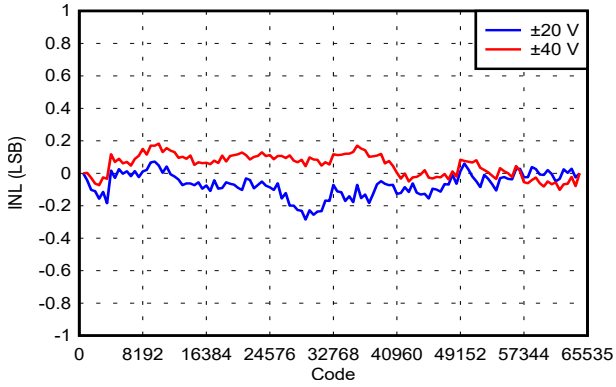
The calculated error contributions from U1, R1, and R3 show that the final gain stage output is just as accurate as the DAC81401.

Measurement Result

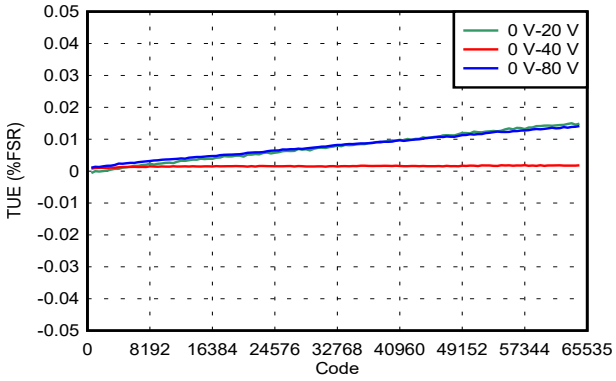
Integral nonlinearity (INL) and total unadjusted error (TUE) at the gain stage output were measured for different output voltage ranges. The INL and TUE plots from the next four images are measured for linear codes spans from code 512 to code 65024.



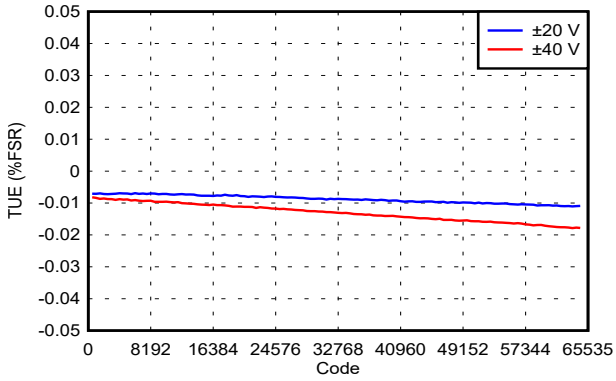
Integral Nonlinearity vs Digital Input Code – Unipolar Mode



Integral Nonlinearity vs Digital Input Code – Bipolar Mode



TUE vs Digital Input Code – Unipolar Mode



TUE vs Digital Input Code – Bipolar Mode

The DAC81401 voltage output range and corresponding gain stage voltage output range are listed in the following table.

DAC81401 VOUT Range	Gain Stage Voltage Range
0 V–5 V	0 V–20 V
0 V–10 V	0 V–40 V
0 V–20 V	0 V–80 V
±5 V	±20 V
±10 V	±40 V

Power Supply Requirement

An external high-voltage power supply is needed for the OPA593 in the gain stage (U1) and the attenuation stage (U2). The supplies also need to meet the headroom and footroom requirements as per the *OPA593 85-V, 250-mA Output Current, Precision, Power Op Amp* data sheet. These external power supplies need to be provided from a high-voltage supply source. Typical values used for HV+ and HV– are +41 V and −41 V or 81 V and 0 V, respectively.

$$\text{HV}- = \min\left(\text{VOUT}_{\text{HV}}\right) - \text{footroom}\left(\text{OPA593}\right)$$

$$\text{HV}+ = \max\left(\text{VOUT\_HV}\right) + \text{headroom}\left(\text{OPA593}\right)$$

Where VOUT_HV is output of the gain stage (U1) in the block diagram shown in *High-Voltage Gain Stage Circuit Block Diagram*.

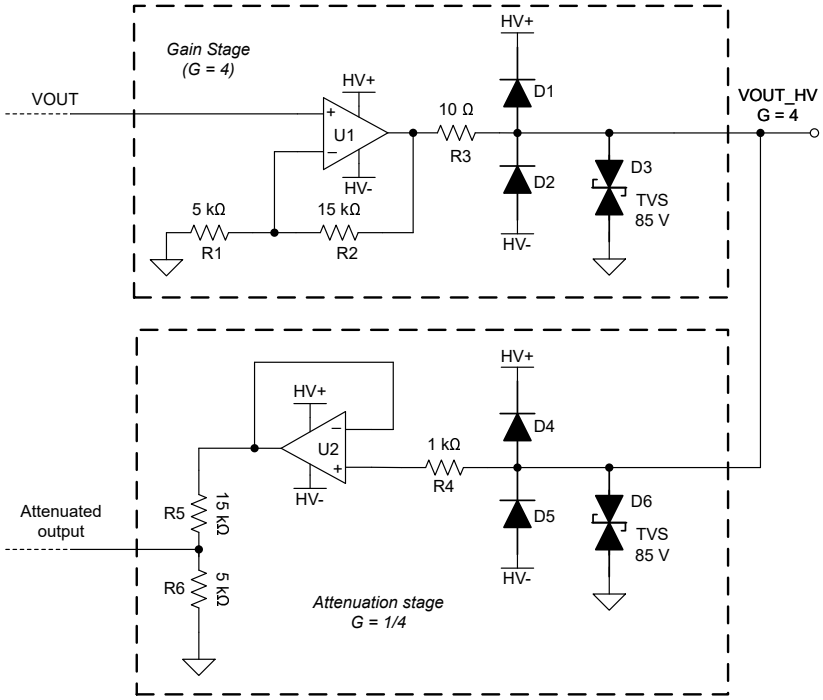
Set the DAC81401 power supply as recommended by the *DACx1401 Single-Channel, 16-Bit and 12-Bit, High-Voltage Output DACs With Precision Internal Reference* data sheet. AVDD and AVSS of the DAC81401 can be used for the V+ and V– power supply of the buffer stage operational amplifier (U3).

Overvoltage Stress (OVS) Protection Design

If the OPA593 (U1 and U2) output pins are exposed to industrial transient testing without external protection components, the internal diode structures of the DAC81401 becomes forward biased and conducts current. If the conducted current is large, as is common in high-voltage industrial transient tests, the structures can get permanently damaged and impact the device functionality.

The gain stage output and attenuation stage input includes an external electrical overstress protection circuit for short-circuit events. Protection is achieved by using the transient voltage suppressor (TVS) diodes D3 and D6 and clamp-to-rail diodes D1, D2, D4, and D5.

The combined protection from the TVS and clamp-to-rail diodes limits the current flowing into the device internal diode structures to prevent permanent damage. Considering R1 = 10 Ω and diode forward biased voltage is 0.7 V, the peak current entering to the device (U1 and U2) is 80 mA when the Schottky diode clamps VOUT to ±1.5 V from the rail. It is also important to connect the TVS diodes D3 and D6 to the gain stage output and attenuation stage input nodes to provide a discharge path for the energy sent to these nodes through diodes D3, D6, and the internal diode structures. R1 helps to limit the peak transient current or steady state current in case of incorrect bias voltage.



Protection Stage Block Diagram

Pseudocode Example

The following pseudocode sequence example:

- Powers up the DAC81401
- Enables the internal reference
- Enables the DAC channel
- Configures the voltage output range
- And sets the VOUT_HV output voltage

```
//Write these SPI commands after the device power supply is power configured

//Device power up
WRITE 0x0A04 to SPI_CONFIG register (0x03)
//Internal reference power up
WRITE 0x0000 to GEN_CONFIG register (0x04)
//DAC channel power up
WRITE 0xFFFE to DAC_PWDWN register (0x09)

//Configure the gain stage voltage output, default voltage range is 0 V to 20 V
//For 20 V span
WRITE 0x0000 to DACRANGE register (0x0A)
//For 5 V
WRITE 0x3FFF to DAC register (0x10)
//For 10 V
WRITE 0x7FFF to DAC register (0x10)
//For 15 V
WRITE 0xBFFF to DAC register (0x10)
//For 20 V
WRITE 0xFFFF to DAC register (0x10)
```

Design Featured Devices

Device	Key Features	Link
OPA593	85-V, Low offset, Low noise, 10 MHz, 250 mA output current precision operational Amplifier	OPA593
OPA189	36-V, Low offset, Low drift, Low noise, 14 MHz precision operational amplifier	OPA189

Design References

See the *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, DAC81401 Evaluation Module product page
- Texas Instruments, DAC81401 product page
- Texas Instruments, DAC81401 EVM User's Guide

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