Application Note

Analog Input Configurations, Mixing and Muxing of TAx5x1x Devices

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ABSTRACT

The TAx5x1x (TAC5212, TAC5211, TAC5112, TAC5111, TAA5212, TAC5242, TAA5242, TAC5142) family of devices have single or dual-channel analog-to-digital converters which supports highly configurable inputs for audio applications. This application note looks at the different input configurations such as input swing, common mode setting, AC/DC Coupling in normal and low power mode as well as the mixing and muxing option that are supported in this TAx5x1x device family. TAC5212, a stereo software control device is used in this application note as an example. For hardware pin control, the pin configurations for the input are provided in the respective data sheet. The audio input in this note is provided from LINE input. Microphone inputs or a mono version of this device can be configured in the similar manner.

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1 Introduction

TAC5212 is a CODEC with dual-channel analog-to-digital converters whose input pins (IN1P/M and IN2P/M) are configurable as differential inputs, single-ended inputs or single-ended mux inputs in AC or DC coupling. The type of input is configured through ADC_CH1_INSRC, the input impedance is configured through ADC_CH1_IMP and the coupling and common-mode tolerance is configured through ADC_CH1_CM_TOL.

Table 1-1. Input Configuration Selection

Input Configuration Setting	B0_P0_R80 (ADC_CH1_CFG0) [7:6]	Input Channel Configuration
0	ADC_CH1_INSRC=[00]	Analog differential input
1	ADC_CH1_INSRC=[01]	Analog single-ended input
2	ADC_CH1_INSRC=[10]	Analog single-ended mux INP1 input
3	ADC_CH1_INSRC=[11]	Analog single-ended mux INM1 input

Table 1-2. ADC Input Impedance Selection

Input Impedance Setting	B0_P0_R80 (ADC_CH1_CFG0) [5:4]	ADC Channel 1 Input Impedance
0	ADC_CH1_IMP=[00]	Typical 5-kΩ input impedance (For 4 Vrms case, is 10-kΩ)
1	ADC_CH1_IMP=[01]	Typical 10-kΩ input impedance
2	ADC_CH1_IMP=[10]	Typical 40-kΩ input impedance
3	ADC_CH1_IMP=[11]	Reserved

The common-mode tolerance is defined as the variation of the common mode signal of the differential amplifier, this is depicted in Figure 1-1.

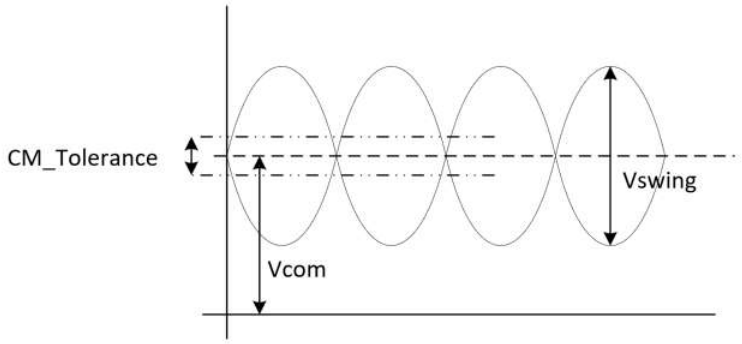


Figure 1-1. Common-Mode Tolerance

In AC-Coupling mode, this device family supports three common mode tolerances; differentially 100 mVpp, 1 Vpp and rail-to-rail (supply to ground) and in DC-Coupling mode, it supports differentially of 1 Vpp and rail-to-rail (supply to ground). This common mode tolerance needs to be selected based on the maximum expected common-mode variation. Since wider common-mode tolerance does degrade other performance parameters, the recommendation is to select the lowest tolerance mode possible.

Table 1-3. Common-Mode Tolerance Selection

Common-Mode Tolerance Setting	B0_P0_R80 (ADC_CH1_CFG0) [3:2]	Input Channel Common-Mode Tolerance
0	ADC_CH1_CM_TOL=[00]	AC-coupled input with common mode variance tolerance supported 50 mVpp for single ended and 100 mVpp for differential configuration
1	ADC_CH1_CM_TOL=[01]	AC-coupled / DC-coupled input with common mode variance tolerance supported 500 mVpp for single ended and 1 Vpp for differential configuration (Expected SNR degradation of 1-2 dB)
2	ADC_CH1_CM_TOL=[10]	AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) (Expected SNR degradation of approximately 35 dB, High CMRR supported only in this case)
3	ADC_CH1_CM_TOL=[11]	Reserved

Note that it is important to keep in mind the full-scale range (Vswing) of the device in all modes. This is especially important for large common-mode signals as they will limit the effective input range. In Mode 1 DC-Couple for example, a 500 mVp common voltage variant from the device internal common mode voltage of 1.375 V will limit the Vswing to 3.75 Vpp single-ended or 7.5 Vpp (2.65 Vrms) differential. In mode 2, it can support a common-mode range of 0V to Supply, but there would be no room left for a differential signal to be applied to the input pins at either of these extremes.

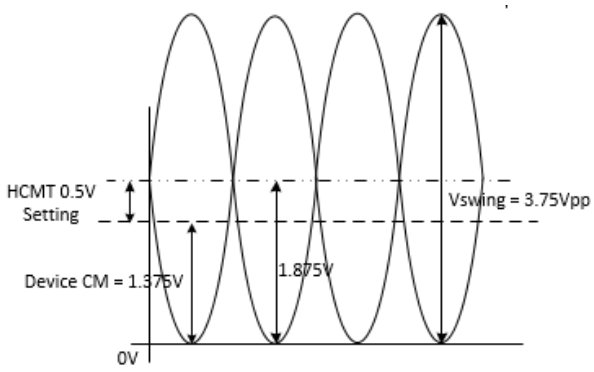


Figure 1-2. Mode 1 Common-Mode Example

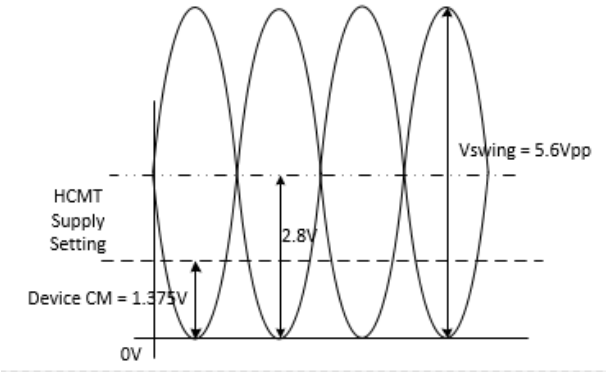
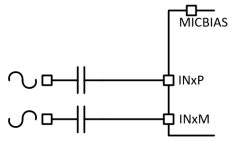
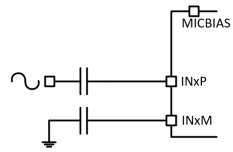
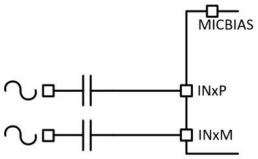
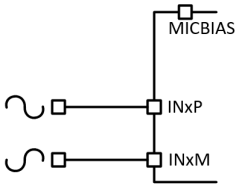
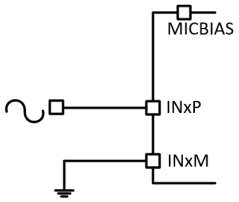
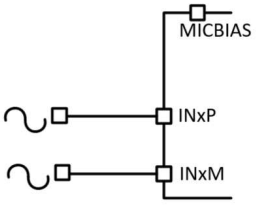


Figure 1-3. Mode 2 Common-Mode Example

2 Analog Input Configuration

Table 2-1 provides a summary of the different input configurations for IN1 in this application note, the same applies to IN2 input with the register channel change to 2.

Table 2-1. IN1 Input Configuration and Input Swing

Input Pin	Input Mode	Topology	Input Swing
IN1P-IN1M	LINE-IN Differential, AC-coupled		2 Vrms
IN1P	LINE-IN Single-Ended, AC-coupled		1 Vrms
IN1P	LINE-IN Single-Ended Mux IN1P, AC-coupled		1 Vrms
IN1M	LINE-IN Single-Ended Mux IN1M, AC-coupled		1 Vrms
IN1P-IN1M	LINE-IN Differential, DC-coupled		4 Vrms
IN1P	LINE-IN Single-ended, DC-coupled		2 Vrms
IN1P	LINE-IN Single-ended Mux IN1P, DC-coupled		2 Vrms
IN1M	LINE-IN Single-ended Mux IN1M, DC-coupled		2 Vrms

For each of the test, audio signal is provided from APx500 analog balance or unbalanced output with input level referenced to the full-scale swing of the device configuration for example 0 dBrG is referenced to 2 Vrms single ended swing or 4 Vrms differential input swing in DC-Coupled configuration.

2.1 Differential AC Coupled Configuration

In the AC-Coupled differential input configuration, the following device register setting is used and the respective input waveform provided to IN1P/M for the full-scale swing. Change the register setting in line 13 and 14 for the different input impedance and common-mode tolerance setting B0_P0_R80 (0x50) and B0_P0_R85 (0x55). The following plots are based on Mode 0 with 5KΩ input impedance.

```
1  ##### Record AC-Couple Differential IN1-IN2 path ######
2  # Target Mode, TDM, 32-bit
3  # Primary ASI only, multiple of 48KHz Sampling
4  #
5  w a0 00 00  # Set page 0
6  w a0 01 01  # Software Reset
7  w a0 02 09  # Wake up with AVDD > 2v and all VDDIO level
8  w a0 10 50  # Configure DOUT as Primary ASI (PASI) DOUT
9  w a0 19 00  # 1 data input and 1 data output for PASI
10 w a0 1a 30  # PASI TDM, 32 bit format
11 w a0 1e 20  # PASI Ch1 on slot 0
12 w a0 1f 21  # PASI Ch2 on slot 1
13 w a0 50 00  # ADC Ch1 diff input, 5KOhm, 2Vrms ac-coupled, audio band
14 w a0 55 00  # ADC Ch2 diff input, 5KOhm, 2Vrms ac-coupled, audio band
15 w a0 76 c0  # Enable Input Ch1 and Ch2, disable output channels
16 w a0 78 a0  # Power up ADC and MICBIAS
```

Figure 2-1. Differential AC-Coupled Register Setting

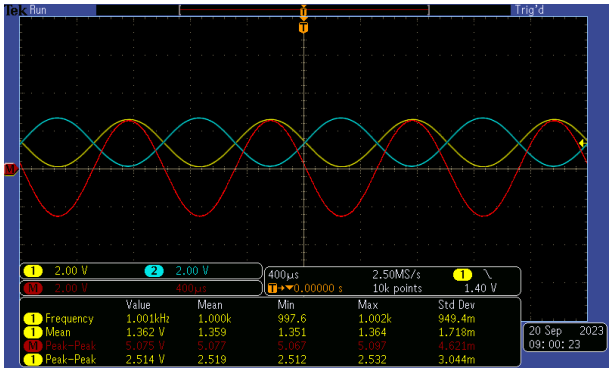


Figure 2-2. Differential AC-Coupled Input Swing at -1dBrG (0dBrG = 2Vrms)

A frequency plot of the Dynamic Range with -60dBrG input and SNR with input AC signal shorted to ground are provided here of the 100mVpp common-mode setting. A similar plot can be obtained for the 2 different common-mode tolerances.

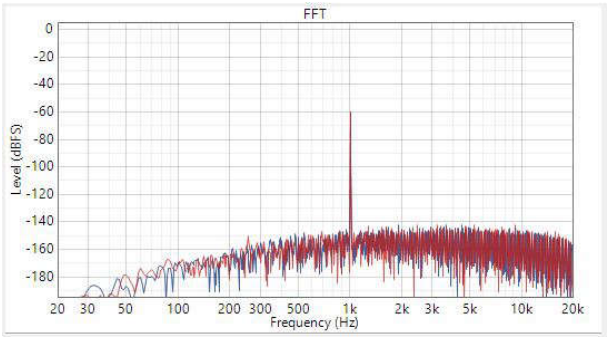


Figure 2-3. Differential AC-Coupled Dynamic Range at -60dBrG Input

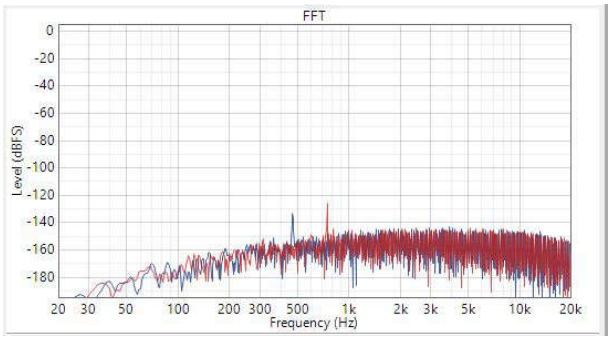


Figure 2-4. SNR with Input AC Signal shorted to GND

Table 2-2 summarizes the performances for the three different common tolerances across the input impedance for the different software control device variants. Table 2-3 summarizes the performances for hardware pin control devices which supports 5KOhm input impedance only in differential AC-Coupled.

Table 2-2. AC-Coupled Performance Summary - Software Control Device

		DR (dB)			SNR (dB)			THDN (at-1dBrG)		
HCMT Mode	Zin	TAC521x	TAC511x	TAA521x	TAC521x	TAC511x	TAA521x	TAC521x	TAC511x	TAA521x
0	5K	118	103	118	118	103	118	-95	-91	-95
	10K	113	103	113	113	103	113	-102	-91	-102
	40K	101	103	102	102	103	102	-97	-91	-97
1	5K	116	102	116	116	102	116	-95	-91	-95
	10K	112	102	112	112	102	112	-102	-91	-102
	40K	100	102	101	101	102	101	-96	-91	-97
2	5K	113	101	113	113	101	113	-95	-91	-95
	10K	109	101	109	109	101	109	-101	91	-101
	40K	99	101	100	100	101	100	-96	-91	-96

Table 2-3. AC-Coupled Performance Summary - Hardware Control Device

		DR (dB)			SNR (dB)			THDN (at-1dBrG)		
MD5-MD4	Zin	TAC5242	TAC5142	TAA5242	TAC5242	TAC5142	TAA5242	TAC5242	TAC5142	TAA5242
00	5K	117	101	117	117	101	117	-95	-91	-95

2.2 Single Ended AC Coupled Configuration

In the AC-Coupled single-ended input configuration, the following device register setting is used and the respective input waveform provided to IN1P for the full-scale swing.

```
##### Record AC-Couple Single-Ended IN1-IN2 path ######
# Target Mode, TDM, 32-bit
# Primary ASI only, multiple of 48KHz Sampling
#
w a0 00 00  # Set page 0
w a0 01 01  # Software Reset
w a0 02 09  # Wake up with AVDD > 2v and all VDDIO level
w a0 10 50  # Configure DOUT as Primary ASI (PASI) DOUT
w a0 19 00  # 1 data input and 1 data output for PASI
w a0 1a 30  # PASI TDM, 32 bit format
w a0 1e 20  # PASI Ch1 on slot 0
w a0 1f 21  # PASI Ch2 on slot 1
w a0 50 40  # ADC Ch1 SE input, 5KOhm, 1Vrms ac-coupled, audio band
w a0 55 40  # ADC Ch2 SE input, 5KOhm, 1Vrms ac-coupled, audio band
w a0 76 c0  # Enable Input Ch1 and Ch2, disable output channels
w a0 78 a0  # Power up ADC and MICBIAS
```

Figure 2-5. Single Ended AC-Coupled Register Setting

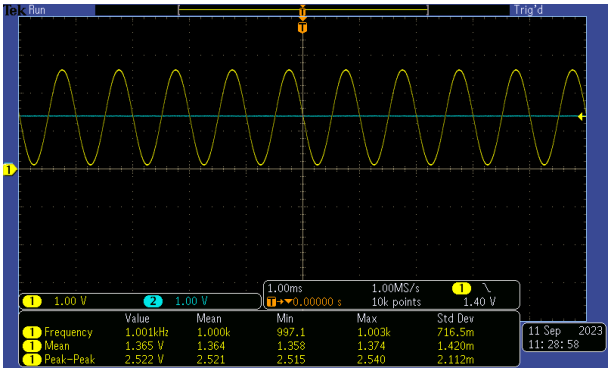


Figure 2-6. Single Ended AC-Coupled Input Swing at -1dBrG (0dBrG = 1Vrms)

A frequency plot of the Dynamic Range with -60dBrG input and SNR with input AC signal shorted to ground are provided here.

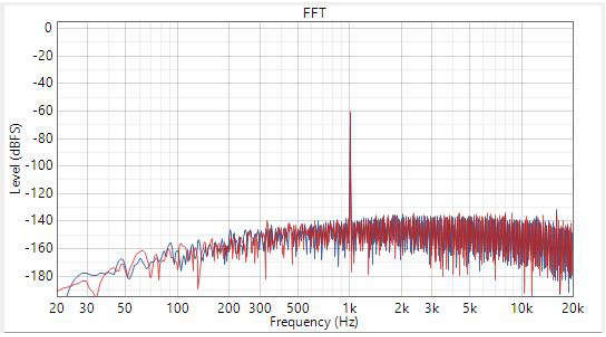


Figure 2-7. Single Ended AC-Coupled Dynamic Range at -60dBrG Input

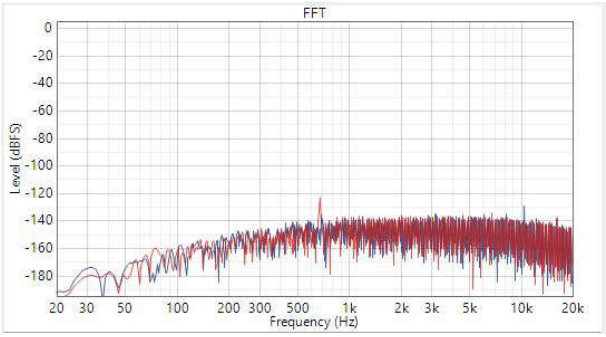


Figure 2-8. SNR With Input AC Signal Shorted to GND

2.3 Differential DC Coupled Configuration

In the DC-Coupled differential input configuration, the following device register setting is used and the respective input waveform provided to IN1P/M for the full-scale swing. Change the register setting in line 13 and 14 for the different input impedance and common-mode tolerance setting B0_P0_R80 (0x50) and B0_P0_R85 (0x55). The setting and plots below are based on Mode 2 with 10K Ohm input impedance. The external common-mode voltage is set at 2.8V.

```
1  ##### Record DC-Couple Differential IN1-IN2 path ######
2  # Target Mode, TDM, 32-bit
3  # Primary ASI only, multiple of 48KHz Sampling
4  #
5  w a0 00 00  # Set page 0
6  w a0 01 01  # Software Reset
7  w a0 02 09  # Wake up with AVDD > 2v and all VDDIO level
8  w a0 10 50  # Configure DOUT as Primary ASI (PASI) DOUT
9  w a0 19 00  # 1 data input and 1 data output for PASI
10 w a0 1a 30  # PASI TDM, 32 bit format
11 w a0 1e 20  # PASI Ch1 on slot 0
12 w a0 1f 21  # PASI Ch2 on slot 1
13 w a0 50 1a  # ADC Ch1 diff input, 10KOhm, Mode 2, 4Vrms dc-coupled, audio band
14 w a0 55 1a  # ADC Ch2 diff input, 10KOhm, Mode 2, 4Vrms dc-coupled, audio band
15 w a0 76 c0  # Enable Input Ch1 and Ch2, disable output channels
16 w a0 78 a0  # Power up ADC and MICBIAS
```

Figure 2-9. Differential DC-Coupled Register Setting

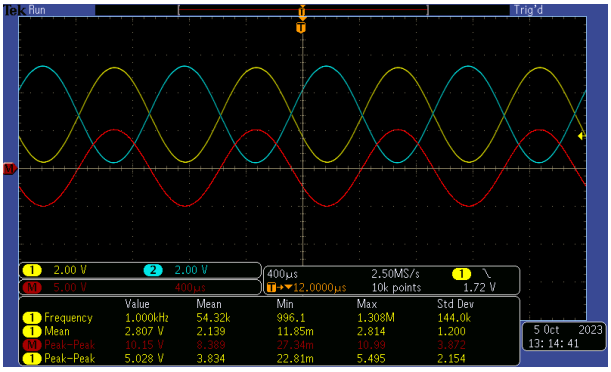


Figure 2-10. Differential DC-Coupled Input Swing at -1dBrG (0dBrG = 4Vrms)

A frequency plot of the Dynamic Range with -60dBrG input and SNR with input AC signal shorted to ground are provided here for the supply common-mode setting. A similar plot can be obtained for the other common-mode tolerance.

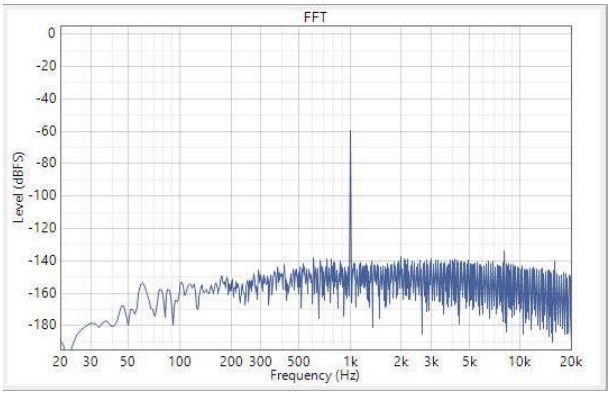


Figure 2-11. Differential DC-Coupled Dynamic Range at -60dBrG Input

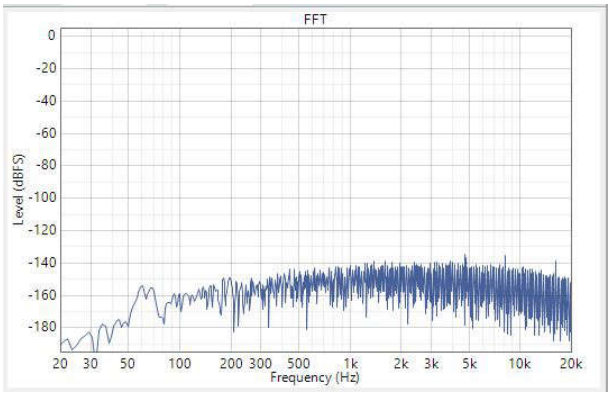


Figure 2-12. SNR with Input AC Signal shorted to GND

Table 2-4 summarizes the performances for the two different common tolerances for differential DC-Coupled mode across input impedance and device variants. Table 2-5 summarizes the performances for hardware pin control devices which supports 5KOhm input impedance only in differential DC-Coupled.

Table 2-4. DC-Coupled Performance Summary- Software Control Device

				THDN (at-1dBrG)			DR (dB)			SNR (dB)		
HCMT Mode	Zin	External Vcm (V)	0 dBrG (Vrms)	TAC521x	TAA521x	TAC511x	TAC521x	TAA521x	TAC511x	TAC521x	TAA521x	TAC511x
1	5K	1.875	2.62	-101	-102		117	117		117	117	
	10K	1.875	2.62	-101	-102		117	117		117	117	
	40K	1.875	2.62	-98	-99		107	106		106	106	
2	5K	2.8	4	-81	-80		113	113		114	114	
	10K	2.8	4	-81	-80		113	113		114	114	
	40K	2.8	4	-82	-81		105	105		105	105	
1	5K	1.875	2			-90			102			102
	10K	1.875	2			-90			102			102
	40K	1.875	2			-90			102			102
2	5K	2.8	2			-86			101			101
	10K	2.8	2			-86			101			101
	40K	2.8	2			-86			101			101

Table 2-5. DC-Coupled Performance Summary- Hardware Control Device

				THDN (at-1dBrG)			DR (dB)			SNR (dB)		
MD5 -MD4	Zin	External Vcm (V)	0 dBrG (Vrms)	TAC5242	TAC5142	TAA5242	TAC5242	TAC5142	TAA5242	TAC5242	TAC5142	TAA5242
01	5K	1.875	2.62	-95	-91	-96	111	99	111	111	99	111

2.4 Single Ended DC Coupled Configuration

In the DC-Coupled single-ended input configuration, the following device register setting is used and the respective input waveform provided to IN1P for the full-scale swing.

```
##### Record DC-Couple Single-Ended IN1-IN2 path ######
# Target Mode, TDM, 32-bit
# Primary ASI only, multiple of 48KHz Sampling
#
w a0 00 00  # Set page 0
w a0 01 01  # Software Reset
w a0 02 09  # Wake up with AVDD > 2v and all VDDIO level
w a0 10 50  # Configure DOUT as Primary ASI (PASI) DOUT
w a0 19 00  # 1 data input and 1 data output for PASI
w a0 1a 30  # PASI TDM, 32 bit format
w a0 1e 20  # PASI Ch1 on slot 0
w a0 1f 21  # PASI Ch2 on slot 1
w a0 50 46  # ADC Ch1 SE input, 5KOhm, 2Vrms dc-coupled, audio band
w a0 55 46  # ADC Ch2 SE input, 5KOhm, 2Vrms dc-coupled, audio band
w a0 76 c0  # Enable Input Ch1 and Ch2, disable output channels
w a0 78 a0  # Power up ADC and MICBIAS
```

Figure 2-13. Single Ended DC-Coupled Register Setting

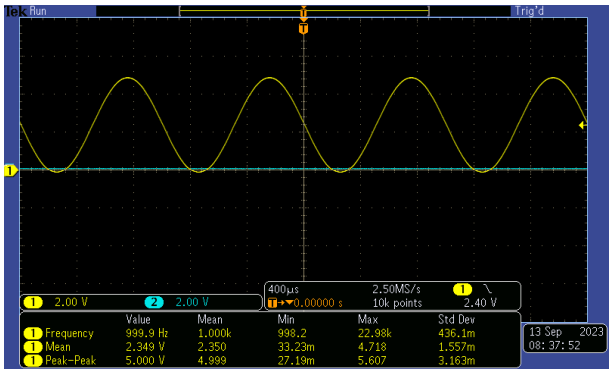


Figure 2-14. Single Ended DC-Coupled Input Swing at -1dBrG (0dBrG = 2Vrms)

A frequency plot of the Dynamic Range with -60dBrG input and SNR with input AC signal shorted to ground are provided here.

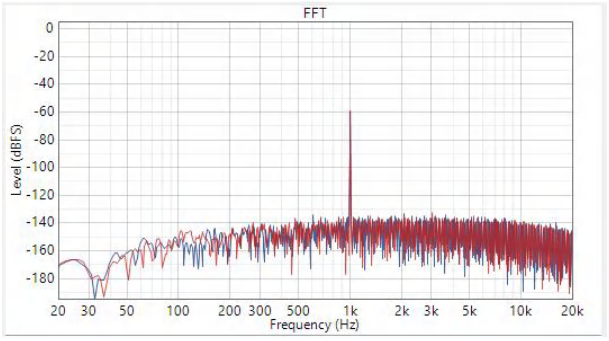


Figure 2-15. Single Ended DC Coupling Dynamic Range with -60dBrG Input

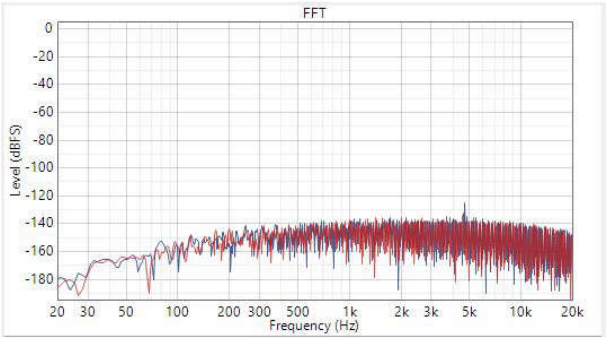


Figure 2-16. Single Ended DC Coupling SNR

2.5 Analog Input Mux Configuration

Analog mux input allows input selection either from IN1P or IN1M into the ADC path. The device needs to be configured in its respective mux setting in register B0_P0_R80 (0x50) ADC_CH1_INSRC. In this configuration, either IN1P or IN1M be the input to the ADC signal chain, they are independent source. In this example, IN1P is a 1KHz tone at -1dBrG and IN1M is a 1250Hz tone at -1dBrG; 0dBrG = 1Vrms Single-Ended Fullscale.

```
##### Record AC-Couple SE Mux IN1P path ######
# Target Mode, TDM, 32-bit
# Primary ASI only, multiple of 48KHz Sampling
#
w a0 00 00  # Set page 0
w a0 01 01  # Software Reset
w a0 02 09  # Wake up with AVDD > 2v and all VDDIO level
w a0 10 50  # Configure DOUT as Primary ASI (PASI) DOUT
w a0 19 00  # 1 data input and 1 data output for PASI
w a0 1a 30  # PASI TDM, 32 bit format
w a0 1e 20  # PASI Ch1 on slot 0
w a0 1f 21  # PASI Ch2 on slot 1
w a0 50 80  # ADC Ch1 SE MUX IN1P input, 5KOhm, 1Vrms ac-coupled, audio band
w a0 55 00  # ADC Ch2 default Diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 76 c0  # Enable Input Ch1 and Ch2, disable output channels
w a0 78 a0  # Power up ADC and MICBIAS
```

Figure 2-17. IN1P Mux Input Register Setting

```
##### Record AC-Couple SE Mux IN1M path ######
# Target Mode, TDM, 32-bit
# Primary ASI only, multiple of 48KHz Sampling
#
w a0 00 00  # Set page 0
w a0 01 01  # Software Reset
w a0 02 09  # Wake up with AVDD > 2v and all VDDIO level
w a0 10 50  # Configure DOUT as Primary ASI (PASI) DOUT
w a0 19 00  # 1 data input and 1 data output for PASI
w a0 1a 30  # PASI TDM, 32 bit format
w a0 1e 20  # PASI Ch1 on slot 0
w a0 1f 21  # PASI Ch2 on slot 1
w a0 50 c0  # ADC Ch1 SE MUX IN1M input, 5KOhm, 1Vrms ac-coupled, audio band
w a0 55 00  # ADC Ch2 default Diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 76 c0  # Enable Input Ch1 and Ch2, disable output channels
w a0 78 a0  # Power up ADC and MICBIAS
```

Figure 2-18. IN1M Mux Input Register Setting

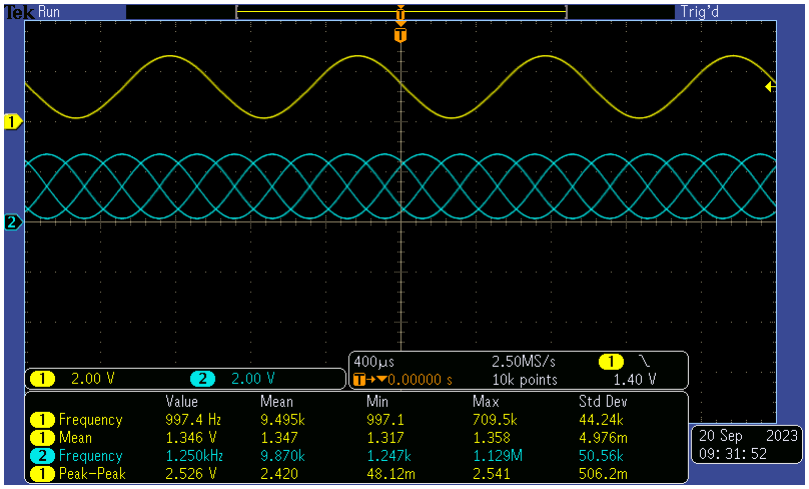


Figure 2-19. IN1P and IN1M Mux Input at -1dBrG (0 dBrG = 1Vrms)

The output of the respective setting shows the desired signal and the suppression of the other input signal.

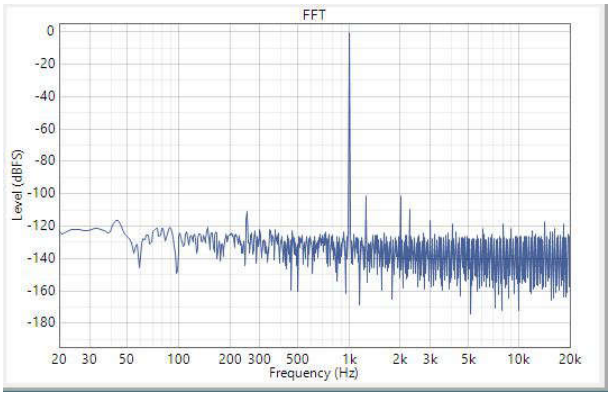


Figure 2-20. Output with IN1P Mux Input Configured

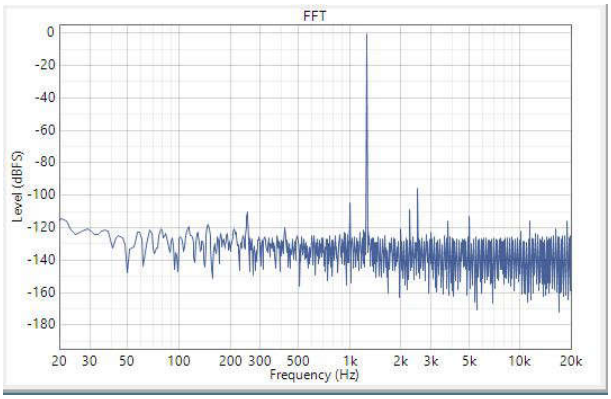


Figure 2-21. Output with IN1M Mux Input Configured

3 Power Tune Mode and Analog Mixing Feature

Following are features that are available in this device for power saving, as well as, analog mixing capability.

3.1 Differential AC Coupled Power Tune Mode

When balancing power and performance are needed, the following example provides the register setting for a differential AC-Coupled input with 1.8 V AVDD in power tune mode. Register PWR_TUNE_CFG0 in B0_P0_R78 (0x4E) provides the configuration to place the device into power compensation mode.

```
##### Record AC-Couple Differential IN1-IN2 path ######
# Target Mode, TDM, 32-bit
# Primary ASI only, multiple of 48KHz Sampling
# AVDD = 1.8V, Differential 1Vrms Input
#
w a0 00 00  # Set page 0
w a0 01 01  # Software Reset
w a0 02 0D  # Wake up with AVDD = 1.8v and all VDDIO level
w a0 10 50  # Configure DOUT as Primary ASI (PASI) DOUT
w a0 19 00  # 1 data input and 1 data output for PASI
w a0 1a 30  # PASI TDM, 32 bit format
w a0 1e 20  # PASI Ch1 on slot 0
w a0 1f 21  # PASI Ch2 on slot 1
w a0 34 c0  # PLL is disabled
w a0 4d 02  # MICBIAS = VREF, VREF = 1.375V for 1 Vrms differential
w a0 4e 04  # Enable Low Power Filter
w a0 50 00  # ADC Ch1 diff input, 5KOhm, ac-coupled, audio band
w a0 55 00  # ADC Ch2 diff input, 5KOhm, ac-coupled, audio band
w a0 76 c0  # Enable Input Ch1 and Ch2, disable output channels
w a0 78 80  # Power up ADC
```

Figure 3-1. Power Tune Mode Differential AC-Coupled Register Setting

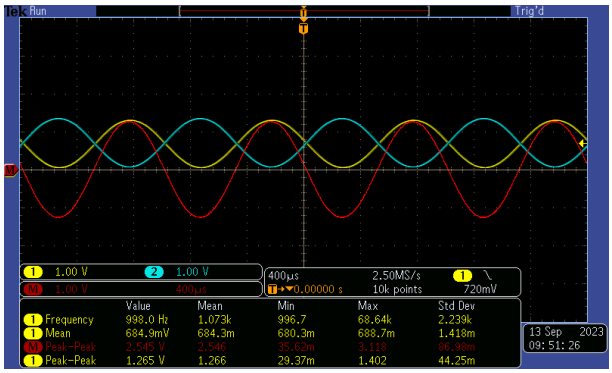


Figure 3-2. Power Tune Differential AC-Coupled Input at -1dBrG (0dBrG = 1Vrms)

A frequency plot of the Dynamic Range with -60dBrG input and SNR with input AC signal shorted to ground are provided here.

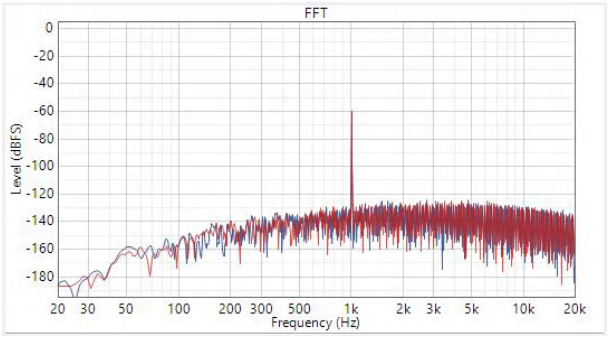


Figure 3-3. Power Tune Mode Differential AC-Coupled Dynamic Range at -60dBrG

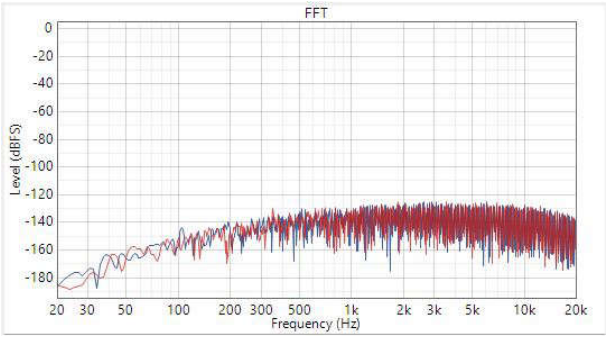


Figure 3-4. Power Tune Mode Differential AC-Coupled SNR

3.2 Analog Mixing

When mixing of analog is desired, this device provides capability of mixing from various input channels with programmable mixer feature and scale factor to generate the final output channels. In this example an input from single ended IN1P and IN1M with different tone and input swing are mixed as shown in the register setting and the input waveforms. IN1P is a 1 KHz tone at -10 dBrG and IN1M is a 750 Hz tone at -20 dBrG; 0 dBrG = 1 Vrms Fullscale.

```
##### Record Mix AC-Couple SE IN1P and IN1M Input path ######
# Target Mode, TDM, 32-bit
# Primary ASI only, multiple of 48KHz Sampling
#
w a0 00 00  # Set page 0
w a0 01 01  # Software Reset
w a0 02 09  # Wake up with AVDD > 2v and all VDDIO level
w a0 10 50  # Configure DOUT as Primary ASI (PASI) DOUT
w a0 19 00  # 1 data input and 1 data output for PASI
w a0 1a 30  # PASI TDM, 32 bit format
w a0 1e 20  # PASI Ch1 on slot 0
w a0 1f 21  # PASI Ch2 on slot 1
w a0 50 40  # ADC Ch1 SE input, 5KOhm, 1Vrms ac-coupled, audio band
w a0 55 00  # ADC Ch2 default Diff input, 5KOhm, 2Vrms ac-coupled, audio band
w a0 00 01  # Set page 1
w a0 2c 20  # Enable ADC Mixer
w a0 00 00  # Set page 0
w a0 76 c0  # Enable Input Ch1 and Ch2, disable output channels
w a0 78 a0  # Power up ADC and MICBIAS
```

Figure 3-5. Analog Single Ended Mix Register Setting

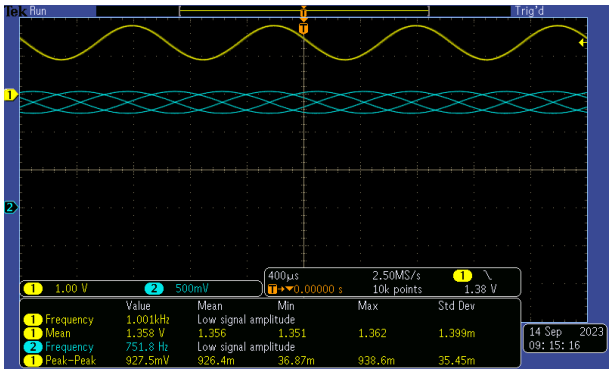


Figure 3-6. IN1P and IN1M Input Signal

The corresponding mixed output frequency respond is shown in Figure 3-7.

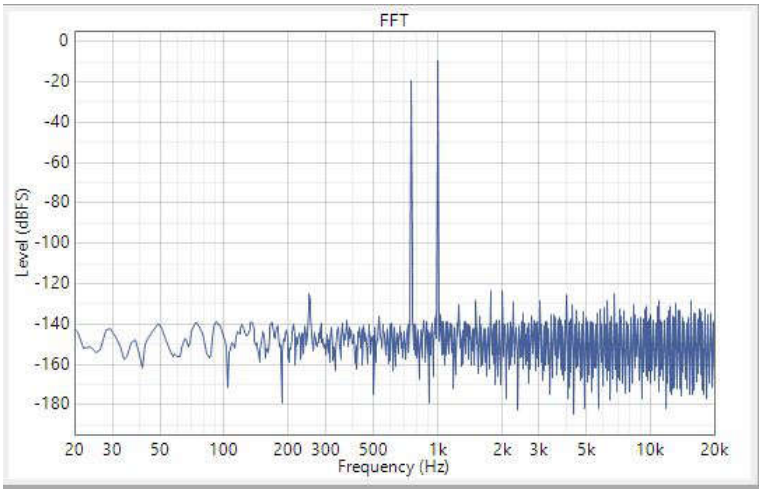


Figure 3-7. Mixed Analog Input of IN1P and IN1M

4 Summary

The TAx5x1x family of devices offers very flexible input configuration with its muxing and mixing capability making it suitable for a wide range of applications. Multiple common-mode tolerance modes are provided to allow the system to perform well even in the presence of large amounts of common-mode noise. Since the performance of the devices does change with the input configuration, it is recommended to use the lowest common-mode setting possible that still satisfies the tolerance required by the system. For best performance, AC coupling is recommended.

5 References

- Texas Instruments, *TAC5212 High-Performance Stereo Audio Codec With 115dB Dynamic Range ADC and 120dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAC5211 High-Performance Mono Audio Codec With 115dB Dynamic Range ADC and 115dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAC5112 Low-Power Stereo Audio Codec With 102dB Dynamic Range ADC and 106dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAC5111 Low-Power Mono Audio Codec With 108dB Dynamic Range ADC and 108dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAA5212 Low-Power High-Performance Stereo Audio ADC With 115dB Dynamic Range*, data sheet.
- Texas Instruments, *TAC5242 High-Performance Pin Controlled Stereo Audio Codec With 118dB Dynamic Range ADC and 120dB Dynamic Range DAC*, data sheet.
- Texas Instruments, *TAA5242 Low-power High-Performance Stereo Audio ADC With 118dB Dynamic Range*, data sheet.
- Texas Instruments, *TAC5142 Low-Power Pin Controlled Stereo Audio Codec With 100dB Dynamic Range ADC and 106dB Dynamic Range DAC*, data sheet.

6 Revision History

Changes from Revision * (October 2023) to Revision A (May 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *TAC5242, TAA5242, and TAC5142*	1
• Added *AC-Coupled Performance Summary - Hardware Control Device* table	5
• Added *DC-Coupled Performance Summary- Hardware Control Device* table	7

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