Analog Engineer's Circuit

Programmable comparator circuit with hysteresis or latching output

Smart DAC

Katlynne Jones

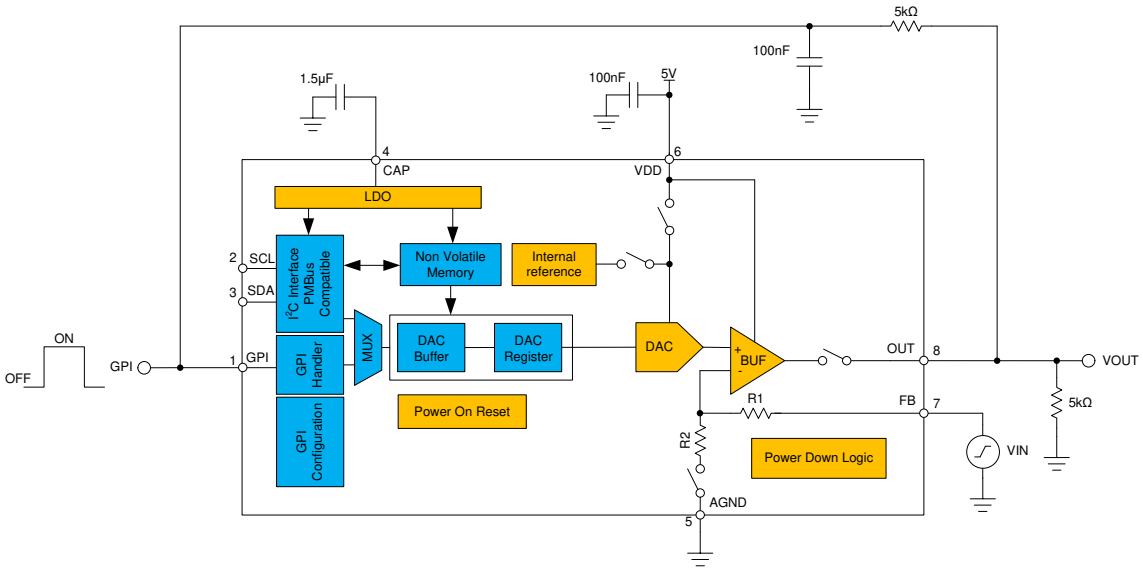
Design Objective

Key Input Parameter	Key Output Signal	Recommended Device
0-V to 5.5-V analog input, programmable threshold voltages, GPI feedback	Digital output of a comparator, GPI feedback	DAC53701, DAC43701, DAC53701-Q1, DAC43701-Q1

Objective: *Create a comparator with adjustable hysteresis thresholds or a latching output.*

Design Description

This design uses a buffered voltage output DAC to create a comparator with a programmable threshold value. Additional features such as hysteresis or a latching output can be configured as well. In this design, the integrated buffer will act as a comparator and the output of the DAC will act as the threshold for the comparator. The 8-bit DAC43701, and 10-bit DAC53701 have a general-purpose input pin, GPI, that can be used to trigger a function generator, switch between a high and low DAC value, or power down the DAC. The DAC43701 and DAC53701 integrated buffer has an exposed feedback path via the feedback pin (FB) which will act as the voltage input to the comparator. All register settings can be saved using the non-volatile memory (NVM) on the DAC43701 and DAC53701 meaning that the devices can be used without a processor, even after a power cycle. This circuit can be used in applications such as laser distance measurement, cordless vacuum cleaner, medical accessories, retail automation, or grid infrastructure.



Design Notes

1. The *DACx3701 10-Bit and 8-Bit, Voltage-Output Smart DACs With Nonvolatile Memory and PMBus™ Compatible I2C Interface With GPI Control Data Sheet* recommends using a 100-nF decoupling capacitor for the VDD pin and a 1.5µF or greater bypass capacitor for the CAP pin. The CAP pin is connected to the internal LDO. Place these capacitors close to the device pins.
2. An external reference of 1.8V to 5.5V can be applied to the VDD pin of the device. In addition, there is an internal precision 1.21-V reference with ×1.5, ×2, ×3, and ×4 gain options. If using a noisy supply, it is best to use the internal reference instead of VDD as the reference because noise on the reference translates directly to noise on the output of the DAC53701.
3. The input signal should not exceed VDD. Also, the maximum threshold voltage is limited by the reference voltage used. If necessary, larger input voltages can be scaled using a voltage divider and the threshold voltage can be adjusted accordingly.
4. The GPI_CONFIG field in the CONFIG2 register maps the GPI pin to the various functions.
   a. To configure a programmable comparator with hysteresis, the GPI will be set to Margin-High, Low function. Set the high threshold in the DAC_MARGIN_HIGH register, and the low threshold in the DAC_MARGIN_LOW register.
   b. To configure a latching comparator, the GPI pin will be set to Power-Up, Down (10kΩ) function. Set the threshold in the DAC_DATA register.
5. Comparator with Hysteresis: In this design, the 5-V VDD supply input is used as the reference. The high threshold value for the comparator is set to is set to 3V using the DAC_MARGIN_HIGH register, and the low threshold is set to 1V using the DAC_MARGIN_LOW register. The codes programmed to these registers, in decimal, is calculated using:

$$DAC\_MARGIN\_HIGH = \frac{V_{THRESH\_HIGH}}{V_{REF} \times GAIN} \times 1024$$

$$DAC\_MARGIN\_LOW = \frac{V_{THRESH\_LOW}}{V_{REF} \times GAIN} \times 1024$$

   With a 5-V reference, unity gain, and threshold values of 3V and 1V, the equation becomes:

$$DAC\_MARGIN\_HIGH = \frac{3V}{5V} \times 1024 = 614.4d$$

$$DAC\_MARGIN\_LOW = \frac{1V}{5V} \times 1024 = 204.8d$$

   This is rounded to 614d and 205d to give a high threshold of 2.998V and low threshold of 1V.
6. Latching Comparator: In this design, the 5-V VDD supply input is used as the reference. The threshold value for the comparator is set to is set to 3V using the DAC_DATA register. The code programmed to this register, in decimal, is calculated using:

$$DAC\_DATA = \frac{V_{THRESH}}{V_{REF} \times GAIN} \times 1024$$

   With a 5-V reference, unity gain, and a threshold value of 3V, the equation becomes:

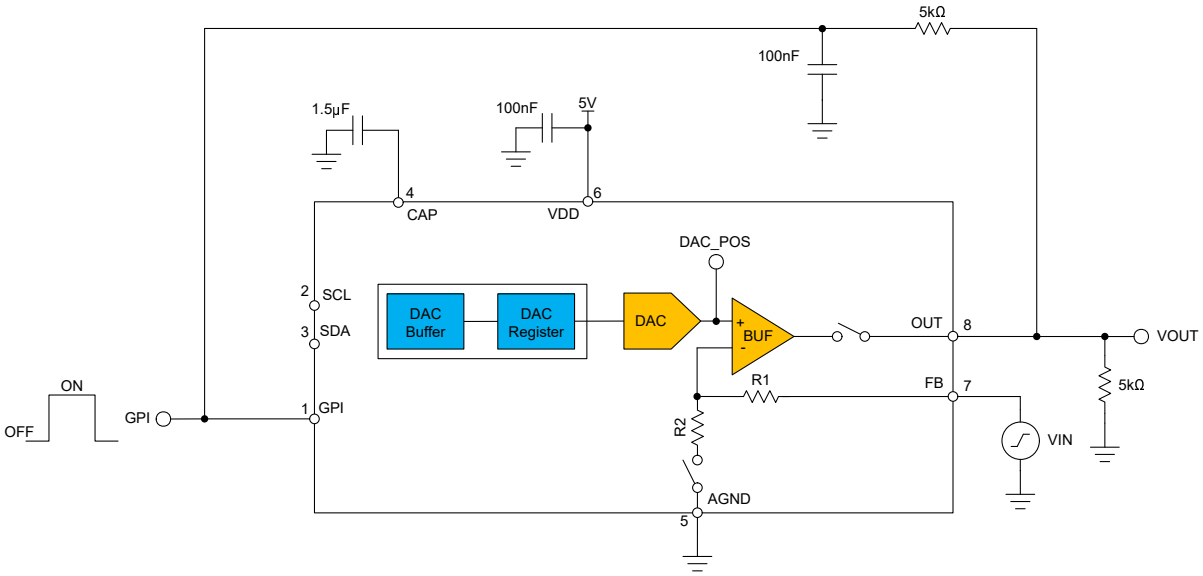
$$DAC\_DATA = \frac{3V}{5V} \times 1024 = 614.4d$$

   This is rounded down to 614d to give a threshold of 2.998V.

7. Using a 5-V reference and the 10-bit DAC53701, the LSB size, or step size between each code, is about 4.88mV. Using lower reference voltages decreases the LSB size and increases the resolution of the threshold value. Using a smaller reference limits the upper limit of the threshold value, but as previously discussed, input voltages can be scaled down if necessary.
8. The DAC53701 can be programmed with the initial register settings described in the Register Settings section using I2C. The initial register settings can be saved in the NVM by writing a 1 to the NVM_PROG field of the TRIGGER register. After programming the NVM, the device loads all applicable registers with the values stored in the NVM after a reset or a power cycle.
9. The GPI pin starts with a low voltage at start-up due to the pulldown resistor on the output. A high start pulse must be applied to the GPI pin of the latching comparator to power-on the DAC53701. The comparator with hysteresis starts at the low threshold value at start-up.

Design Simulations

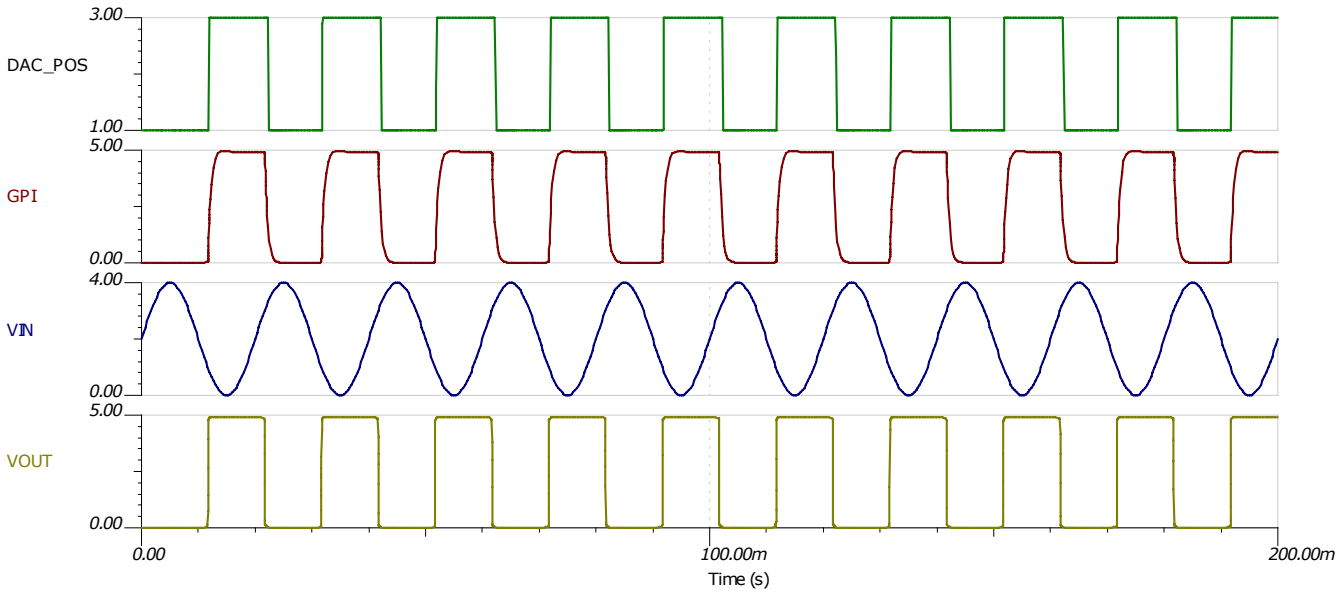
This schematic is used for the following simulations of the DAC53701 programmable comparator with hysteresis and latching comparator.



Transient Simulation Results

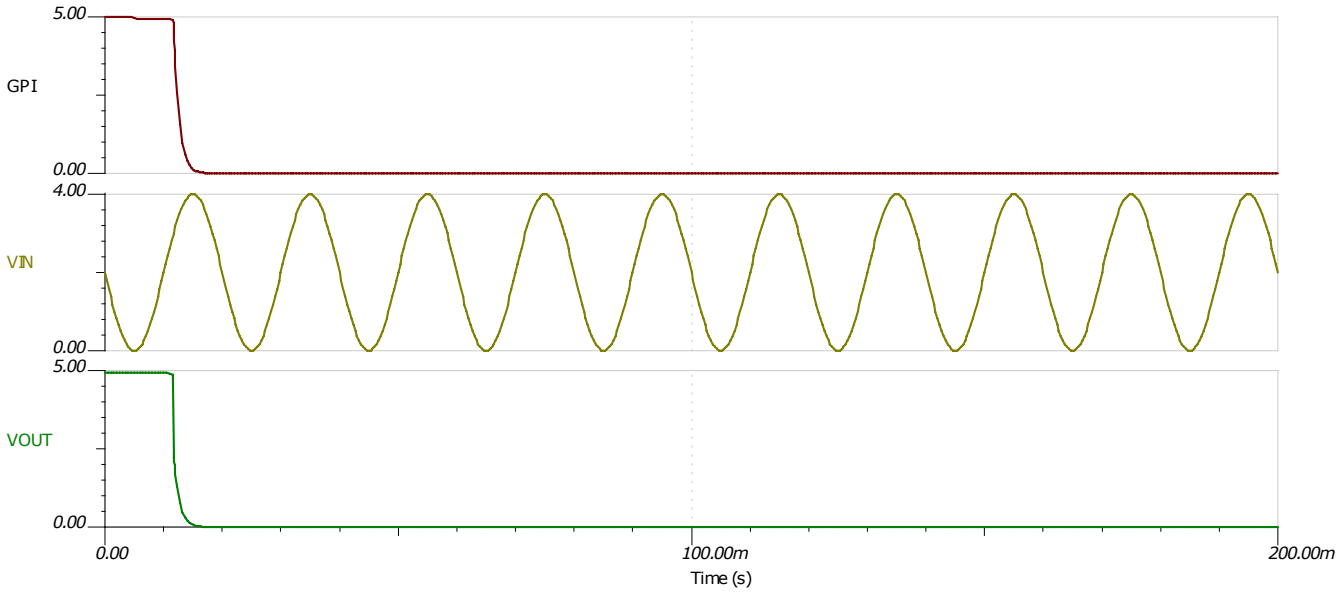
Programmable Hysteresis

This simulation shows the DAC53701 output responding to a 4-Vpp input sine wave biased around 2V. The DAC_POS value changes with the MARGIN_HIGH and MARGIN_LOW values triggered by the GPI.



Latching Comparator

This simulation shows the DAC53701 output responding to a 4-Vpp input sine wave biased around 2V. A high pulse is applied to the GPI pin for 5ms to turn on the DAC and start the comparator. When the V_{IN} rises to 3V, the comparator output goes low and triggers the GPI to put the DAC in power-down mode.



Register Settings

Register Settings for the DAC53701 Programmable Comparator With Hysteresis

Register Address	Register Name	Setting	Description
0xD1	GENERAL_CONFIG	0x0000	[15:14] 0b00: Selects the type of waveform to be generated by the continuous waveform generator (CWG)
			[13] 0b0: Write 0b1 to lock device. Unlock by writing 0b0101 to DEVICE_UNLOCK_CODE field in the PROTECT register
			[12] 0b0: Write 0b1 to enable PMBus mode
			[11:9] 0b000: Selects the code step used for programmable slew rate control
			[8:5] 0b1111: Selects the code step used for programmable slew rate control
			[4:3] 0b00: Powers up the device output
			[2] 0b0: Disables the internal reference
			[1:0] 0b00: Selects the gain to be applied to the internal reference
0xD2	CONFIG2	0x1000	[15:14] 0b00: Configures the device I2C address
			[13:11] 0b010: Configures the GPI pin as Margin-High, Low trigger
			[10] 0b0: Write 0b1 to generate a high priority medical alarm
			[9] 0b0: Write 0b1 to generate a medium priority medical alarm
			[8] 0b0: Write 0b1 to generate a medium priority medical alarm
			[7:6] 0b00: Always write 0b00
			[5:4] 0b00: Selects the interburst time for medical alarms
			[3:2] 0b00: Selects the pulse off time for medical alarms
			[1:0] 0b00: Selects the pulse on time for medical alarms

Register Settings for the DAC53701 Programmable Comparator With Hysteresis (continued)

Register Address	Register Name	Setting	Description
0xD3	TRIGGER	0x0410	[15:12] 0b0000: Write 0b0101 to unlock the device
			[11] 0b0: Don't care
			[10] 0b1: Write 0b1 to enable the GPI pin
			[9] 0b0: Write 0b1 to load all registers with factory reset values
			[8] 0b0: Write 0b1 to enable continuous waveform generation mode
			[7] 0b0: Write 1 to initiate PMBus MARGIN_HIGH command
			[6] 0b0: Write 1 to initiate PMBus MARGIN_LOW command
			[5] 0b0: Write 0b1 to reload applicable registers with existing NVM settings
			[4] 0b1: Write 0b1 to store applicable register settings to the NVM
			[3:0] 0b0000: Write 0b1010 to reset registers with existing NVM settings or default settings
0x25	DAC_MARGIN_HIGH	0x0998	[15:12] 0b0000: Don't care
			[11:2] 0x266: 10-bit data updates the MARGIN_HIGH code
			[1:0] 0b00: Don't care
0x26	DAC_MARGIN_LOW	0x0334	[15:12] 0b0000: Don't care
			[11:2] 0xCD: 10-bit data updates the MARGIN_LOW code
			[1:0] 0b00: Don't care

Register Settings for the DAC53701 Latching Comparator

Register Address	Register Name	Setting	Description
0xD1	GENERAL_CONFIG	0x0000	[15:14] 0b00: Selects the type of waveform to be generated by the continuous waveform generator (CWG)
			[13] 0b0: Write 0b1 to lock device. Unlock by writing 0b0101 to DEVICE_UNLOCK_CODE field in the PROTECT register
			[12] 0b0: Write 0b1 to enable PMBus mode
			[11:9] 0b000: Selects the code step used for programmable slew rate control
			[8:5] 0b0000: Selects the slew rate used for programmable slew rate control
			[4:3] 0b00: Powers up the device output
			[2] 0b0: Disables the internal reference
			[1:0] 0b00: Selects the gain to be applied to the internal reference
0xD2	CONFIG2	0x0800	[15:14] 0b00: Configures the device I2C address
			[13:11] 0b001: Configures the GPI pin as Power-Up, Down trigger
			[10] 0b0: Write 0b1 to generate a high priority medical alarm
			[9] 0b0: Write 0b1 to generate a medium priority medical alarm
			[8] 0b0: Write 0b1 to generate a medium priority medical alarm
			[7:6] 0b00: Always write 0b00
			[5:4] 0b00: Selects the interburst time for medical alarms
			[3:2] 0b00: Selects the pulse off time for medical alarms
			[1:0] 0b00: Selects the pulse on time for medical alarms

Register Settings for the DAC53701 Latching Comparator (continued)

Register Address	Register Name	Setting	Description
0xD3	TRIGGER	0x0410	[15:12] 0b0000: Write 0b0101 to unlock the device
			[11] 0b0: Don't care
			[10] 0b1: Write 0b1 to enable the GPI pin
			[9] 0b0: Write 0b1 to load all registers with factory reset values
			[8] 0b0: Write 0b1 to start continuous waveform generation output
			[7] 0b0: Write 1 to initiate PMBus MARGIN_HIGH command
			[6] 0b0: Write 1 to initiate PMBus MARGIN_LOW command
			[5] 0b0: Write 0b1 to reload applicable registers with existing NVM settings
			[4] 0b1: Write 0b1 to store applicable register settings to the NVM
			[3:0] 0b0000: Write 0b1010 to reset registers with existing NVM settings or default settings
0x25	DAC_DATA	0x0998	[15:12] 0b0000: Don't care
			[11:2] 0x266: 10-bit data updates the DAC_DATA code
			[1:0] 0b00: Don't care

Pseudo Code Examples

The following shows a pseudo code sequence to program the initial register values for each configuration to the NVM of the DAC53701. The values given here are for the design choices made in the Design Notes.

Pseudo Code Example for Programmable Comparator With Hysteresis

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Power-up the device, internal reference disabled
WRITE GENERAL_CONFIG(0xD1), 0x00, 0x00
//Configure GPI for Margin-High, Low function
WRITE CONFIG2(0xD2), 0x10, 0x00
//Write DAC margin high code
WRITE DAC_MARGIN_HIGH(0x25), 0x09, 0x98
//Write DAC margin low code
WRITE DAC_MARGIN_LOW(0x26), 0x03, 0x34
//Enable the GPI, save settings to NVM
WRITE TRIGGER(0xD3), 0x04, 0x10
```

Pseudo Code Example for Latching Comparator

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Power-up the device, internal reference disabled
WRITE GENERAL_CONFIG(0xD1), 0x00, 0x00
//Configure GPI for Power-Up, Down(10-kΩ) function
WRITE CONFIG2(0xD2), 0x08, 0x00
//Write DAC data code
WRITE DAC_DATA(0x21), 0x09, 0x98
//Enable the GPI, save settings to NVM
WRITE TRIGGER(0xD3), 0x04, 0x10
```

Design Featured Devices

Device	Key Features	Link
DAC53701	10-bit buffered voltage-output smart digital-to-analog converter	ti.com/product/DAC53701
DAC53701-Q1	Automotive 10-bit buffered voltage-output smart digital-to-analog converter	ti.com/product/DAC53701-Q1
DAC43701	8-bit buffered voltage-output smart digital-to-analog converter	ti.com/product/DAC43701
DAC43701-Q1	Automotive 8-bit buffered voltage-output smart digital-to-analog converter	ti.com/product/DAC43701-Q1

Find other possible devices using the Parametric search tool.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, DAC53701 Evaluation Module
- Texas Instruments, *DAC53701EVM User's Guide*
- Texas Instruments, Precision Labs - DACs

For direct support from TI Engineers use the E2E community:

e2e.ti.com

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265