Functional Safety Information

TPS732-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPS732-Q1 (SOT-223 (DCQ), VSON (DRB), and SOT-23 (DBV) packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

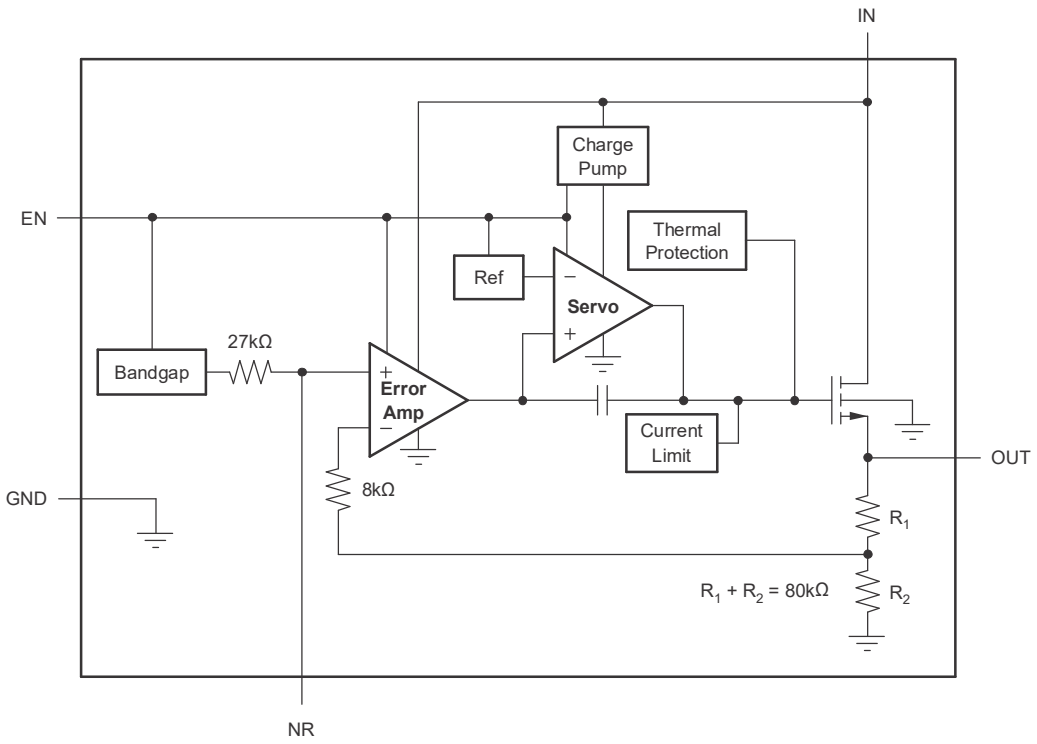

Figure 1-1. Functional Block Diagram

The TPS732-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-223 (DCQ) Package

This section provides functional safety failure in time (FIT) rates for the SOT-223 (DCQ) package of the TPS732-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	3
Package FIT rate	5

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 100mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed = <50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VSON (DRB) Package

This section provides functional safety failure in time (FIT) rates for the VSON (DRB) package of the TPS732-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	2
Package FIT rate	4

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 100mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed = <50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 SOT-23 (DBV) Package

This section provides functional safety failure in time (FIT) rates for the SOT-23 (DBV) package of the TPS732-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	5
Die FIT rate	3
Package FIT rate	2

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 100mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed = <50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS732-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
V_{OUT} high (following V_{IN})	10
V_{OUT} low (no output)	50
V_{OUT} not in specification (Voltage or timing)	35
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS732-Q1 (SOT-223 (DCQ), VSON (DRB), and SOT-23 (DBV) packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2, Table 4-6, and Table 4-10)
- Pin open-circuited (see Table 4-3, Table 4-7, and Table 4-11)
- Pin short-circuited to an adjacent pin (see Table 4-4, Table 4-8, and Table 4-12)
- Pin short-circuited to supply (see Table 4-5, Table 4-9, and Table 4-13)

Table 4-5 through Table 4-13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device operates at free-air temperatures between -40°C and 150°C
- Device operates at an input voltage of at least 1.7V and no more than 5.5V
- Device operates according to all recommended operating conditions and does not exceed the absolute maximum ratings

4.1 SOT-223 (DCQ) Package

Figure 4-1 shows the TPS732-Q1 pin diagram for the SOT-223 (DCQ) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS732-Q1 data sheet.

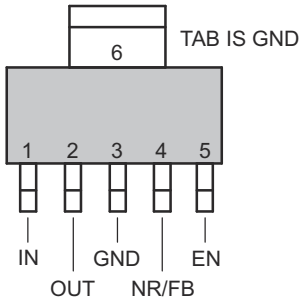

Figure 4-1. Pin Diagram (SOT-223 (DCQ)) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device. System performance depends on upstream current limiting.	B
OUT	2	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B
GND	3	No effect. Normal operation.	D
NR/FB	4	[Fixed Output] The internal reference cannot start. The device cannot turn on.	B
EN	5	The device is disabled, resulting in no output voltage.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No output voltage.	B
OUT	2	Output voltage is disconnected from load.	B
GND	3	Device biasing has no current path. The device is not operational and does not regulate.	B
NR/FB	4	[Fixed Output] Any noise-reduction benefits are lost.	C
EN	5	Device potentially disables.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	OUT	2	Regulation is not possible. $V_{OUT} = V_{IN}$. If V_{IN} exceeds 5.5V, damage is possible.	B
OUT	2	GND	3	Regulation is not possible. The device operates at current limit. The device can cycle in and out of thermal shutdown.	B
GND	3	NR/FB	4	Any noise-reduction benefits are lost.	C
NR/FB	4	EN	5	The output voltage is incorrect.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
OUT	2	Regulation is not possible. $V_{OUT} = V_{IN}$. If V_{IN} exceeds 5.5V, damage is possible.	B
GND	3	No output voltage. System performance depends on the upstream current limit.	B
NR/FB	4	[Fixed Output] NR pin is damaged if V_{IN} is higher than 6V.	A
EN	5	Device is always enabled. Regulation is possible.	B

4.2 VSON (DRB) Package

Figure 4-2 shows the TPS732-Q1 pin diagram for the VSON (DRB) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS732-Q1 data sheet.

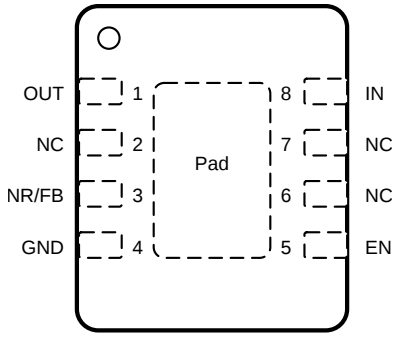

Figure 4-2. Pin Diagram (VSON (DRB) Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B
NC	2	No effect. Normal operation.	D
NR/FB	3	[Adjustable Output] Device stops regulating. V_{OUT} becomes equal to V_{IN} minus dropout because the pass FET is driven as hard as possible.	B
GND	4	No effect. Normal operation.	D
EN	5	The device is disabled, resulting in no output voltage.	B
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Output voltage is disconnected from load.	B
NC	2	No effect.	D
NR/FB	3	[Adjustable Output] Error amplifier input is left floating, output voltage is not equal to set voltage.	B
GND	4	Device biasing has no current path. The device is not operational and does not regulate.	B
EN	5	Device potentially disables.	B
NC	6	No effect.	D
NC	7	No effect.	D
IN	8	No output voltage.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC	2	No effect. Normal operation.	D
NC	2	NR/FB	3	No effect.	D
NR/FB	3	GND	4	[Adjustable Output] Device stops regulating. V_{OUT} becomes equal to V_{IN} minus dropout because the pass FET is always on.	B
GND	4	EN	5	Output is forced OFF, V_{OUT} is 0.0V	B
EN	5	NC	6	No effect. Normal operation.	D
NC	6	NC	7	No effect. Normal operation.	D
NC	7	IN	8	No effect. Normal operation.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible. $V_{OUT} = V_{IN}$. If V_{IN} exceeds 5.5V, damage is possible.	B
NC	2	No effect. Normal operation.	D
NR/FB	3	[Adjustable Output] FB pin is damaged if V_{IN} is higher than 6V. The device having no output voltage is possible.	B
GND	4	No output voltage. System performance depends on the upstream current limit.	B
EN	5	Device is always enabled. Regulation is possible.	B
NC	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
IN	8	No effect. Normal operation.	D

4.3 SOT-23 (DBV) Package

Figure 4-3 shows the TPS732-Q1 pin diagram for the SOT-23 (DBV) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS732-Q1 data sheet.

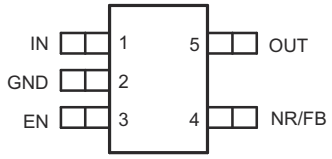

Figure 4-3. Pin Diagram (SOT-23 (DBV) Package)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device. System performance depends on upstream current limiting.	B
GND	2	No effect. Normal operation.	D
EN	3	The device is disabled, resulting in no output voltage.	B
NR/FB	4	[Adjustable Output] Device stops regulating. V_{OUT} becomes equal to V_{IN} minus dropout because the pass FET is driven as hard as possible.	B
OUT	5	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No output voltage.	B
GND	2	Device biasing has no current path. The device is not operational and does not regulate.	B
EN	3	Device potentially disables.	B
NR/FB	4	[Adjustable Output] Error amplifier input is left floating, output voltage is not equal to set voltage.	B
OUT	5	Output voltage is disconnected from load.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	GND	2	Power is not supplied to the device. System performance depends on upstream current limiting.	B
GND	2	EN	3	Output is forced OFF, V_{OUT} is 0.0V.	B
NR/FB	4	OUT	5	[Adjustable Output] V_{OUT} is set to V_{FB}.	B

Table 4-13. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
GND	2	No output voltage. System performance depends on the upstream current limit.	B
EN	3	Device is always enabled. Regulation is possible.	B
NR/FB	4	[Adjustable Output] FB pin is damaged if V_{IN} is higher than 6V. The device having no output voltage is possible.	B
OUT	5	Regulation is not possible. $V_{OUT} = V_{IN}$. If V_{IN} exceeds 5.5V, damage is possible.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2019	*	Initial Release

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