Application Report
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Maximizing SFDR Performance in the GSPS ADC: Spur Sources and Methods of Mitigation

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ABSTRACT

The SFDR performance of an ADC is limited by the largest spur in the spectrum from DC to F_s / 2. These spurs can either be reduced or avoided entirely for maximum SFDR performance, based on the application. This reference design explores the reason behind spurs in the 10-bit and 12-bit GSPS ADC family. The specific products covered are: ADC12D1800RF, ADC12D1600RF, ADC12D1000RF, ADC12D800RF, ADC12D500RF, ADC12D1800, ADC12D1600, ADC12D1000, ADC10D1500, and ADC10D1000. For simplicity, ADC12Dx00RF refers to the ADC12D800RF and ADC12D500RF.

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1 GSPS ADC Architecture Background

This reference design explains how to minimize spurs in the GSPS ADC family in order to achieve the best SFDR performance. To understand the sources of the spurs, understanding the choice of architecture is necessary.

Figure 1 shows typical architectural options for ADCs by sampling rate. The absolute rate that determines the *low* or *high* value changes as technology advances. Higher sampling rates also generally imply lower resolutions. The flash converter is the fastest (ultra-high) architecture and is where the GSPS ADC architecture originates.

Additionally, techniques of folding, interpolating, and interleaving modify the flash architecture to achieve a low-power design which is practical to implement. The basic flash architecture requires 2^N comparators and latches for an N-bit converter. For a 12-bit converter, there are 4096 comparators and latches, which consumes a large amount of power and die area. Folding and interpolating are techniques to reduce and reuse the comparators and latches, which reduces area and power consumption. Interleaving is a technique commonly used to achieve high sample rates.

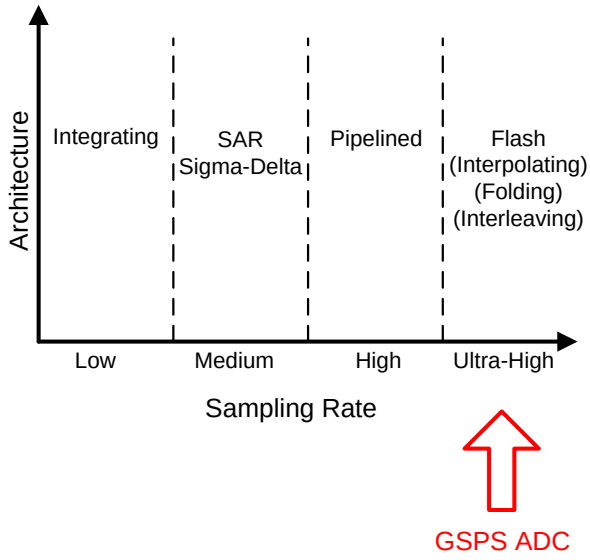

Figure 1. ADC Architecture by Sampling Rate

Figure 2 shows the block diagram for the ADC10D1000 device. Only one interleaved channel is shown, although this device can be interleaved up to four-times (4x) in DES Mode. This diagram shows some of the blocks which affect linearity performance including the track-and-hold, folding, and interpolating.

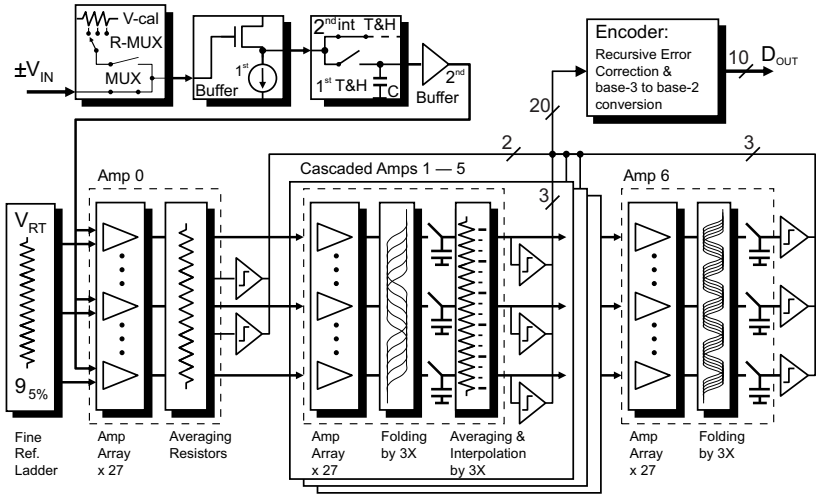

Figure 2. ADC10D1000 Block Diagram

Table 1 lists the functional blocks of the GSPS ADC. Each block is included for a specific reason, such as to achieve the target performance, die size, or sampling rate. However, the use of a block often results in added distortion. For more information on the GSPS ADC architecture, see [1].

Table 1. GSPS ADC Functional Blocks

Block	Description	Pros	Cons
Track-and-hold	Track and hold analog input signal	Improves performance at low F_{IN}	Can reduce maximum sampling rate
Folding	Fold transfer function into sub-ranges	Reduces number of latches to improve power and area	Introduces distortion
Interpolating	Interpolate conversion between series of amplifiers	Reduces number of amplifiers to improve power and area	Introduces distortion
Interleaving	Time-interleave multiple ADC cores	Achieves higher sampling rates	Introduces distortion from mismatch factors
Calibrating	Trim bias currents in linear amplifiers	Reduces distortion	Time offline to calibrate

2 Sources of Spurs

There are several sources of spurs for the GSPS ADC family. These sources include:

- Mismatch between sub-converters in an interleaved ADC architecture
- Coupling from system clocks
- Non-linearities of the ADC

In general, these spurs are categorized into three areas:

- Interleaving spurs
- Fixed frequency spurs
- Input frequency-dependent spurs

2.1 Interleaving Spurs

In order to achieve higher sampling rates, multiple ADCs can be interleaved into a single, composite ADC. Each ADC sub-converter has a certain offset and gain characteristic. The offset is the average code produced by the sub-converter with no analog input. Assuming that the transfer curve of the ADC is linear, the gain is the analog input amplitude which produces the maximum output code.

Figure 3 shows an example of an ideal 4x-interleaved ADC. All four ADCs sample the same analog input signal, 90 degrees out of phase with respect to one another.

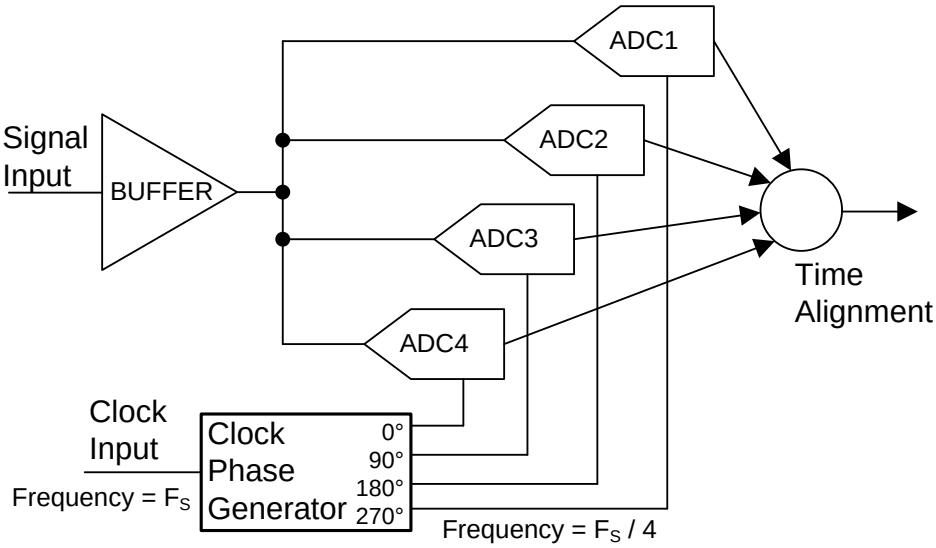

Figure 3. 4x Interleaved Ideal ADC

However, the reality is that interleaving is a non-ideal process. Figure 4 shows the primary sources of mismatch. Gain error, DC offset, and timing skew cause systematic errors in the sampled signal, which result in predictable spurs in the composite spectrum.

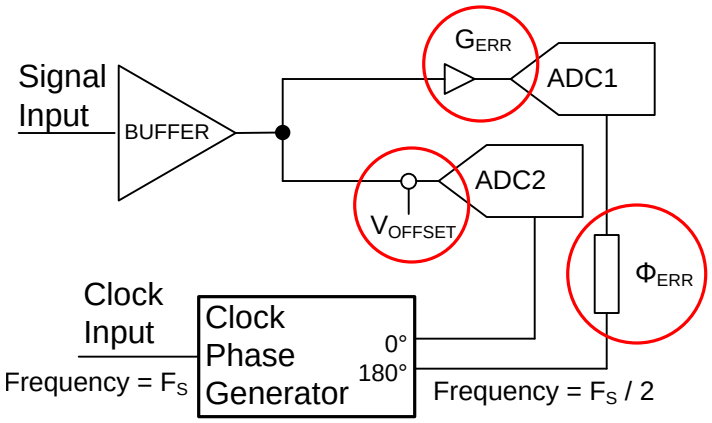

Figure 4. 2x Interleaved Non-Ideal ADC

The GSPS ADC family can have 1, 2, or 4 interleaved sub-converters, based on the device and mode. All of TI's 10-bit and 12-bit GSPS ADCs are dual-channel devices which can be interleaved into a virtual single-channel device that operates at twice the dual-channel sampling rate. This interleaved mode is referred to as *Dual-Edge Sampling Mode* (DES Mode) because one channel is sampled on the rising edge of the sampling clock and the other channel is sampled on the falling edge. *Non-DES Mode* refers to the non-interleaved dual-channel mode. Figure 5 is a typical simplified block diagram for most GSPS ADC datasheets. Figure 5 shows one ADC for the I-channel and one ADC for the Q-channel.

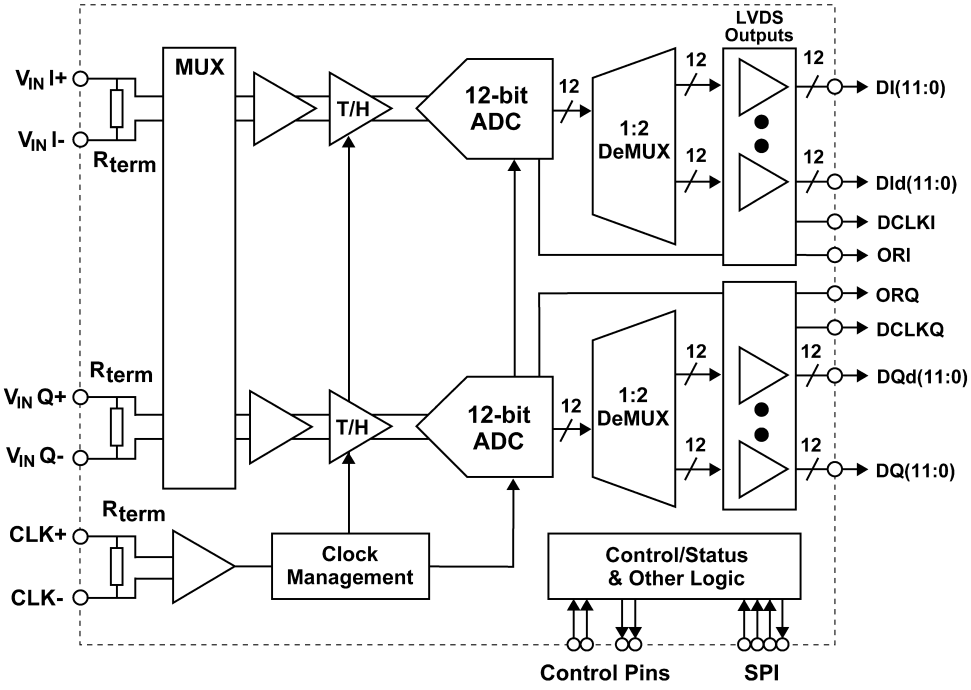

Figure 5. Typical GSPS ADC Block Diagram

In the implementation, however, most of the GSPS ADCs actually have two internally interleaved sub-converters per channel (see Table 2). These two sub-converters are referred to as I_1 and I_2, and Q_1 and Q_2. The ADC12Dx00RF device is a unique product because it has only one converter per channel.

Table 2. Sub-converters Per Product

Product	Sub-converters (Non-DES Mode)	Sub-converters (DES Mode)
ADC10D1500, ADC10D1000	2	4
ADC12D1800, ADC12D1600, ADC12D1000	2	4
ADC12D800RF, ADC12D500RF	1	2
ADC12D1800RF, ADC12D1600RF, ADC12D1000RF	2	4

Note that this reference design is a practical overview of interleaving spurs. There are other effects which can contribute to interleaving spurs, but offset mismatch, gain mismatch, and timing skew cover the first order effects. For detailed information including calculations, other effects contributing to interleaving spurs, and the magnitude of spur which results from the level of each type of mismatch, please see [2].

For a single converter, the FFT results in a spur at DC, which represents the offset of the converter. The application of an input signal, F_{IN}, simply results in a tone at F_{IN} in addition to the spur at DC. Note that the following diagrams only illustrate the locations of spurs and that the magnitude of the spurs is not to scale. An example of a single sub-converter is the ADC12D800RF or ADC12D500RF device in Non-DES Mode.

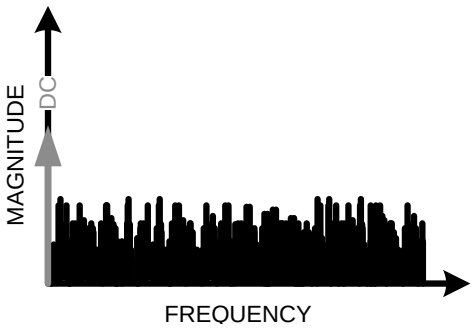

Figure 6. Single Converter With No Input

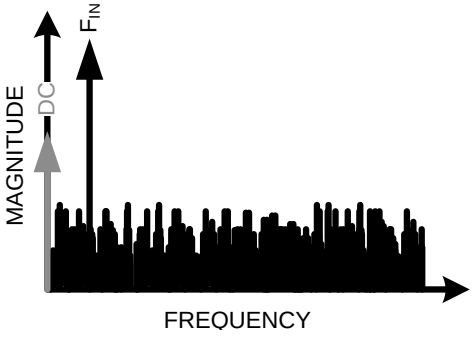

Figure 7. Single Converter With Input

When two sub-converters are interleaved, the offset of each sub-converter is slightly different, that is offset mismatch, which produces a tone at $F_S / 2$. The tone at $F_S / 2$ is in addition to the average offset of the composite interleaved ADC, which produces a tone at DC. Gain mismatch between the two sub-converters produces a tone at $F_S / 2 – F_{IN}$. In an ideal scenario, the two sub-converters sample one after the other with uniform time intervals. Any deviation from this idea scenario is timing skew. Timing skew between the two sub-converters additionally contributes to the tone at $F_S / 2 – F_{IN}$. An example of two interleaved sub-converters is the ADC12D1800, ADC12D1600, or ADC12D1000 device in Non-DES Mode, or the ADC12D800RF or ADC12D500RF device in DES Mode.

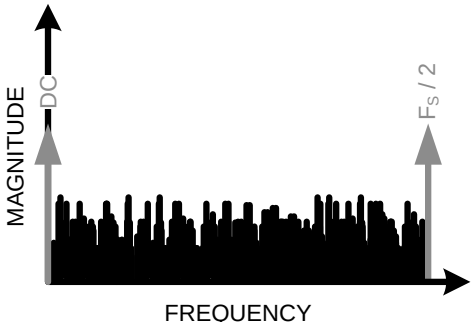

Figure 8. Dual Sub-Converter With No Input

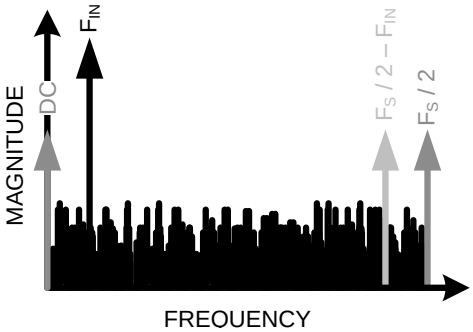

Figure 9. Dual Sub-Converter With Input

Similarly, when an ADC is composed of four interleaved sub-converters, the offset mismatch produces spurs at F_S / 2 and F_S / 4, and the composite offset produces a spur at DC. If the sub-converters sample in time—Bank 1, Bank 2, Bank 3, and Bank 4—the gain mismatch and timing skew between Bank 1 and Bank 3, and between Bank 2 and Bank 4 produces tones at F_S / 4 ± F_{IN}. Gain mismatch and timing skew between the composite (Bank 1 and Bank 3) ADC and the composite (Bank 2 and Bank 4) ADC produces a tone at F_S / 2 – F_{IN}. An example of four interleaved sub-converters is the ADC12D1800, ADC12D1600, or ADC12D1000 device in DES Mode.

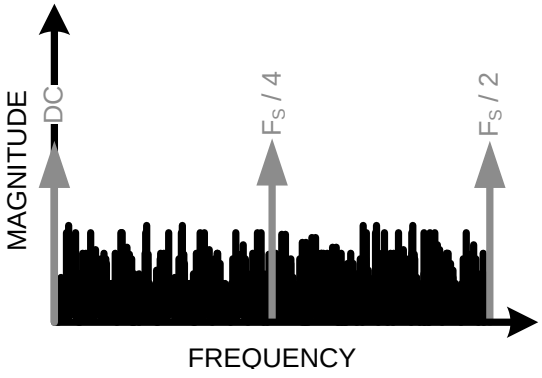

Figure 10. Quad Sub-Converter With No Input

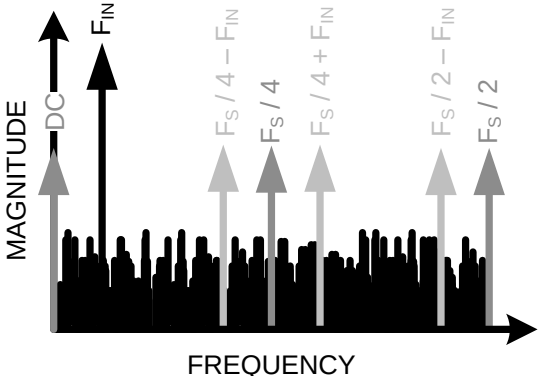

Figure 11. Quad Sub-Converter With Input

Figure 12 is an example FFT of the ADC12D1800RF in DES Mode with an input signal. In this Mode, four sub-converters are interleaved. The interleaving spurs can be seen at F_S / 4 ± F_{IN}, and F_S / 2 – F_{IN}.

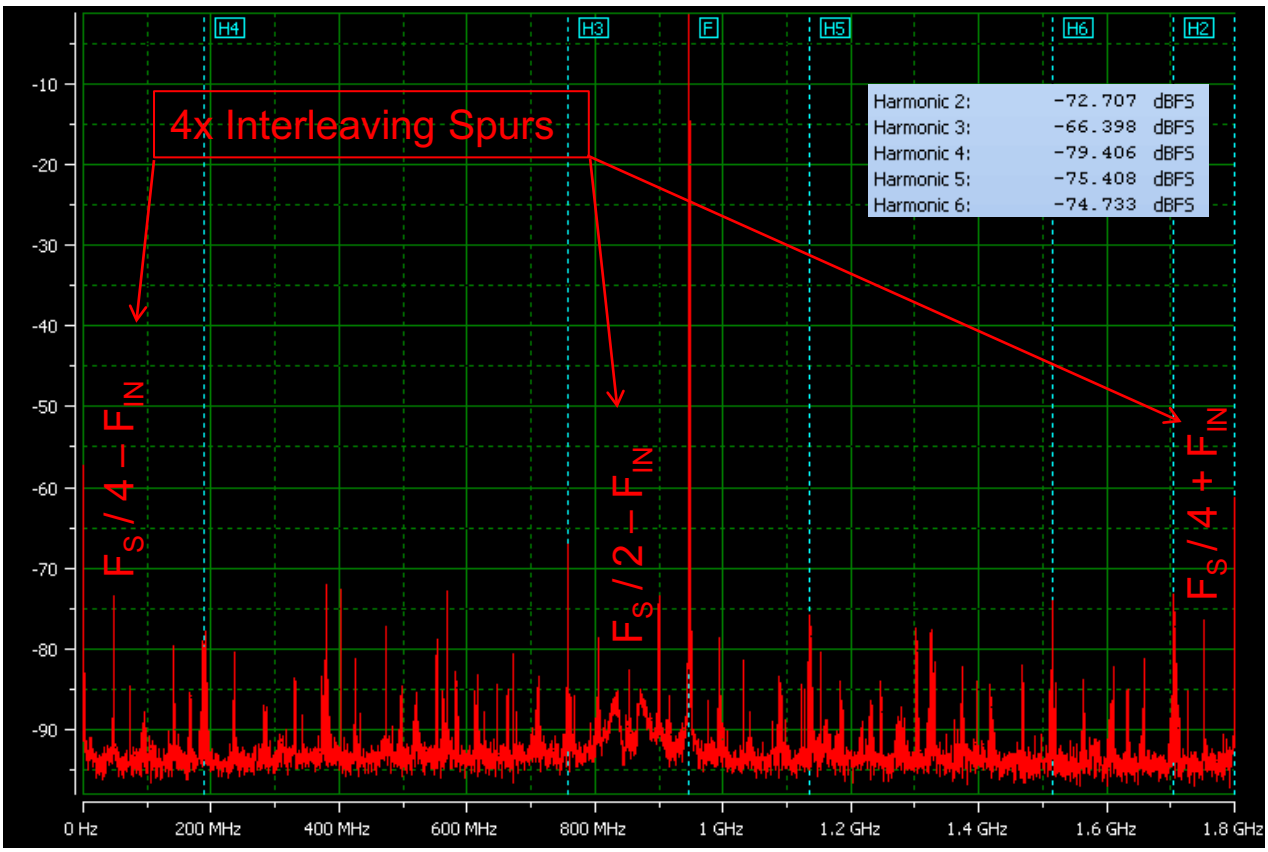

Figure 12. ADC12D1800RF DES-Mode Interleaving Spurs

2.2 Fixed Frequency Spurs

In addition to the spurs which result from offset mismatch in an interleaved ADC, there are also spurs which result from coupling from on-chip clocks. These clocks are the sub-converter sampling clock, the data clock (DCLK), and an additional system clock. These spurs always appear in known fixed-frequency locations which are related to the sampling clock, F_{CLK}. When there are multiple sources of a fixed-frequency spur, the power of that spur is a sum of the power from each source. Because these spurs are predictable, they are simpler to account for in a system design. For example, in a multi-channel application, a fixed-frequency spur can be arranged to land on a channel boundary to avoid interference with system performance.

2.2.1 Fixed Frequency Spurs: the Sub-Converter Clock

Each sub-converter is clocked at F_{CLK} or F_{CLK} / 2, based on the device used. The local sampling clock to each sub-converter can couple to the output, which generates a spur at a fixed frequency related to F_{CLK} (see Figure 13). For example, the ADC10D1000 device has F_{CLK} = 1000 MHz and two sub-converters per channel. These two sub-converters run at F_{CLK} / 2 = 500 MHz. If the ADC is configured into the DES Mode, then F_S = 2000 MSPS and the sub-converter clock coupling into the output appears at F_S / 4, which is 2000 MHz / 4 = 500 MHz. If the ADC is configured into the Non-DES Mode, then F_S = 1000 MHz and the sub-converter clock coupling into the output appears at F_S / 2, which is 1000 MHz / 2 = 500 MHz.

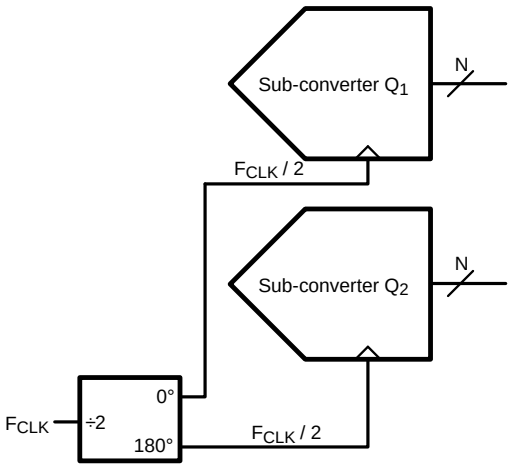

Figure 13. Sub-Converter Clock Coupling

Based on the mode used, such as DES Mode or Non-DES Mode, and the device, this spur is located at DC, F_S / 4, or F_S / 2 (see Table 3).

Table 3. Sub-Converter Clock Spur Location

Product	F_{CLK} (MHz)	Sub-Converters / Channel	Sub-Converter Clock (MHz)	DES Mode Spur Location	Non-DES Mode Spur Location
ADC10D1000	1000	2	500	F_S / 4	F_S / 2
ADC10D1500	1500	2	750	F_S / 4	F_S / 2
ADC12D1000	1000	2	500	F_S / 4	F_S / 2
ADC12D1600	1600	2	800	F_S / 4	F_S / 2
ADC12D1800	1800	2	900	F_S / 4	F_S / 2
ADC12D500RF	500	1	500	F_S / 2	DC
ADC12D800RF	800	1	800	F_S / 2	DC
ADC12D1000RF	1000	2	500	F_S / 4	F_S / 2
ADC12D1600RF	1600	2	800	F_S / 4	F_S / 2
ADC12D1800RF	1800	2	900	F_S / 4	F_S / 2

2.2.2 Fixed Frequency Spurs: the Data Clock

Coupling from the data clock (DCLK) into the output can also contribute to a fixed frequency spur. The frequency at which the spur appears is determined by the output mode. The possible output modes are: Non-Demux Mode (NDM), Demux Mode, single data-rate (SDR), and dual-data rate (DDR). Note that not all of these modes are available on every GSPS ADC (see the respective datasheet for details). In Non-Demux Mode, the data for an N-bit ADC is produced at the output of each channel on an N-bit bus at the sampling rate. In Demux Mode, the data is produced on two N-bit busses at half the sampling rate. The Demux Mode is generally used to ease the difficulty of data capture at high speed by reducing the data rate by half. However, Demux Mode does require twice the number of data busses.

In SDR Mode, the DCLK frequency is the same as the data. Data transitions on either the rising or falling edge of DCLK. In DDR Mode, the DCLK frequency is half of the data rate. Data transitions on both rising and falling edges of DCLK (see Figure 14).

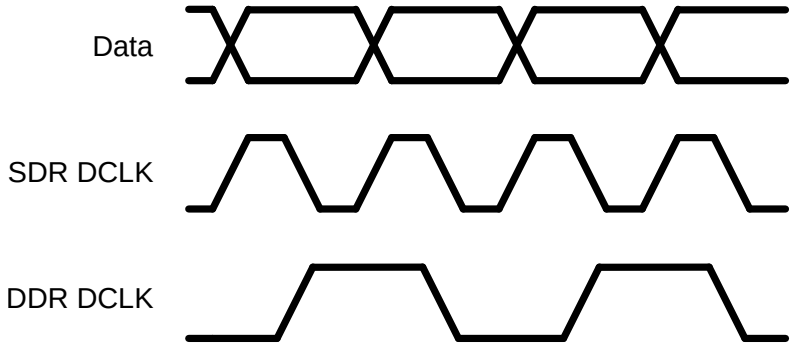

Figure 14. SDR and DDR Modes

For example, if the ADC12D800RF is used in Non-Demux SDR Mode, then DCLK = 800 MHz. If the device is used in the DES Mode, then F_S = 1600 MSPS and the DCLK generates a spur at F_S / 2, which is 1600 MHz / 2. If the device is used in the Non-DES Mode, then F_S = 800 MSPS and the DCLK generates a spur at F_S / 2. Table 4 lists a summary of DCLK Spur Locations.

Table 4. DCLK Spur Location[(1)]

Product	NDM SDR DCLK (MHz)	NDM DDR DCLK (MHz)	Demux SDR DCLK (MHz)	Demux DDR DCLK (MHz)	DES-Mode Spur Locations				Non-DES Mode Spur Locations			
ADC10D1000		500		250		F_S / 4		F_S / 8		F_S / 2		F_S / 4
ADC10D1500		750		375		F_S / 4		F_S / 8		F_S / 2		F_S / 4
ADC12D1000		500		250		F_S / 4		F_S / 8		F_S / 2		F_S / 4
ADC12D1600		800		400		F_S / 4		F_S / 8		F_S / 2		F_S / 4
ADC12D1800		900		450		F_S / 4		F_S / 8		F_S / 2		F_S / 4
ADC12D500RF	500	250	250		F_S / 2	F_S / 4	F_S / 4		F_S	F_S / 2	F_S / 2	
ADC12D800RF	800	400	400		F_S / 2	F_S / 4	F_S / 4		F_S	F_S / 2	F_S / 2	
ADC12D1000RF		500		250		F_S / 4		F_S / 8		F_S / 2		F_S / 4
ADC12D1600RF		800		400		F_S / 4		F_S / 8		F_S / 2		F_S / 4
ADC12D1800RF		900		450		F_S / 4		F_S / 8		F_S / 2		F_S / 4

(1) **Note:** Not all modes are available on each device. The table has been left blank where the mode is unavailable.

2.2.3 Fixed Frequency Spurs: the System Clock

Coupling from another system clock also contributes to a fixed frequency spur. This clock is heavily loaded, so it does contribute a non-negligible spur to the output spectrum. This clock is used for internal circuitry which is related to a proprietary implementation of the architecture. Based on the setting of the LFS bit (Low Frequency Select), the location of the spur is affected.

Table 5. System Clock Spur Location

Product	DES-Mode Spur Location LFS = 0	DES-Mode Spur Location LFS = 1	Non-DES Mode Spur Location LFS = 0	Non-DES Mode Spur Location LFS = 1
ADC10D1000	F_S / 16	F_S / 8	F_S / 8	F_S / 4
ADC10D1500	F_S / 16	F_S / 8	F_S / 8	F_S / 4
ADC12D1000	F_S / 16	F_S / 8	F_S / 8	F_S / 4
ADC12D1600	F_S / 16	F_S / 8	F_S / 8	F_S / 4
ADC12D1800	F_S / 16	F_S / 8	F_S / 8	F_S / 4
ADC12D500RF	F_S / 8	F_S / 4	F_S / 4	F_S / 2
ADC12D800RF	F_S / 8	F_S / 4	F_S / 4	F_S / 2
ADC12D1000RF	F_S / 16	F_S / 8	F_S / 8	F_S / 4
ADC12D1600RF	F_S / 16	F_S / 8	F_S / 8	F_S / 4
ADC12D1800RF	F_S / 16	F_S / 8	F_S / 8	F_S / 4

2.2.4 Fixed Frequency Spurs: An Example

Figure 15 shows an example of a fixed frequency spur. The ADC12D1800RF device is configured into DES Mode with a Demux DDR DCLK and with no analog input signal. For this mode, F_S = 3.6 GSPS. The spur present at 900 MHz = F_S / 4 is visible in the spectrum, although there is no analog input. As listed in Table 3, Table 4, and Table 5, determining the sources of the F_S / 4 spur is possible. In this example, the spur at F_S / 4 is from a combination of the sub-converter clock coupling and the DCLK.

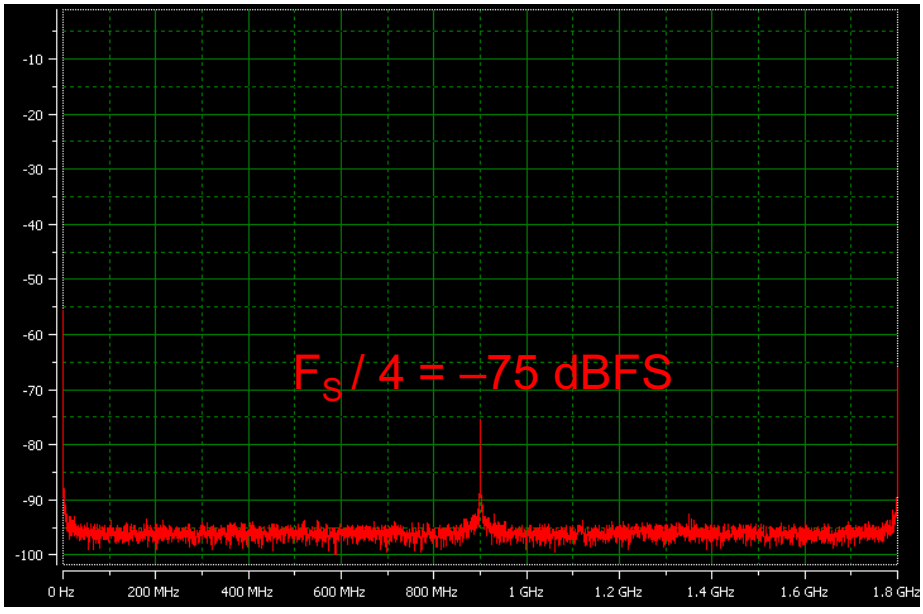

Figure 15. ADC12D1800RF in DES Mode With No Analog Input

2.3 Non-Linearity Spurs

2.3.1 Harmonic Spurs

The source of harmonic distortion in the GSPS ADC is from non-linearities, which are contributions from all of the sources combined and are not individually distinguished. The frequency location is easy to predict (harmonic) but the amplitude of the distortion is not.

Table 6 lists the sources of harmonic distortion. The track-and-hold at the front end of the ADC produces lower-order harmonics of the input signal which roll off with the analog input bandwidth. The power of these harmonics, as related to the power of the input signal follows the standard relationship, such as for an amplifier. Higher-order harmonics are produced in the interpolating, folding architecture and are produced according to the folding-interpolating factor. The levels of these higher-order harmonics follow a non-linear relationship to the power of the input signal. As the higher-order spurs fold back-and-forth in the sampled spectrum, these spurs give the appearance of *grass* just above the noise floor in an FFT. At the output of the ADC, the summed power of the lower-order and higher-order harmonics can be observed together.

Table 6. GSPS ADC Distortion by Source

Source of Distortion	Harmonics Produced	Rolls Off With	Relationship to Input Power
Track-and-hold	Lower-order harmonics	Analog input bandwidth	Standard relationship
Amplifiers in interpolating, folding architecture	Higher-order harmonics	Folding-interpolating factor	Non-linear relationship

The harmonic distortion produced by the track-and-hold follows the standard relationship to input power for a non-linear circuit, the same as an amplifier. First, consider the non-linear system shown in Equation 1.

$$v_o(t) = a_1 V_{IN}(t) + a_2 V_{IN}^2(t) + a_3 V_{IN}^3(t) + a_4 V_{IN}^4(t) + a_5 V_{IN}^5(t) + \ldots \quad (1)$$

For differential circuits, such as track-and-hold, the even harmonics are ideally zero, and $HD_3 >> HD_5$ which is approximated with Equation 2.

$$v_o(t) \cong a_1 V_{IN}(t) + a_3 V_{IN}^3(t) \quad (2)$$

For a sinusoidal input, calculate with Equation 3.

$$V_{IN}(t) = A\cos(\omega t) \quad (3)$$

$$v_o(t) \cong a_1 A\cos(\omega t) + a_3 A^3 \cos^3(\omega t)$$
$$= \underbrace{\left[a_1 A + \frac{3a^3A^3}{4}\right]}_{HD_1}\cos(\omega t) + \underbrace{\left[\frac{a^3A^3}{4}\right]}_{HD_3}\cos(3\omega t) \quad (4)$$

Equation 4 is defined as Equation 5.

$$v_o(t) \equiv HD_1\cos(\omega t) + HD_3\cos(3\omega t)$$
$$HD_1 = a_1 A \qquad HD_3 = \frac{a_3 A^3}{4} \quad (5)$$

Therefore, for the standard non-linear circuit, if the input level, A, is decreased by 1 dB, then HD_3 decreases by 3 dB because HD_1 is proportional to A and HD_3 is proportional to A^3. The track-and-hold follows this relationship and therefore the level of the lower-order harmonics such as HD_2, HD_3, HD_4, HD_5, and others can be strongly influenced by increasing or decreasing input signal power. However, the higher-order harmonics observe a highly non-linear relationship to the input power and higher-order harmonics do not significantly decrease with a decrease of input signal power. Because higher-order harmonics do not significantly decrease, the maximum SFDR, as limited by harmonics, can be achieved at the maximum input signal power.

Figure 16 shows the harmonic level for different input signal levels. The harmonic index was only reported up to HD_{25}, but the harmonics also continue beyond that point. HD_3 is typically the highest level harmonic because it is the lowest-index non-even harmonic. Lower-order harmonics, approximately HD_2 to HD_9 for this example, are dominated by the effect of non-linearities in the track-and-hold, and roll off with the input bandwidth. Higher-order harmonics, HD_2 to HD_{25}, resulting from the folding-interpolating architecture remain present over harmonic index and input level with a fairly consistent range of amplitudes (–85 dBFS, –100 dBFS). The folding-interpolating also generates harmonic content at lower indices down to HD_2, but the effect of the track-and-hold dominates at lower-order harmonics.

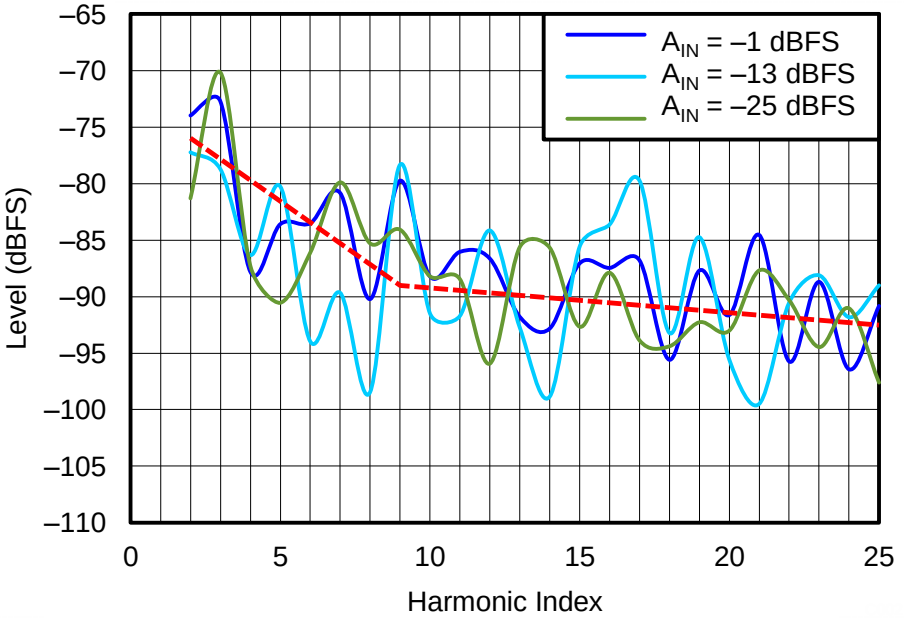

Figure 16. ADC12D1600RF Harmonic Index Versus Level

Figure 17 shows the FFT for the ADC12D800RF with F_S = 800 MSPS and MSPS = 125 MHz. In this case, the SFDR is limited by the HD_3 spur located at 375 MHz to 70 dBc. For this plot the data was processed twice. The blue plot shows the original data that was processed first. For this data, the blue *grass*, which is the harmonic content, can be observed above the noise floor. The same data was processed again (red plot), with the harmonic content mathematically removed by notching a small amount of bins around each harmonic location.

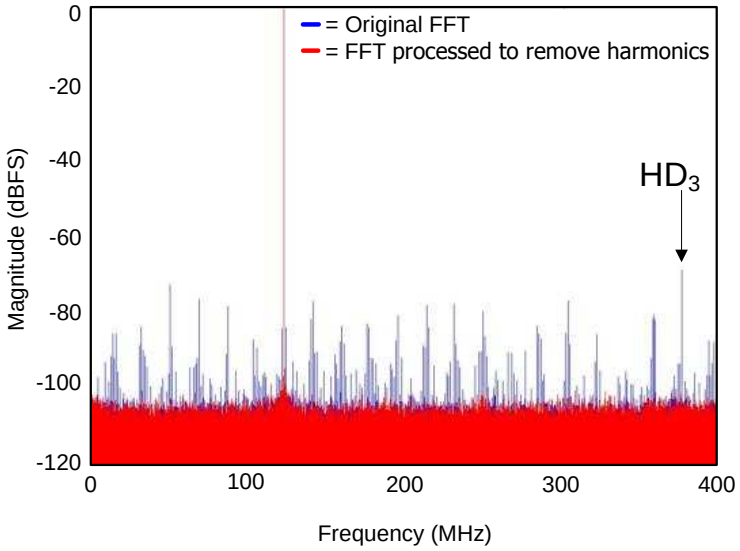

Figure 17. ADC12D800RF Single-Converter Harmonic Spurs

Figure 18 shows the FFT for the ADC12D1000RF with F_S = 1000 MSPS and MSPS = 125 MHz. This ADC has two sub-converters, each running at 500 MSPS and interleaved to achieve an overall 1000 MSPS. For this case, the worst spur is from gain mismatch and timing skew between the sub-converters which results in a spur at $F_S / 2 – F_{IN}$.

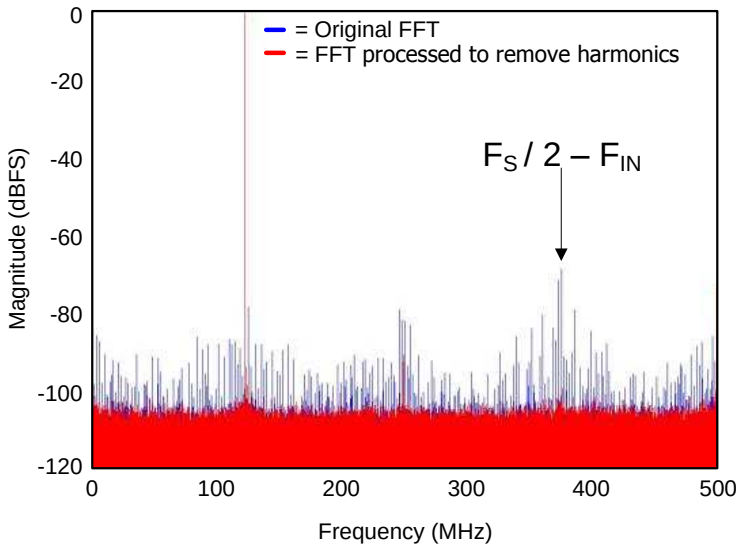

Figure 18. ADC12D1000RF Dual Sub-Converter Harmonics

Note that for both FFTs in Figure 17 and Figure 18, the ADC is performing under worst-case conditions for this particular architecture (such as a single, CW tone). A wideband input signal results in less spurious content generated because transitions on the transfer curve are more random. Therefore, evaluating wideband applications under actual operating conditions, not only with a CW test tone, is important.

2.3.2 Third-Order Intermodulation Distortion

Although there are actually four third-order intermodulation distortion products (IMD_3), only the two close-in ones are typically considered because these are the terms which are difficult to filter out from the band of interest. For input frequencies at f_1 and f_2, the IMD_3 terms are located at $2f_2 - f_1$ and $2f_1 - f_2$, see Figure 19. f_1 and f_2 are shown at different levels to exaggerate the difference between them, but in practice they are set to the same level. IMD_3 is defined with Equation 6.

$$IMD_3 = \min(f_1, f_2) - \max(2f_2 - f_1, 2f_1 - f_2) \quad (6)$$

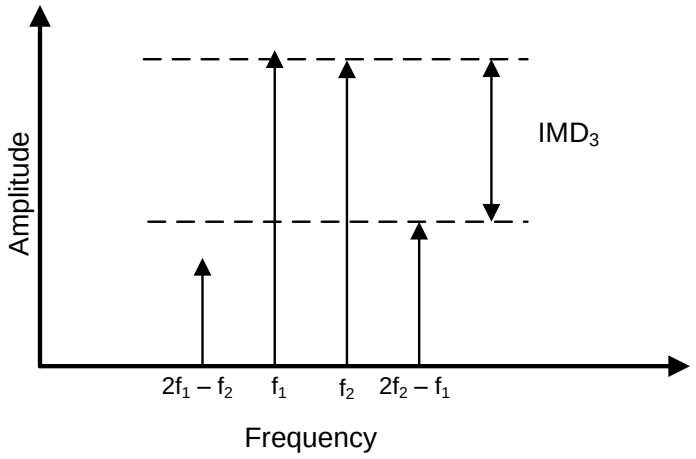

Figure 19. Close-In IMD_3

Figure 20 shows the IMD_3 for the ADC12D1800RF at various input levels. The results are less linear for lower-input amplitude signals, as well as lower-input frequencies. The less-linear results occur because for higher input frequencies and levels, the IMD_3 is most strongly a function of the track-and-hold. Because IMD_3 is primarily a function of the analog input, IMD_3 performance, as shown in Figure 20, is similar for the ADC12D1600RF, ADC12D1000RF, ADC12D800RF, and ADC12D500RF.

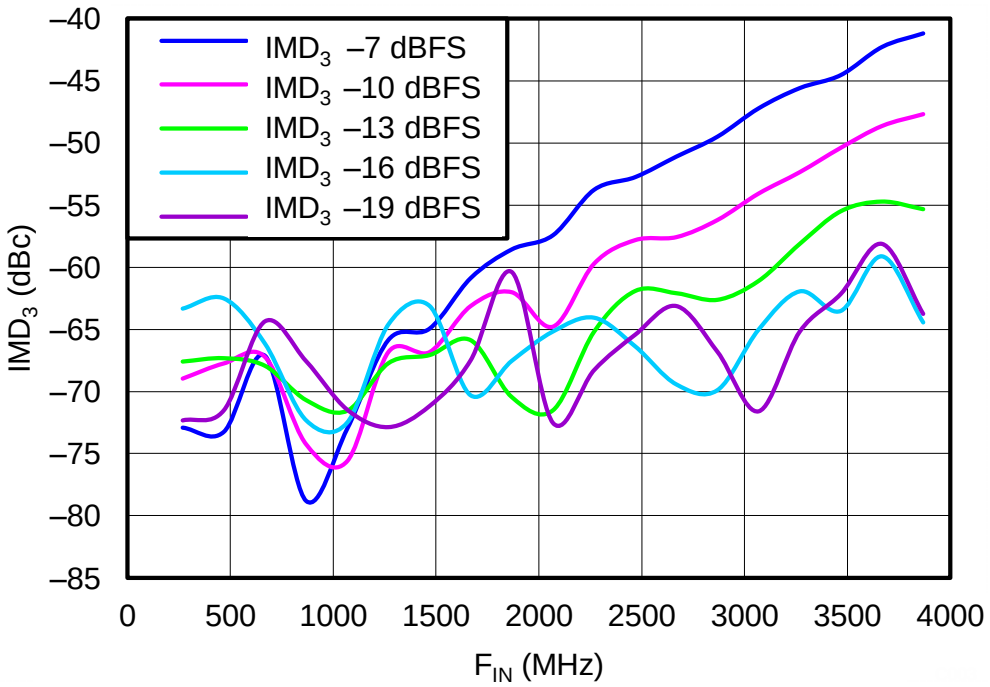

Figure 20. ADC12D1800RF IMD_3

3 Methods of Mitigation

A number of options are available to minimize any spurs and maximize the SFDR performance. These options include features of the GSPS ADC, digital correction, frequency planning, dithering the input, and systems solutions.

3.1 ADC Features

The GSPS ADCs include certain features which can minimize spurs, such as calibration, offset adjust, full-scale range adjust, duty cycle correct, DES timing adjust, and sub-converter timing adjust. Note that not every feature is available on every ADC (see Table 7).

Calibration— This feature is designed to trim the analog input differential termination resistors, the CLK input resistor, and set internal bias currents which affect the linearity of the converter. Calibrating minimizes full-scale error, offset error, DNL and INL. Calibration must be run in order to achieve the full rated performance because it is the principal feature used to maximize SFDR.

I-channel and Q-channel offset adjust—The offset for each I-channel and Q-channel can be adjusted independently with 15-bits of precision. However, individual sub-converter offset adjust is not available on every device. This feature can be used to correct for any residual offset error between the I-channel and Q-channel which would result in a spur at $F_S / 2$.

I-channel and Q-channel FSR adjust—The input full-scale range for each I-channel and Q-channel may be adjusted independently with 12-bits of precision plus polarity. However, individual sub-converter FSR adjust is not available on every device. This feature is used to correct for any residual gain error between the I-channel and Q-channel which results in a spur at $F_S / 2 – F_{IN}$.

Duty Cycle Correct—The Sampling Clock phase between the I-channel and Q-channel is automatically and continuously adjusted in the background. The Duty Cycle Correct feature addresses the variable component of the clock phase error in DES Mode. The feature is enabled by default and TI recommends to leave the feature enabled.

DES timing adjust—The Sampling Clock phase between the I- and Q-channel can be adjusted manually from the nominal mid-range setting. Using the DES Timing Adjust feature addresses the residual static timing skew offset of the clock phase error in DES Mode.

Table 7. ADC Features to Address Spurs

Feature	ADC10D1x00	ADC12D1x00	ADC12Dx00RF	ADC12D1x00RF	DES Mode Spurs Addressed
Calibration	Yes	Yes	Yes	Yes	DC, $F_S / 4$, $F_S / 2$, $F_S / 2 – F_{IN}$, $F_S / 4 \pm F_{IN}$
I/Q-channel offset adjust	Yes	Yes	Yes	Yes	$F_S / 2$
I/Q-channel FSR adjust	Yes	Yes	Yes	Yes	$F_S / 2 – F_{IN}$
Duty cycle correct	Yes	Yes	Yes	Yes	$F_S / 2 – F_{IN}$
DES timing adjust	No	Yes	Yes	Yes	$F_S / 2 – F_{IN}$

Calibration is the main feature of the GSPS ADC to linearize the performance. For example, Figure 21 shows the ADC12D1800RF device in Non-DES Mode with and without calibration for F_{IN} = 997.47 MHz. Calibration yields a performance improvement in over 2 ENOB. The un-calibrated performance with calibration vectors reset to the default values, as shown in Figure 21, is not typically seen because the ADC performs a calibration upon power-up. However, performing another calibration after applying the desired mode and allowing for self-heating is necessary to achieve the optimized performance.

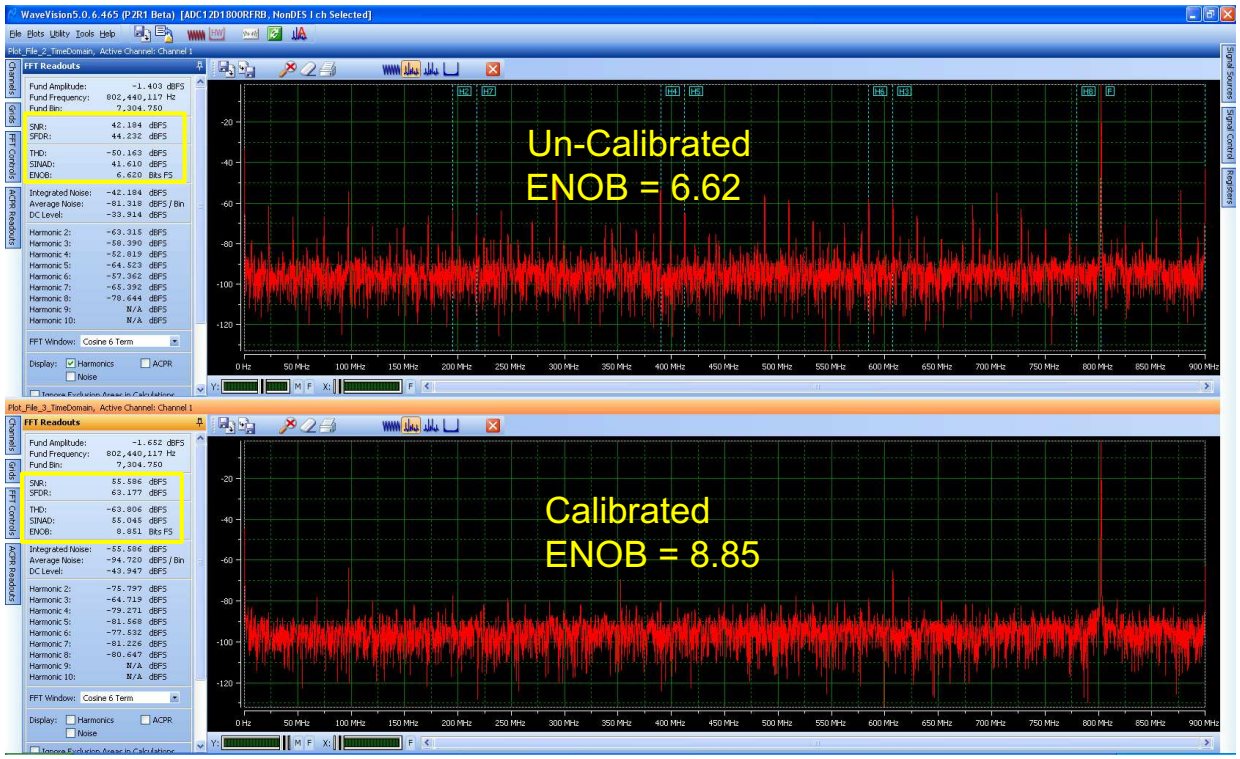

Figure 21. ADC12D1800RF With and Without Calibration

The DES Timing Adjust is a good example of an analog correction of interleaving spurs on the GSPS ADC. Figure 22 shows that as the timing codes are changed, the magnitude of the DES timing spur, located at $F_S / 2 - F_{IN}$, decreases with the decreasing timing skew. Each code skews the sample instant of the I-channel, with respect to the Q-channel. At the relative minimum point, the DES timing spur is 13 dB less than the next highest spur, which is HD_3.

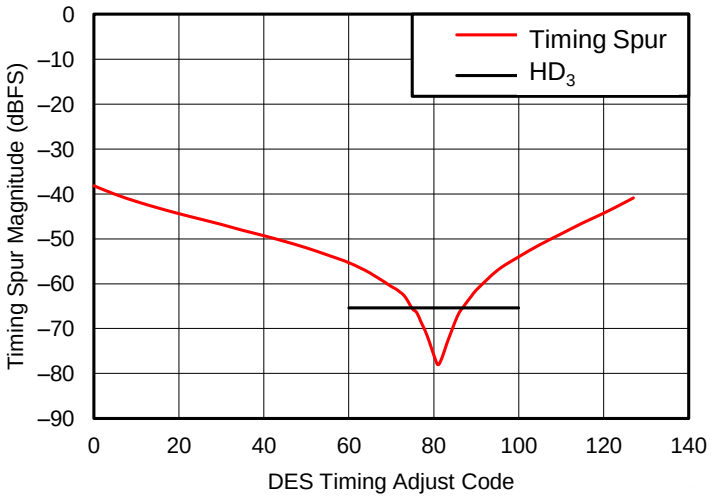

Figure 22. ADC12D1800RF DES Timing Code Versus Spur Magnitude

3.2 Digital Correction

While the GSPS ADCs offer features to enable analog correction of interleaving spurs, using digital correction to address interleaving spurs is also possible. For resolutions greater than 8 bits, achieving the level of matching required for analog correction is a challenge. One drawback to analog correction is that a feature setting, which optimizes the performance under a given set of conditions such as temperature or analog input frequency, may not be optimal at a different temperature or input frequency.

For digital correction, the errors can be estimated and corrected with coefficients by post-processing the data. The algorithm detects the errors in either the time or frequency domain, and converge on correction coefficients. Digital correction adds complexity to the system, but can also optimize performance under a wider variety of operating conditions.

3.3 Frequency Planning

Frequency planning is used to ensure that lower-order harmonics do not interfere with the band of interest. TI offers a tool called the ADC Harmonic Calculator to determine the location of harmonics (see the tool folder for more information and to download the calculator, www.ti.com/tool/adc-harmonic-calc). This tool, however, does not include the effect of harmonics and interleaving. Figure 23 shows an example of how to plan around lower-order harmonics for the ADC12D1800 in DES Mode. The input signal bandwidth is 60 MHz centered at 1000 MHz and no harmonic falls back into the band of interest until HD_6. Frequency planning works well for applications which are over-sampled.

	Inputs Here
Signal BW	60.00
Filter BW	100.00
Signal Center Freq	1000.00
ADC Sample Rate	3600.00

Results									
	Signal	HD_2	HD_3	HD_4	HD_5	HD_6	HD_7	HD_8	HD_9
Min Freq	1030	1700	750	600	1650	1500	550	1200	1800
Max Freq	970.6	1500	450	200	1150	900	3	400	350
Overlaps signal		0	0	0	0	1	0	1	0

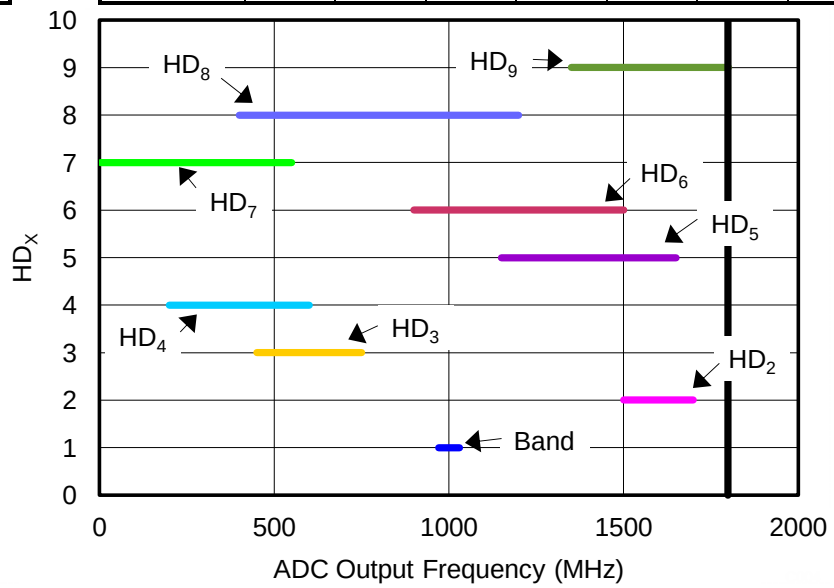

Figure 23. Example of Frequency Planning

3.4 Dithering the Input

Adding dither the analog input signal can improve harmonic performance by randomizing transitions across the ADC transfer function. However, adding dither to the input signal reduces the maximum input signal level which can be applied before clipping the ADC. If the dither is added as band-limited white noise to the spectrum outside the band of interest, then the dither can easily be filtered out. See Figure 24 and Figure 25 for an example. Table 8 lists improvements in harmonic distortion. Dithering the input only reduces the level of the harmonics, but does not affect the interleaving spurs.

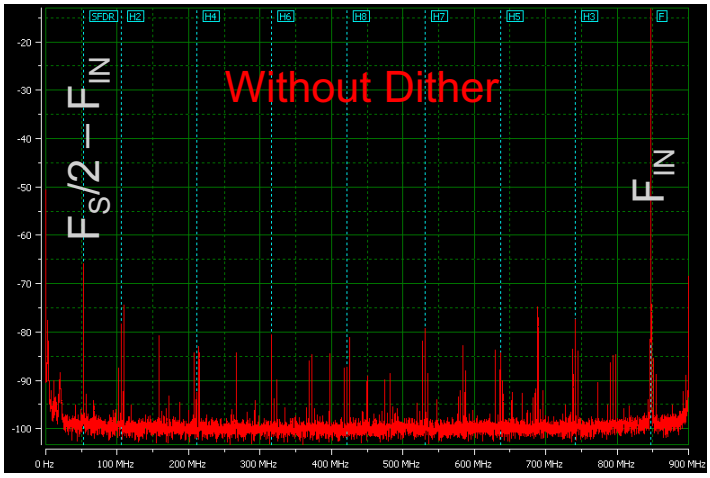

Figure 24. ADC12D1800RF Without Dither

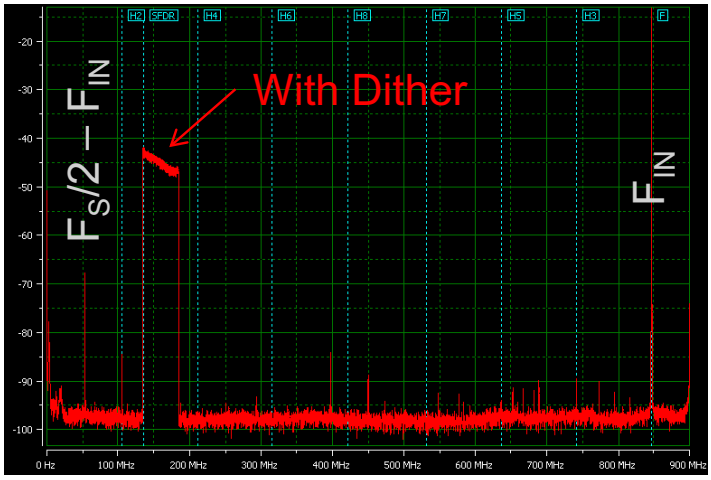

Figure 25. ADC12D1800RF With Dither

Table 8. Improvements in Harmonic With Dither Example: ADC12D1800RF A_{IN} = –13 dBFS

Harmonic	No Dither (dBc)	With Dither (dBc)	Improvement (dB)
HD_2	–65	–70	5
HD_3	–64	–74	10
HD_4	–77	–77	0
HD_5	–70	–75	5
HD_6	–67	–77	10
HD_7	–66	–78	12

3.5 Systems Solution by Application

Some fixed frequency spurs from the DCLK, offset mismatch, and sub-converter clock can be addressed by carefully choosing the DCLK Mode, system architecture, and GSPS ADC selection.Table 9 lists some examples of system solutions.

Table 9. System Solutions

Example	Spur Source	Solution
A spectrum analyzer uses the ADC12D800RF interleaved and cannot tolerate a strong spur in the middle of the spectrum.	DCLK running in Demux SDR Mode causes a spur at F_S / 4	Iinstead choose the Non-Demux SDR DCLK, which moves the spur to F_S / 2.
A wideband communications application uses the ADC12D1800RF interleaved to achieve high sampling bandwidth.	DCLK produces spur at F_S / 8 or F_S / 4	Adjust the sampling clock so that the fixed-frequency spurs land on channel boundaries.
	Offset mismatch spur at F_S / 4	
	Sub-converter clock spur at F_S / 4	
A long-range tactical radar with F_S = 750 MSPS cannot tolerate interleave images .	Most members of the GSPS ADC family have interleaved channels, which produce image spurs	Use the ADC12D800RF, which has only one converter per channel.

4 Conclusion

In order to achieve high-resolution, high-sampling rate ADCs, certain techniques were chosen which also resulted in spurious content. The impact of spurs on system performance can be minimized with a better understanding of the spurs. Spurs in the GSPS ADC family occur because of non-linearities, interleaving, and system clocks. Techniques to address these spurs include ADC features such as calibration, use of dithering, digital correction, and frequency planning. Input signals that consist of multiple wideband or CW tones act like dither and reduce the impact of non-linearities. Therefore testing with single CW-tone inputs may not adequately or relevantly show performance for an actual application. Table 10 lists a summary of spurious sources and solutions.

Table 10. Solutions Recommendations

Spur	Dominant Source	Solution
Lower-order harmonics	Non-linearity in track-and-hold	Calibration
		Frequency planning
Higher-order harmonics	Folding-interpolating architecture	Calibration
		Dithering
IMD_3	Non-linearity in track-and-hold, folding-interpolating architecture	
DC, F_S / 4, F_S / 2	Sub-converter offset mismatch in interleaving architecture	ADC selection
		ADC features
		Digital correction
F_S / 2 – F_{IN}, F_S / 4 ± F_{IN}	Sub-converter gain mismatch and timing skew in interleaving architecture	
F_S / 8, F_S / 4, F_S / 2	Coupling from DCLK	DCLK selection
DC, F_S / 2	Coupling from sub-converter clock	ADC selection

5 References

1. *A 1.8V 1.0Gsps 10b Self-Calibrating Unified-Folding-Interpolating ADC with 9.1 ENOB at Nyquist Frequency* (Taft 2009)
2. *Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems* (Kurosawa 2002)

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