Application Report
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Migrating From MSP430FW42x Scan Interface to MSP430FR6x8x/FR5x8x Extended Scan Interface

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ABSTRACT

The purpose of this application report is to facilitate the migration of designs based on the MSP430FW42x Scan Interface (SIF) to the MSP430FR5xx/FR6xx Extended Scan Interface (ESI). This document describes the main differences between the two peripheral modules and provides migration solutions covering both software and hardware aspects.

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1 Scan Interface and Extended Scan Interface Comparison Overview

Table 1 gives an overview about the differences between MSP430FW42x's Scan Interface and MSP430FR5xx/6xx's Extended Scan Interface.

Table 1. Differences Between MSP430FW42x's Scan Interface and MSP430FR5xx/6xx's Extended Scan Interface

Feature	MSP430FW42x's Scan Interface	MSP430FR5xx/FR6xx's Extended Scan Interface
Analog front ends	AFE	AFE1 and AFE2
PSM table	Located in general-purpose memory	Located in dedicated RAM (128 Bytes). CPU access protection while in PSM operation.
Number of inputs for processing within PSM	2 inputs signals	2 or 3 input signals
Threshold DAC resolution	10-bits	12-bits
Number of registers available for sequence definition	24 registers	32 registers
Recalibration algorithm for DAC threshold	Test cycle insertion. Time measurement by Timer_A connection.	Test cycle insertion. Time measurement by Timer_A connection. Using AFE2 for recalibration in background.
Integrated counters	SIFCNT1 used as up, down, or up-and-down counter. SIFCNT2 used as down counter.	ESICNT0 used as up counter. ESICNT1 used as up and down counter. ESICNT2 used as down counter.
Counter interrupt generation	Only fixed delta counts (1, 4, 64, or 256)	For up and down counter: freely programmable. Up counter and down counter: fixed delta counts(1, 4, 256, or 65536).
Processing state machine after startup	Start state depends on AFE current status	Dedicated “Reset State: S0”; next state depends on AFE status
Analog auxiliary/test outputs	Taken directly from 10-bit DAC	Taken from 8 bit coarse DAC (of 8 bit + 4 bit =12-bit cascaded DAC)

2 Scan Interface to Extended Scan Interface Migration – Hardware Considerations

This section discusses the differences between the SIF and ESI hardware.

2.1 Oscillator Within Timing State Machine (TSM) Submodule

Both the Scan Interface (SIF) and Extended Scan Interface (ESI) have an RC oscillator within their TSM submodule. While the SIF oscillator is usually configured to generate a frequency of either 1 MHz or 4 MHz, the ESI oscillator is adjusted to 4.8 MHz. For this frequency, the data sheet provides minimum and maximum parameters that considers supply voltage and temperature changes. This helps to design for a worst-case scenario that can ensure all settling times are met. Therefore, recalibrating the ESI oscillator frequency during runtime is not needed.

The ESI oscillator uses six instead of four control bits to adjust its output frequency. This allows adjustment of a wider frequency range and with a higher resolution. Note that the 1-MHz output frequency can only be realized with ESI by using the ESIDIV1x divider.

The ESI oscillator has a nonmonotonic characteristic. This must be considered when adjusting the oscillator by using software regulation loops.

Another important parameter is the start-up time of the oscillator. The ESI oscillator starts up within 100 ns, but the specified start-up time also includes synchronization clock cycles. The start-up time and synchronization clock cycles must be considered when defining a TSM sequence, especially when switching from one TSM state that uses ACLK to another TSM state in which the ESI oscillator is used.

2.2 Timing State Machine (TSM)

The ESI's timing state machine (TSM) looks similar to the SIF's TSM. There are just few minor updates:

- ESI has also a software trigger to start a TSM sequence beside the divided ACLK signal.
- The number of TSM registers used to define the TSM sequence was increased from 24 to 32 registers.
- ESI uses more synchronization clock cycles when switching from one TSM state that uses ACLK to another state that uses ESI oscillator.
- ESI allows using an optional control bit that allows to introduce a comparator offset cancellation sequence (autozero).

2.3 AFE Comparator

A major change within ESI is the introduction of a second analog front end. Both analog front ends (AFE1 and AFE2) have an own comparator. The differences of ESI's comparators compared with SIF's comparator are:

- Input offset voltage looks similar. However, ESI allows doing an offset cancellation (autozero) that reduces offset voltage.
- Common mode input voltage range is improved on ESI. It is going down to 0 V that especially supports LC-sensor solutions (detection of negative half waves).
- The ESI comparator settle time is only identical to SIF's solution for higher supply voltages (>2.7 V). For lower supply voltages, the comparator settle time is higher (see the device-specific data sheet).

2.4 AFE DAC

As mentioned in previous chapter, the ESI has two analog front ends AFE1 and AFE2. Both analog front ends have a dedicated DAC. The differences between the ESI DACs and the SIF DAC are:

- ESI's DACs have a resolution of 12-bit. Both DACs are cascaded as a 8-Bit DAC and 4-Bit DAC. SIF DAC has a resolution of 10-bit.
- SIF DAC uses supply voltage V_{CC} as its reference voltage. ESI uses $0.8 \times V_{CC}$ as reference voltage for its DAC. This ensures that the ESI's DAC operational range is nearly the same as the comparator's common mode input voltage range.
- The outputs ESITEST1 and ESITEST2 are connected to the 8-bit coarse DACs.

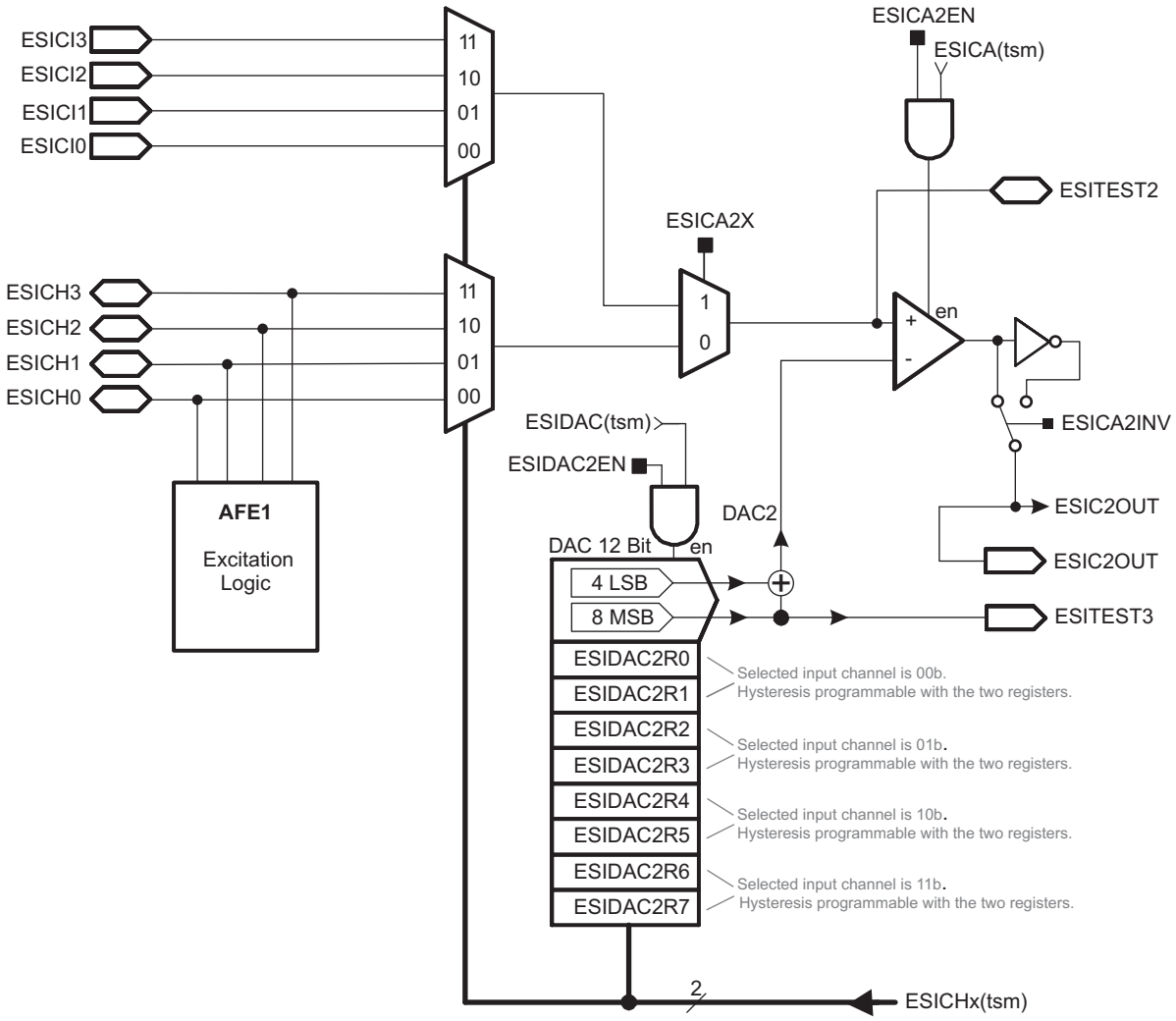

Figure 1. ESI AFE Block Diagram

2.5 Processing State Machine (PSM)

The ESI's programmable sequential machine is identical to the one that is used in SIF. Only the inputs and outputs of this sequential machine are upgraded:

- ESI optionally allows the use of three sensor input signals (PPUSx signals).
- The ESI-PSM table is stored in ESI RAM. The ESI PSM starts always the start address of ESI RAM (State S0). The SIF-PSM has entry points that depends on the input signals. The states S0, S1, S2, and S3 are therefore reserved as cluster states for reset.
- ESI does not use the Q7 bit for next state calculation; bit 7 of the next state latch is always 0. ESI allows using the Q7 bit for interrupt generation or as the trigger signal for storage of the next state latch vector.
- ESI's PSM has three 16-bit counters. Each counter has its own counter register and each counter can be cleared by its own counter reset bit.
- There are two 16-bit programmable thresholds for ESICNT1 counter that allows to define when an interrupt should be generated. Two thresholds are programmable to cover up- and down-counting.

3 Scan Interface to Extended Scan Interface Migration – Software Considerations

This section provides some advise for converting software written for Scan Interface (SIF) to Extended Scan Interface (ESI).

3.1 Control Registers

Table 2 describes in which ESI control registers the appropriate SIF functionality can be found. In general, the ESI control bit names begin all with “ESI” instead of “SIF”. Furthermore, some control bit names were changed (for example, SIFCAX are now called ESICA1X and ESICA2X to highlight the functionality within the different analog front ends, AFE1 and AFE2).

Table 2. Control Registers

Scan I/F Control Registers and Control Bits (marked with “.”)	Extended Scan I/F Control Register Covering SIF Functionality	Comments
SIFDEBUG	ESIDEBUG1, ESIDEBUG2, ESIDEBUG3, ESIDEBUG4, ESIDEBUG5	SIF allows access to different information by writing different numbers into SIFDEBUG. ESI splits up this information in different registers.
SIFCNT	ESICNT1, ESICNT2	SIFCNT1 and SIFCNT2 values are both available in register SIFCNT. ESI has separated registers to access counters.
- - -	ESICNT0	ESI has one additional 16-bit counter.
SIFPSMV	- - -	Pointer register does not exist for ESI. Start address of the PSM table is always ESI RAM start address (see the *Peripheral File Map* section in the device-specific data sheet).
SIFCTL1: .SIFIE6, .SIFIE5, .SIFIE4, .SIFIE3, .SIFIE2, .SIFIE1, .SIFIE0	ESIINT1	ESI has two additional interrupt enable bits.
SIFCTL1: .SIFIFG6, .SIFIFG5, .SIFIFG4, .SIFIFG3, .SIFIFG2, .SIFIFG1, .SIFIFG0	ESIINT2	ESI has two additional interrupt flag bits.
- - -	ESIIV	ESI has an interrupt vector register that allows to easily find the source of interrupt within the interrupt service routine.
SIFCTL1: .SIFTESTD, .SIFEN	ESICTL	
SIFCTL2: .SIFDACON, .SIFCAON	- - -	ESI's AFE1 DAC and comparator can only be controlled by the ESITSMx control registers. For AFE2, there are ESI control bits that allow to enable control of AFE2 DAC and comparator by ESITSMx.
SIFCTL2: .SIFCAINV, .SIFCAX	ESIAFE	ESI allows to control these settings for AFE1 and AFE2.
SIFCTL2: .SIFCISEL, .SIFTEN, .SIFCACI3, .SIFVSS, .SIFVCC2, .SIFSH	ESIAFE	

Table 2. Control Registers (continued)

Scan I/F Control Registers and Control Bits (marked with ".")	Extended Scan I/F Control Register Covering SIF Functionality	Comments
SIFCTL2: .SIFTCH1x, .SIFTCH0x	ESICTL	
SIFCTL2: .SIFTCH1OUT, .SIFTCH0OUT	ESIPPU	
SIFCTL3: .SIFS2x, .SIFS1x	ESICTL	ESI allows to select three PSM input signals.
SIFCTL3: .SIFIS2x, .SIFIS1x - - -	ESIINT2 ESITHR1, ESITHR2	ESI allows selection of the interrupt trigger signal only for ESICNT0 and ESICNT2. ESICNT3 generations interrupt based on user-programmable thresholds.
SIFCTL3: .SIFCS	ESICTL	
SIFCTL3: .SIFIFGSETx	ESIINT1	ESI allows defining separately interrupt sources for AFE1 and AFE2.
SIFCTL3: .SIF3OUT, .SIF2OUT, .SIF1OUT, .SIF0OUT	ESIPPU	
SIFCTL4: .SIFCNTRST	ESIPSM	Each ESI counter has its own counter reset control bit.
SIFCTL4: .SIFCNT2EN, .SIFCNT1ENM, .SIFCNT1ENP	ESIPSM	ESI has separated up- (ESICNT0), down- (ESICNT2), and up and down (ESICNT1) counters.
SIFCTL4: .SIFQ7EN	- - -	ESI cannot use Q7 bit for next state calculation.
SIFCTL4: .SIFQ6EN	ESIPSM	
SIFCTL4: .SIFDIV3Bx, .SIFDIV3Ax, .SIFDIV2x, .SIFDIV1x	ESITSM	
SIFCTL5: .SIFCNT3x	ESICNT3	
SIFCTL5: .SIFTSMRP	ESITSM	
SIFCTL5: .SIFCLKFQx, .SIFCLKGON, .SIFCLKEN	ESIOSC	ESI has 6 ESICLKFQx control bits instead of 4 SIFCLKFQx bits. SIFCLKEN is called ESIHFSEL on ESI.
SIFCTL5: .SIFFNOM	- - -	This bit does not exist on ESI. In case 1 MHz TSM clock is needed, the divider ESIDIV1x may be used.
SIFDACRx (x=0…7)	ESIDAC1Rx (x=0…7) ESIDAC2Rx (x=0…7)	ESI has two DACs: one within each analog front end.

Table 2. Control Registers (continued)

Scan I/F Control Registers and Control Bits (marked with ".")	Extended Scan I/F Control Register Covering SIF Functionality	Comments
SIFTSMx (x=0...23)	ESITSMx (x=0…31)	ESI has in total 32 control registers. Registers looks identical, but ESI offer an optional redefinition of bit 5.

3.2 Definition of TSM Sequence

All of the functionality of SIF's TSM control bits is also available on ESI; ESI even offers additional functionality. Bit 5 of the ESITSMx control register can be reconfigured to be used as comparator autozeroing bit by setting the ESITSM.ESICLKAZSEL bit. This allows to include a comparator offset cancellation step within the TSM sequence. Note that switching on the comparator and doing the offset cancellation can be done at the same TSM state. After this state, the comparator has to settle before the measurement can be done. The following pseudo code shows how to use the autozero feature.

```
...
ESITSM |= ESICLKAZSEL;                       // enable comparator autozero feature
...
ESITSM5 = state5_setting;                    // comparator is off in this state
ESITSM6 = ESICA + ESICAAZ + state6_setting;  // comparator is switched on and
                                             // autozero is started
ESITSM7 = ESICA + state7_setting;            // autozero is completed, now
                                             // comparator has to settle
ESITSM8 = ESICA + ESIRSON + state8_setting;  // now the measurement result can
                                             // be latched (ESISRON=1)
ESITSM9 = state9_setting;                    // comparator is off in this state
...
```

In above example, the appropriate timing for each individual ESITSMx state must be considered (see the device-specific data sheet).

Despite the fact that the SIFTSMx and ESITSMx control bits are identical, special care should be taken regarding the ESIREPEAT bits. Because of the changed oscillator frequency and the timing for the TSM sequence, respectively, the ESIREPEAT bits have to be recalculated.

The synchronization between two ESITSMx states, when switching from ACLK to ESIOSC, may take longer than the SIF solution. Note that during synchronization the "new" ESITSMx state setting is already valid and its settings are used for AFE1 and AFE2. To avoid any timing issues (regarding to excitation time) a dummy state may be used. The following pseudo code shows an example.

```
...
ESITSM6 = ESICLK + state6_setting; // clock source = ACLK

          // state duration: ESIREPEAT+1 ACLK clock cycles
ESITSM7 =          state7_setting; // clock source = ESIOSC;
          // state duration: ESIREPEAT+1 ESIOSC clock cycles + synchronization
ESITSM8 =          state8_setting; // clock source = ESIOSC
          // state duration: ESIREPEAT+1 ESIOSC clock cycles
...
```

In the example, ESITSM6 uses ACLK. ESITSM7 then switches on ESIOSC. Because of start-up time and synchronization, the state7_setting is used for the defined ESITSM7 time plus the time needed for start-up and synchronization of ESI oscillation.

3.3 Definition of Processing State Machine (PSM) Table

The SIF module used the SIFPSMV pointer into the MSP430™ memory map as the PSM table definition. This was changed on ESI. ESI uses a dedicated memory (ESI RAM) that must be loaded after power up.

Another change was done regarding the Q7 bit usage. In the SIF module, Q7 was used for next state definition as the trigger for next state calculation, and optional as interrupt source. Within ESI Q7 is not any longer used for next state calculation. Usage as trigger source can be enabled by ESIQ7TRG. Using Q7 for interrupt generation is still available.

A major update was done on ESI regarding to its counters. ESI has three 16-bit counters, an up and down counter (ESICNT1), an up-counter (ESICNT0), and a down-counter (ESICNT2). Especially the up and down counter allows interrupt generation by two free programmable 16-bit threshold registers. The other counters use a similar interrupt generation scheme like the previous SIF module.

The reset entry was changed. The PSM on ESI features now a dedicated and well defined reset state at startup. This lead to a more reliable startup behavior. Migrating the state maps from SIF to ESI may require a remapping of the states S0, S1, S2, and S3 in case a state cluster at reset was used on SIF. ESI has eight PSM states more than SIF. With the ESI PSM, you can define all of the state machines on SIF.

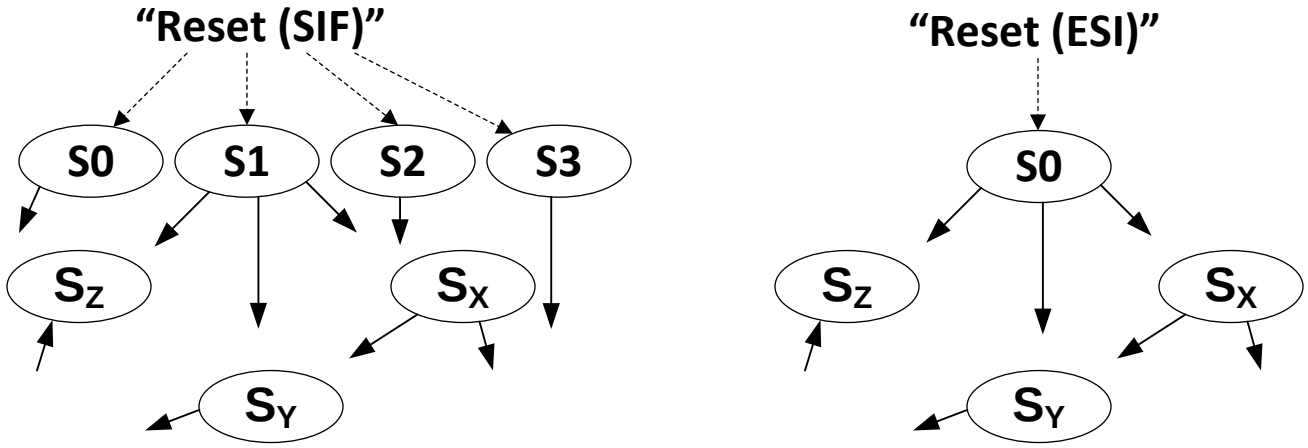

Figure 2. PSM Reset

4 References

- *MSP430FR698x(1), MSP430FR598x(1) Mixed-Signal Microcontrollers* (SLAS789)
- *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* (SLAU367)

Revision History

Changes from Original (August 2014) to A Revision **Page**

- Changed description of both interfaces for the last two rows of Table 1 2
- Added Figure 1 4
- Added the sentence that starts "With the ESI PSM, you can..." to the last paragraph of Section 3.3 8
- Added Figure 2 8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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