

# ***Effects of Clock Noise on High-Speed DAC Performance***

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## **ABSTRACT**

High speed digital-to-analog converters (DACs), synthesizer and clock distribution products are widely used in many applications, such as waveform generators, software defined radio, and modern wireless infrastructure equipment. In a typical system, a DAC device generates the sampled output using the sampling clock from the synthesizer or clock distribution chip. Therefore, the sampling clock quality is direct correlation of the sampled DAC output performance. While standards bodies or system specifications set boundaries for the DAC output performance requirement, very few research has discussed the clock performance requirement for given DAC output requirements. This application note introduces two models to illustrate clock noise transfer characteristics and the relationship between clock noise and DAC output performance. The first model describes the simple clock noise transfer characteristic and its limitation to accurately predict the influence of clock noise on DAC output performance. The second model accounts both the external sampling clock noise and the inherent DAC intrinsic noise contribution to provide more precise predictions. The two models can help designers plan proper clock noise performance under given DAC output specifications. The two examples shown at the end of this application note demonstrate the application of the model in system design.

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## 1 Definitions

$f_{\text{clock}}$ : DAC input clock frequency

$f_{\text{DAC\_output}}$ : DAC output frequency

**Clock NSD**: Noise spectrum density of DAC input clock

**DAC out NSD**: Noise spectrum density of DAC output

**DAC intrinsic noise**: DAC internal noise caused by device thermal noise, flicker noise, switch noise, and other noise.

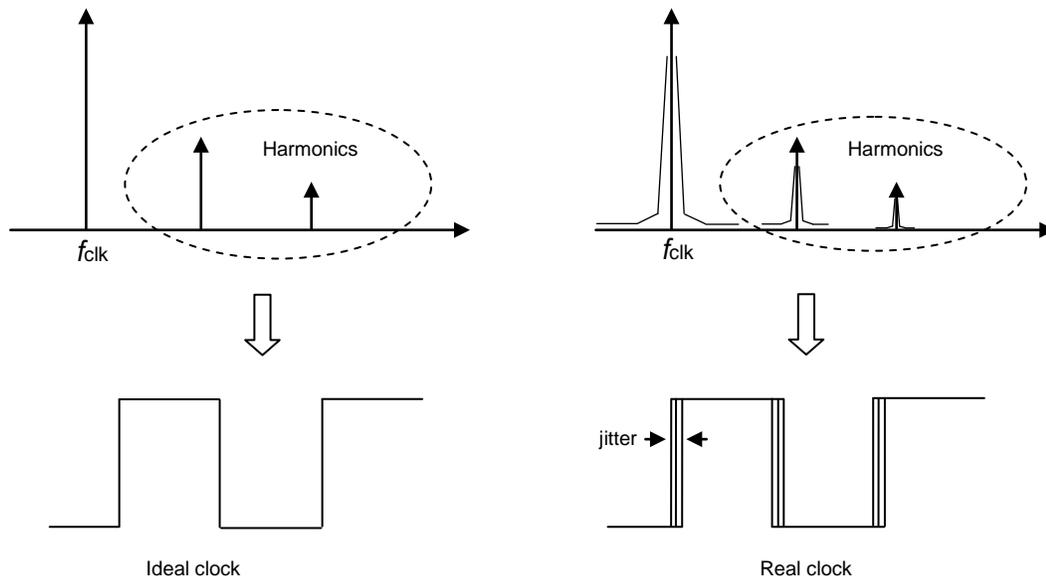
**EVM**: Evaluation module or error vector magnitude, depending on context.

**ACPR\_adj**: Adjacent channel power rejection.

**ACPR\_alt**: Alternate channel power rejection.

## 2 Introduction

DACs need a sampling clock to generate an output signal. [Figure 1](#) shows a comparison between an ideal clock and a real clock. In the frequency domain, the ideal clock has a single tone at the clock output frequency, while the real clock has phase noise around the tone. In the time domain, the ideal clock is an ideal square-wave with deterministic rising edge and falling edge, while the edges in a real clock have random jitter. In typical applications, the designers have enough specifications for the DAC output performance requirement. Meanwhile, they also need to specify the requirement for sampling clock since the DAC output quality is a direct translation from the clock quality. This section introduces the test system used to understand the relationship between clock noise and DAC output performance. Six sampling clock profiles with various jitter and phase-noise specifications are introduced for further testing.



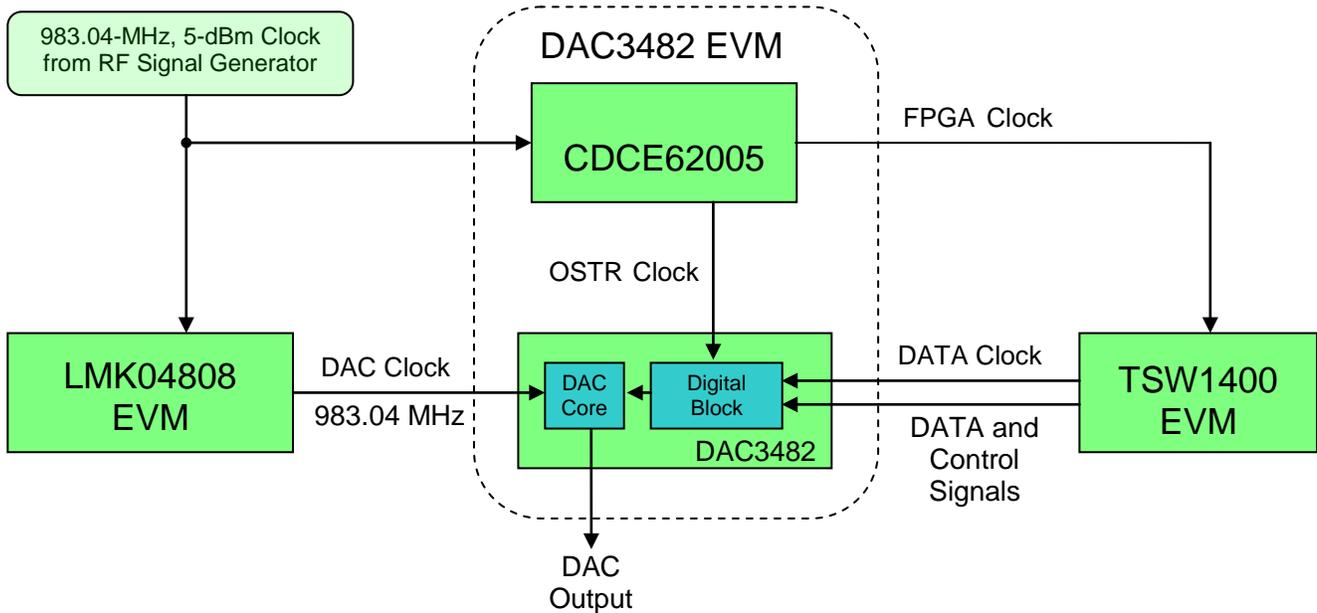
**Figure 1. Ideal Clock Versus Non-Ideal Clock**

Figure 2 shows the test system used in this application note. It consists of an RF signal generator, an LMK04808 EVM, a DAC3482 EVM and a TSW1400 EVM. The related part information is shown in Table 1.

**Table 1. Part and EVM information**

Part	Description
LMK04808	Precision Clock Conditioners Low-Noise Clock Jitter Cleaner with Dual Loop PLLs
CDCE62005	5/10 Outputs Clock Generator/Jitter Cleaner with Integrated Dual VCO
DAC3482	2-channel 16-bit 1.25 GSPS Digital-to-Analog Converter
LMK04808 EVM	Clock Jitter Cleaner With Dual Cascaded PLLs and Integrated 2.9-GHz VCO
DAC3482 EVM	DAC3482 Evaluation Module
TSW1400 EVM	High Speed Data Capture and Pattern Generation Platform

In this system, the RF signal generator provides a 983.04 MHz, 5-dBm clock to both the LMK04808 EVM and CDCE62005. The LMK04808 can clean or deteriorate the input reference to get output clocks with different jitter and phase noise. These clocks can be used as DACCLK, which is the final DAC sampling clock. The CDCE62005 divides the input clock and generates two outputs. One is OSTR clock for the DAC3482 synchronization. The other is the FPGA clock used by the TSW1400 EVM. The TSW1400 EVM can generate data clock, pattern data and other control signals for the digital blocks in DAC3482. The DATA clock is used to latch the pattern data sent from the TSW1400. In tests, changing the LMK04808 configuration can result different DAC clock phase noise and jitter, and changing the NCO configuration in the DAC3482 can result in different DAC output frequencies.



**Figure 2. EVM Setup for Test**

Figure 3 shows different DAC clocks used in single-tone, ACPR and EVM test. The jitter values for these clocks are 1 ps, 500 fs and 200 fs, separately. And the jitter integration band is from 100 Hz to 40 MHz. The *1ps\_close\_in* means the jitter value of DAC clock is 1 ps, and is dominated by close-in phase noise (about 100 Hz to 1 kHz). Clocks with such characteristics can be used in the EVM test to evaluate whether close-in phase noise influences in-band EVM. The *1ps\_peaking* means the jitter value is 1 ps, and is dominated by a peaking in the phase noise curve (about several tens of kHz). The peaking can be served as a marker for measurements, such that the clock noise transfer characteristics can be measured by tracking how this marker transfers from DAC clock input to DAC output. Clocks with such characteristics can also be used in the EVM test to find out how clocks with the same jitter but different shapes influence in-band or out-of-band EVM.

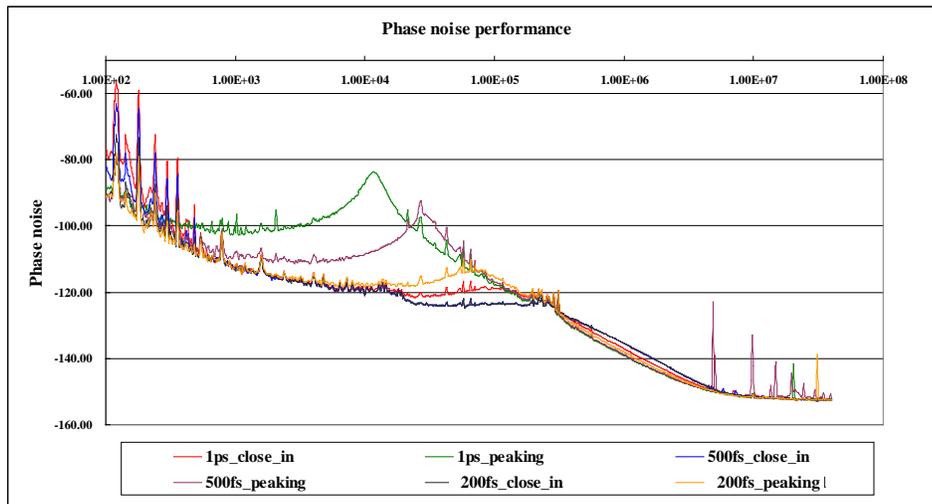


Figure 3. Different DAC Clocks Used in Test

### 3 Clock Noise Transfer Characteristics

In this section, two models are introduced to illustrate the clock noise transfer characteristic. The first model is a simple one which only takes clock noise into consideration. It shows that the clock noise is decreased by the oversampling effect of the DAC. The second model is a more accurate one because it takes both clock noise and DAC intrinsic noise into consideration, and it can make precise predictions of how clock noise transfers to the DAC output. The clocks used in this section have 1-ps, 500-fs and 200-fs jitter, separately. And the jitter is dominated by peaking in the phase noise curve. The test type is single tone test. A fixed number is generated by DAC3482, and it mixes with the divided DAC clock to form the DAC output.

#### 3.1 Simple Clock Noise Transfer Model

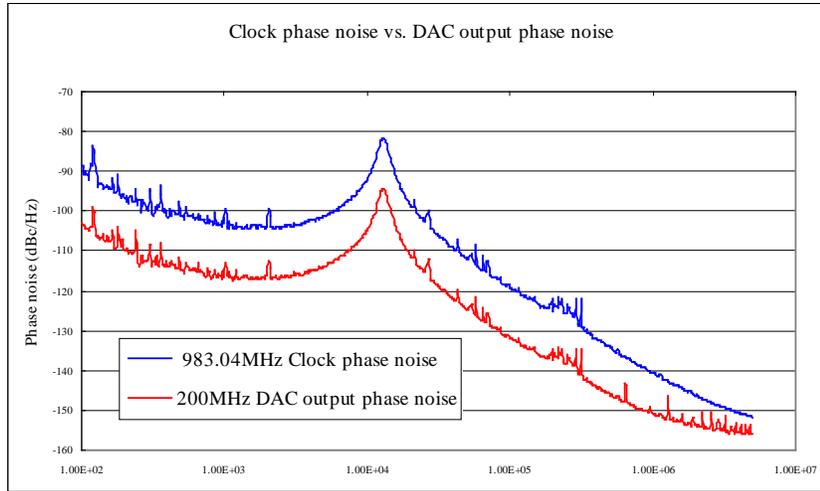
Starting with an example, Figure 4 shows the clock noise transfer characteristic. In this example, the DAC clock is 983.04 MHz and DAC output frequency is 200 MHz. The clock phase noise curve and DAC output phase noise curve have nearly the same shape, both with peaking at about 11 kHz. In terms of power, the DAC output NSD in peaking is about 14 dB lower than that in the clock phase noise curve.

Notice the equation below:

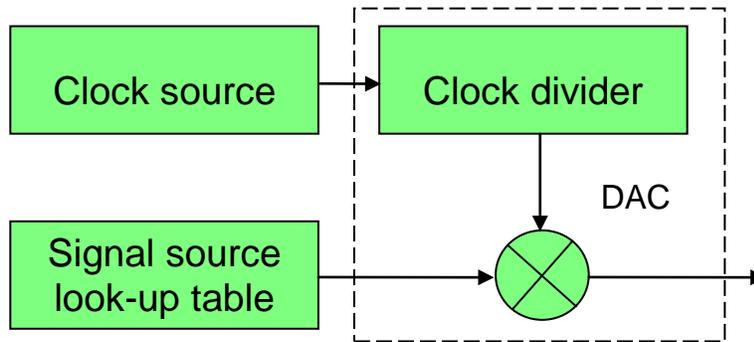
$$14 \approx 20 * \log \frac{983.04}{200} \tag{1}$$

This equation shows that for clock phase noise, the DAC acts like a divider. It divides the clock frequency and therefore lowers the clock phase noise. Figure 5 shows this simple clock noise transfer model. In this model, DAC can be seen as a clock divider plus a mixer. The clock and its noise enter the divider together, and then the divider output mixes with signal source to form the DAC output. Equation (2) illustrates how clock noise performance is improved by DAC.

$$DAC\_output\_NSD = clock\_NSD - 20 * \log \frac{f_{clock}}{f_{DAC\_output}} \tag{2}$$



**Figure 4. Phase Noise of DAC Clock and 200-MHz DAC Output**

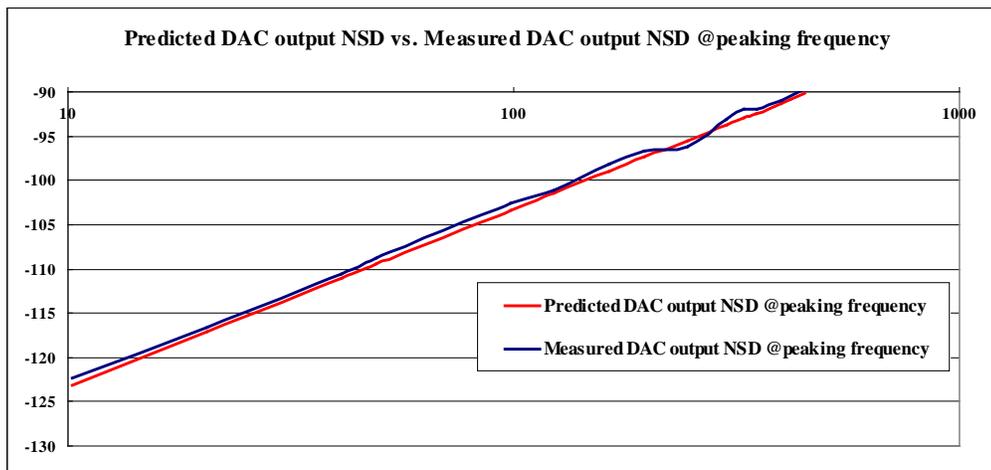


**Figure 5. Simple Clock Noise Transfer Model**

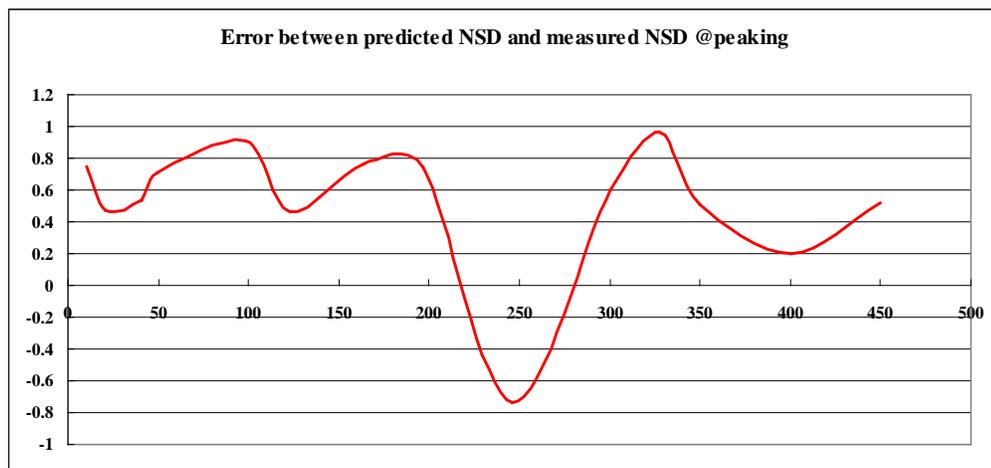
For verifying equation (2) and the model shown in Figure 5, different DAC output frequencies and their NSD at peaking frequency offset are listed in Table 2. The clock is 983.04 MHz with 1-ps jitter dominated by peaking. For DAC output, the peaking frequency in the phase noise curve is about 11 kHz for all cases. Also, the predicted DAC output NSD at the peaking frequency offset based on equation (2) is calculated. Figure 6 shows the comparison of predicted DAC output NSD and measured DAC output NSD. Figure 7 shows the error of predicted values. According to Figure 7, the error lies in about ±1 dB, which indicates that equation (2) is a good approximation to predict peaking transfer character.

**Table 2. NSD at Peaking Frequency Offset Under Different DAC Output Frequencies**

DAC Output Frequency (MHz)	Clock NSD (dBc/Hz)	Predicted DAC Output NSD (dBc/Hz)	Measured DAC Output NSD (dBc/Hz)
10.24	-83.44	-123.09	-122.34
20.48	-83.44	-117.06	-116.59
40.96	-83.44	-111.04	-110.51
49.152	-83.44	-109.46	-108.75
98.304	-83.44	-103.44	-102.53
122.88	-83.44	-101.51	-101.04
163.84	-83.44	-99.01	-98.24
196.608	-83.44	-97.42	-96.67
245.76	-83.44	-95.48	-96.22
300	-83.44	-93.75	-93.15
327.68	-83.44	-92.98	-92.02
350	-83.44	-92.41	-91.9
400	-83.44	-91.25	-91.05
450	-83.44	-90.23	-89.71

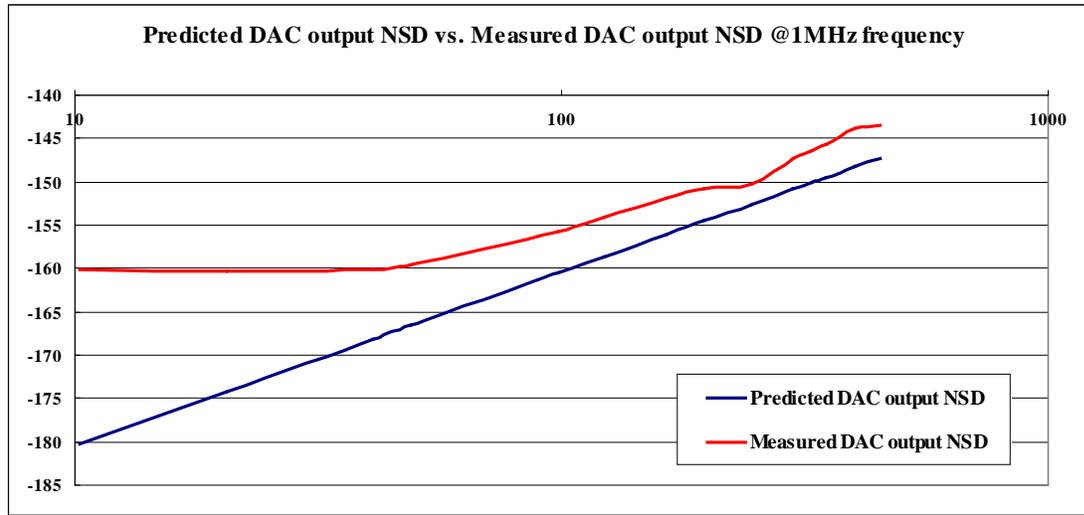


**Figure 6. Predicted DAC Output NSD Versus Measured DAC Output NSD at Peaking Offset**



**Figure 7. Error of Predicted Value at Peaking Offset**

Now that equation (2) is verified by peaking transfer characteristic, it is helpful to verify it again at large frequency offset. Figure 8 shows both predicted and measured DAC output NSD at 1-MHz frequency offset under different DAC output frequencies. The clock used here is 983.04 MHz with 1-ps jitter dominated by peaking. According to this figure, the error is unacceptably large which indicates equation (2) cannot precisely predict large frequency offset case. However, two useful clues can be found in this figure. The first clue is at low DAC output frequency, clock noise is not the main noise source for DAC, and some other noise dominates the total DAC output noise. The second clue is at high frequencies, the noise from DAC itself is still exists and influences total DAC output noise together with clock noise.



**Figure 8. Predicted DAC Output NSD Versus Measured DAC Output NSD at 1-MHz Offset**

The noise from DAC can be considered as DAC intrinsic noise. It is a combination of thermal noise, flicker noise, switch noise, and other noise sources in DAC. The influence of the DAC intrinsic noise is discussed in the next section.

### 3.2 Accurate Model that takes DAC Intrinsic Noise into Consideration

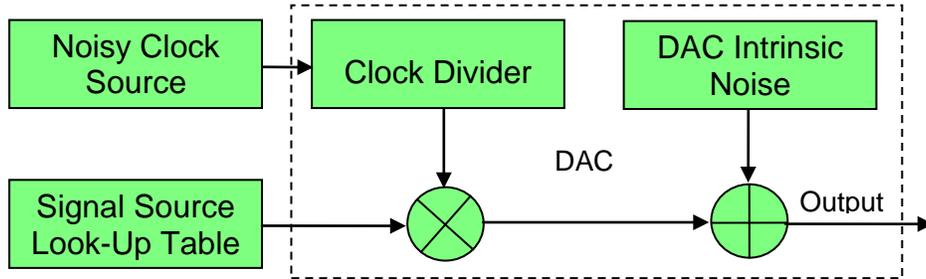
According to the previous discussion, the DAC output noise should be a combination of clock noise and DAC intrinsic noise. An assumption is introduced here that considers clock noise and DAC intrinsic noise are non-correlated, and then they influence DAC output noise separately. By this assumption, Figure 9 shows the accurate model for clock noise transfer characteristics. In this model, the transfer characteristic for clock and input signal is the same as that in the simple model, while the total DAC output noise in this model is the summation of decreased clock noise and DAC intrinsic noise. A fundamental equation can be derived from this model:

$$DAC\_output\_Noise = Clock\_Noise + DAC\_intrinsic\_noise \quad (3)$$

In an application, the noise is usually represented as NSD. So equation (3) can be written as:

$$10^{\frac{DAC\_output\_NSD}{10}} = 10^{\frac{DAC\_int\_rinsic\_noise}{10}} + 10^{\frac{clock\_noise}{10}}$$

$$clock\_noise = clock\_NSD - 20 * \log \frac{f_{clock}}{f_{DAC\_output}} \quad (4)$$



**Figure 9. Accurate Clock Noise Transfer Model**

Equation (4) can be used to precisely predict DAC output NSD when driven by a noisy clock. In an application, the DAC intrinsic noise can be arrived at by two methods. The first method is using the values in the datasheet. In the DAC3482 datasheet ([SLAS748D](#)), the NSD information is on page 16. Although NSD values from Figure 16 to Figure 20 are influenced by some clock noise, they can be used for rough estimations. The other way is measuring it at fixed-frequency offset. This method can largely eliminate clock noise influence and help designers precisely extract DAC intrinsic noise.

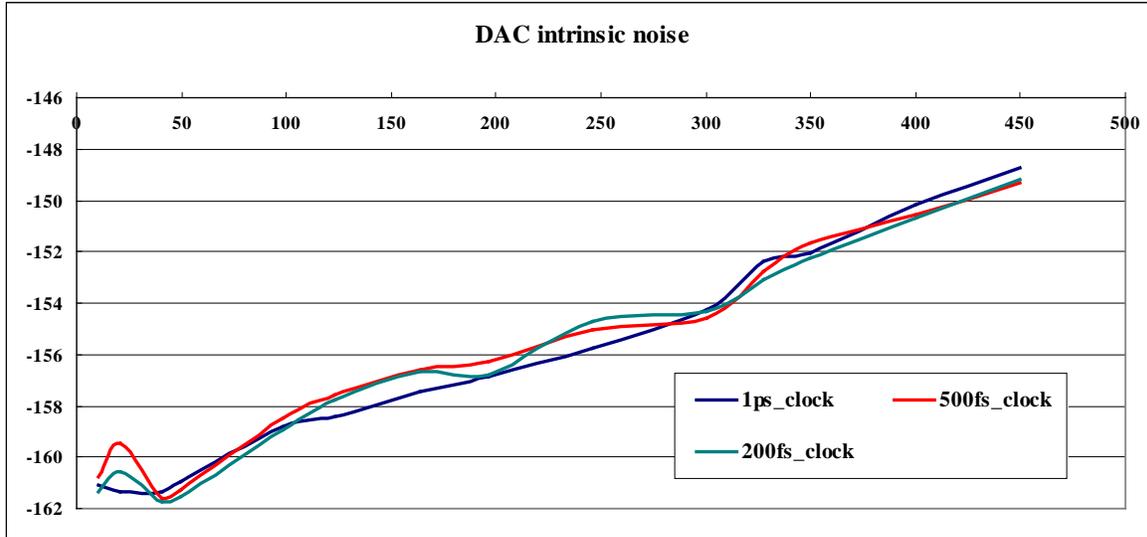
When measuring this DAC intrinsic noise, the frequency offset for NSD should be considered. There are various frequency offsets. One designer may focus on 10-MHz frequency offset NSD at 122.88-MHz IF. A different designer may focus on 1-MHz frequency offset NSD at 245.76-MHz IF. So for general purpose and for illustrating the method conveniently, it is better to select a fixed-frequency offset for all DAC output frequencies making the measurement easier. In this work, this frequency offset is 40-MHz. There must be errors in predicting DAC output NSD at peaking or 1-MHz frequency offset when using DAC intrinsic NSD at 40-MHz frequency offset. However, there is a trade-off between simplicity and accuracy and it can easily illustrate the clock noise transfer characteristic. Designers can also measure NSD at the frequency offsets that they care about. Equation (5) shows how to get this DAC intrinsic noise under known DAC output NSD and clock NSD at 40-MHz offset.

$$DAC\_int\_rinsic\_noise = 10 * \log( 10^{\frac{DAC\_output\_NSD}{10}} - 10^{\frac{clock\_noise}{10}} )$$

$$clock\_noise = clock\_NSD - 20 * \log \frac{f_{clock}}{f_{DAC\_output}} \quad (5)$$

$$NSD\_frequency\_offset = 40MHz$$

Using measured data and equation (5), [Figure 10](#) shows the derived DAC intrinsic noise curves. The clocks in this test are 983.04 MHz with 1-ps, 500-fs, and 200-fs jitter which are dominated by peaking, separately. Under the assumption that DAC intrinsic noise and DAC clock noise are non-correlated, the three curves match each other well. The variation is within ±1 dB.



**Figure 10. Getting DAC Intrinsic Noise with Measured Data and Equation (5)**

For effective evaluation in an application, it is better to get an average value based on the three curves in Figure 10. Equation (6) shows how to get this average value.

$$Avg\_DAC\_int\ rinsic\_noise = 10 * \log \frac{10^{\frac{DAC\_NSD\_1}{10}} + 10^{\frac{DAC\_NSD\_2}{10}} + 10^{\frac{DAC\_NSD\_3}{10}}}{3} \quad (6)$$

Figure 11 shows the derived average DAC intrinsic noise based on equation (6). The frequency offset of NSD in this figure is 40 MHz. With data in this curve, Figure 12 shows errors of predicted value in six cases. The *1ps\_peaking* means the input clock has 1-ps jitter, and the NSD is predicted and measured at peaking frequency offset. The *1ps\_1MHz* means input clock has 1-ps jitter, and the NSD is predicted and measured at 1-MHz offset. In this figure, the error is  $\pm 1.5$  dB, which is larger because the DAC intrinsic noise used here is measured and calculated at 40-MHz offset. However, this is a trade-off between simplicity and accuracy. Designers can use other frequency offsets that they care about to measure and calculate DAC intrinsic noise using the same method.

This completes the discussion of clock noise transfer characteristics. In an application, designers can use the simple model and equation (2) to make a fast estimation to what degree the DAC is affected by clock noise and designers can also use the more accurate model and equation (4) to make a more precise prediction. When doing this, DAC intrinsic noise can either be found from the datasheet or from measurement and equation (5).

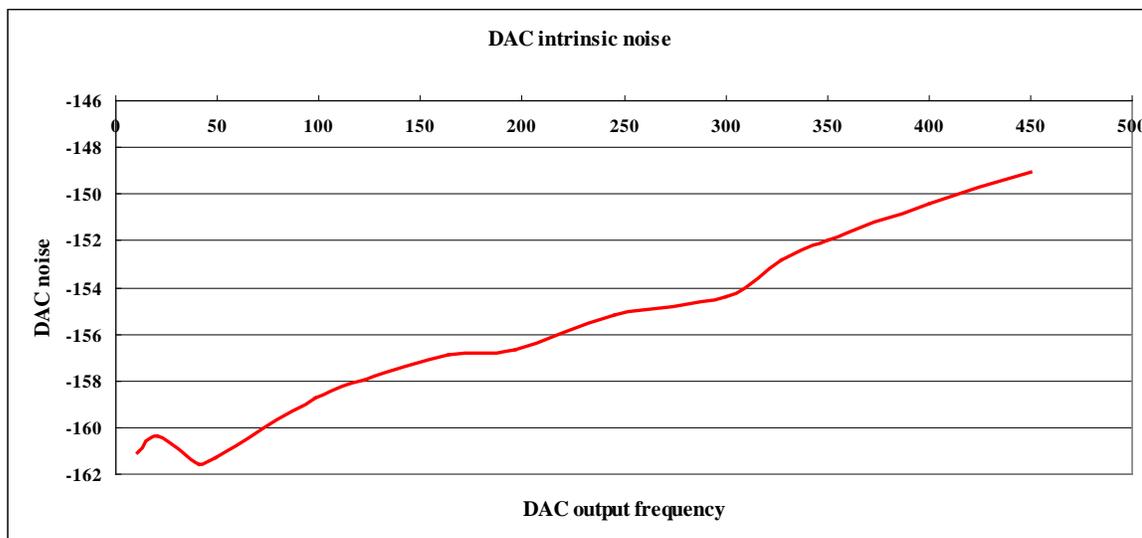


Figure 11. Average DAC Intrinsic Noise

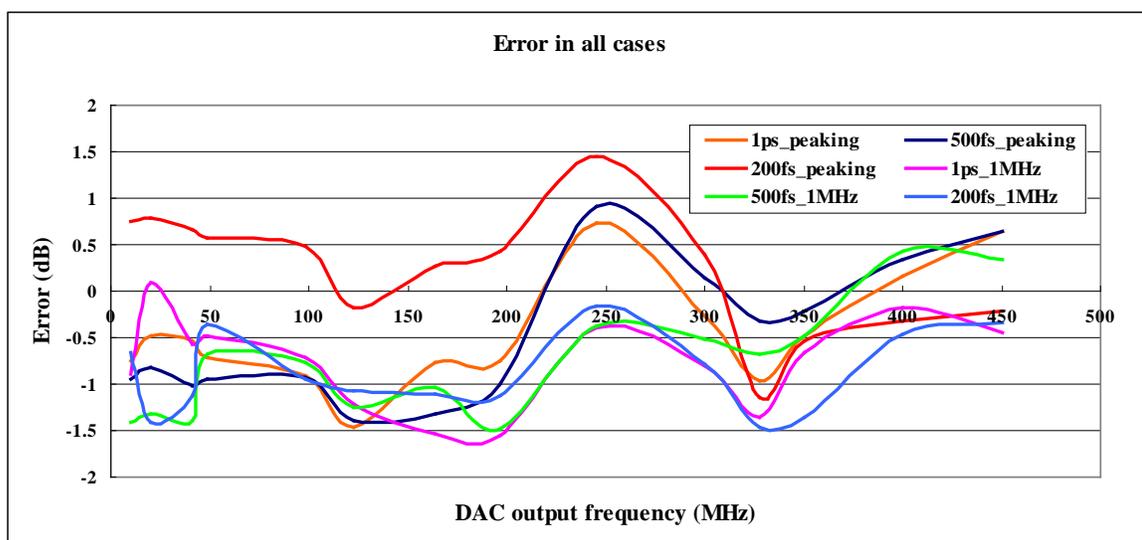


Figure 12. Error of Predicted Values when Using Average DAC Intrinsic Noise

## 4 Application Examples

This section introduces two examples to illustrate how to evaluate clock noise performance under fixed DAC specifications. The first example is when DAC in-band EVM specification is set, how to determine the required clock noise performance. The second example is when the DAC ACPR specification is set, how to determine the required clock noise performance. Verification is also shown for each example. The clocks used in this section are all 983.04 MHz and have 1-ps, 500-fs, and 200-fs jitter values, separately. Meanwhile, there are two corresponding clocks for each jitter, which are clock dominated by close-in phase noise and clock dominated by peaking. In test, the TSW1400 generates a single carrier WCDMA 3GPP pattern signal with 3.84 MCPS chip rate and 5-MHz channel bandwidth for the EVM and ACPR test.

#### 4.1 How to Decide Clock Noise Performance Under DAC In-Band EVM Specification

Assume there is an application that uses a 983.04-MHz clock to drive DAC. The IF is 122.88 MHz and the acceptable EVM for a WCDMA 3GPP pattern signal is 1%. In this situation, how is clock noise performance determined?

First, translate the EVM from percentage to dBc/Hz. In constellation diagram, a vector is defined as:

$$\vec{a}_K = \vec{a}_{K,signal} + \vec{e}_K \quad (7)$$

The first term is the useful signal vector, and the second term is the error vector. The EVM is defined as:

$$EVM = \left[ \frac{E \left\{ \left[ \vec{e}_k \right]^2 \right\}}{E \left\{ \left[ \vec{a}_{K,signal} \right]^2 \right\}} \right]^{1/2} \quad (8)$$

Then SNR can be derived as:

$$\begin{aligned} SNR &= 10 * \log \left[ \frac{E \left\{ \left[ \vec{a}_{K,signal} \right]^2 \right\}}{E \left\{ \left[ \vec{e}_k \right]^2 \right\}} \right] \\ &= -10 * \log( EVM^2 ) \\ &= -20 * \log( EVM ) \end{aligned} \quad (9)$$

When EVM is equal to 1%, the corresponding SNR is 40 dB. It means noise is -40 dBc compared to the useful signal. The bandwidth for the WCDMA signal is 3.84 MHz, so SNR can be translated to NSD specification:

$$\begin{aligned} NSD &= -SNR - 10 * \log( BW ) \\ &= -40 - 10 * \log( 3.84M ) \\ &= -105.84 \end{aligned} \quad (10)$$

Equation (10) means if the in-band noise is treated as white noise, then the NSD should not be larger than -105.84 dBc/Hz. For a quick estimation, using equation (2), the maximum clock NSD can be derived as:

$$\begin{aligned} clock\_NSD &= DAC\_NSD + 20 * \log \frac{983.04}{122.88} \\ &= -105.84 + 18.06 \\ &= -87.78 \end{aligned} \quad (11)$$

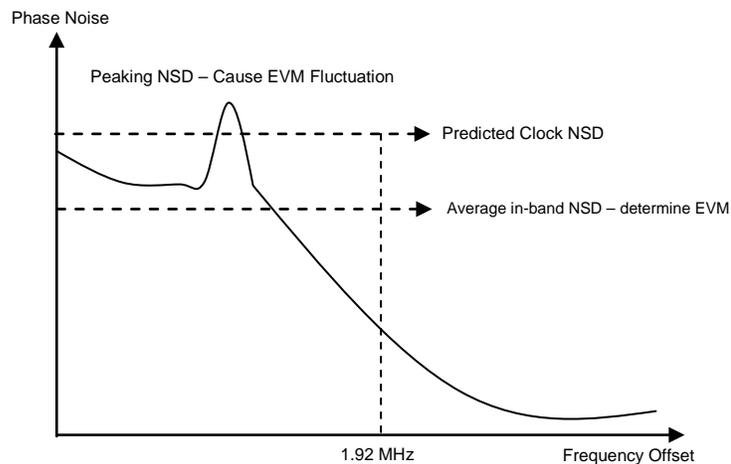
If the DAC is DAC3482, for an accurate estimation, using equation (4), the DAC intrinsic noise is  $-157.92$  dBc/Hz at 122.88 MHz, then the clock NSD can be derived as:

$$\begin{aligned}
 \text{clock\_NSD} &= 10 * \log( 10^{\frac{\text{DAC\_NSD}}{10}} - 10^{\frac{\text{DAC\_int rinsic\_noise}}{10}} ) + 20 * \log \frac{983.04}{122.88} \\
 &= -87.78
 \end{aligned}
 \tag{12}$$

The same results are derived from equation (11) and equation (12). They all mean that the maximum in-band NSD of the 983.04-MHz clock is  $-87.78$  dBc/Hz. By using the six clocks shown in Figure 3, Table 3 shows the measured DAC3482 EVM under these input clocks. In this table, there are two results which can serve as complementary to the method used in this section. The first result is that close-in noise imposes little influence on the DAC EVM, even though it has up to about  $-60$  dBc/Hz NSD in low frequency (100 Hz ~ 1 KHz). The second result is that in the 1-ps peaking dominated clock case, the peaking NSD is  $-83.44$  dBc/Hz which is larger than the predicted value,  $-87.78$  dBc/Hz. However, average NSD in this case is much smaller than  $-87.78$  dBc/Hz, so the EVM still maintains about 0.27 with some fluctuation making it change from 0.26 to 0.28. The influence of peaking NSD and average NSD is shown in Figure 13. In this figure, if the average clock NSD is lower than the predicted value, then the DAC EVM specification can be met. If there is some peaking in clock phase noise curve, then the DAC EVM may fluctuate and the fluctuation depends on the peaking power.

**Table 3. NSD at Peaking Under Different DAC Output Frequencies**

Clock jitter (ps)	Jitter type	Peaking NSD (dBc/Hz)	Measured EVM %
0.2	Close-in dominated	~ $-60$	0.23
0.2	Peaking dominated	$-108.63$	0.23
0.5	Close-in dominated	~ $-60$	0.24
0.5	Peaking dominated	$-95.78$	0.24
1	Close-in dominated	~ $-60$	0.27
1	Peaking dominated	$-83.44$	0.26~0.28



**Figure 13. Influence of Average and Peaking NSD in EVM Test**

## 4.2 How to Decide Clock Noise Performance Under ACPR Specification

Assume there is an application that uses a 983.04-MHz clock to drive the DAC. The IF is 122.88 MHz. The acceptable adjacent channel ACPR is 70 dBc and the alternate channel ACPR is 75 dBc. In this situation, how is the required clock performance determined?

First, translate the ACPR specification to NSD specification:

$$\begin{aligned}
 NSD\_Adj &= -ACPR\_Adj - 10 * \log BW \\
 &= -70 - 10 * \log(3.84M) \\
 &= -135.84
 \end{aligned} \tag{13}$$

$$\begin{aligned}
 NSD\_Alt &= -ACPR\_Alt - 10 * \log BW \\
 &= -75 - 10 * \log(3.84M) \\
 &= -140.84
 \end{aligned} \tag{14}$$

Using equation (2), the clock NSD performance is:

$$\begin{aligned}
 clock\_NSD\_5MHz &= DAC\_NSD\_Adj + 20 * \log \frac{983.04}{122.88} \\
 &= -135.84 + 18.06 \\
 &= -117.78
 \end{aligned} \tag{15}$$

$$\begin{aligned}
 clock\_NSD\_10MHz &= DAC\_NSD\_Alt + 20 * \log \frac{983.04}{122.88} \\
 &= -140.84 + 18.06 \\
 &= -122.78
 \end{aligned} \tag{16}$$

Equation (15) means the clock NSD should not be larger than  $-117.78$  dBc/Hz within the frequency offset range from 3.08 MHz to 6.92 MHz (5 MHz,  $\pm 1.92$  MHz). Equation (16) means the clock NSD should not be larger than  $-122.78$  dBc/Hz within the frequency offset range from 8.08 MHz to 11.92 MHz (10 MHz,  $\pm 1.92$  MHz).

If the DAC is DAC3482, using equation (4) for a more accurate estimation, the DAC intrinsic noise is  $-157.92$  dBc/Hz at 122.88 MHz, the clock NSD can be derived as:

$$\begin{aligned}
 clock\_NSD\_Adj &= 10 * \log \left( 10^{\frac{DAC\_NSD\_Adj}{10}} - 10^{\frac{DAC\_int\_rinsic\_noise}{10}} \right) + 20 * \log \frac{983.04}{122.88} \\
 &= -117.80
 \end{aligned} \tag{17}$$

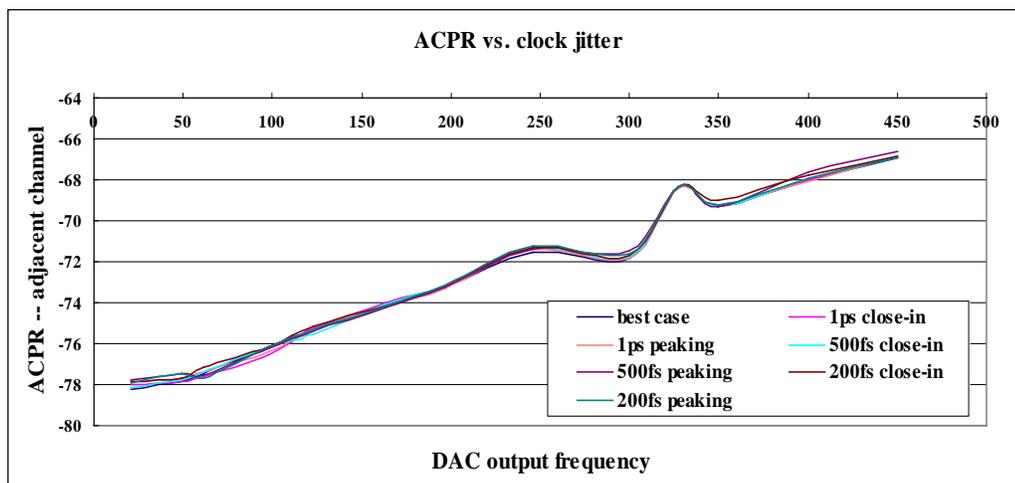
$$\begin{aligned}
 clock\_NSD\_Alt &= 10 * \log \left( 10^{\frac{DAC\_NSD\_Alt}{10}} - 10^{\frac{DAC\_int\_rinsic\_noise}{10}} \right) + 20 * \log \frac{983.04}{122.88} \\
 &= -122.86
 \end{aligned} \tag{18}$$

According to equations (15) through (18), the clock NSD at (3.08 MHz, 6.92 MHz) should not be larger than  $-118$  dBc/Hz and it should not be larger than  $-123$  dBc/Hz at the range (8.08 MHz, 11.92 MHz). By using clocks shown in Figure 3 and WCDMA 3GPP pattern signal generated by TSW1400, Table 4 shows the measured ACPR. Because the wide-band noise floor (above 1-MHz frequency offset) is lower than about  $-140$  dBc/Hz, the measured ACPR can meet the specification perfectly and in this case, the main factor that limits ACPR is DAC itself rather than clock.

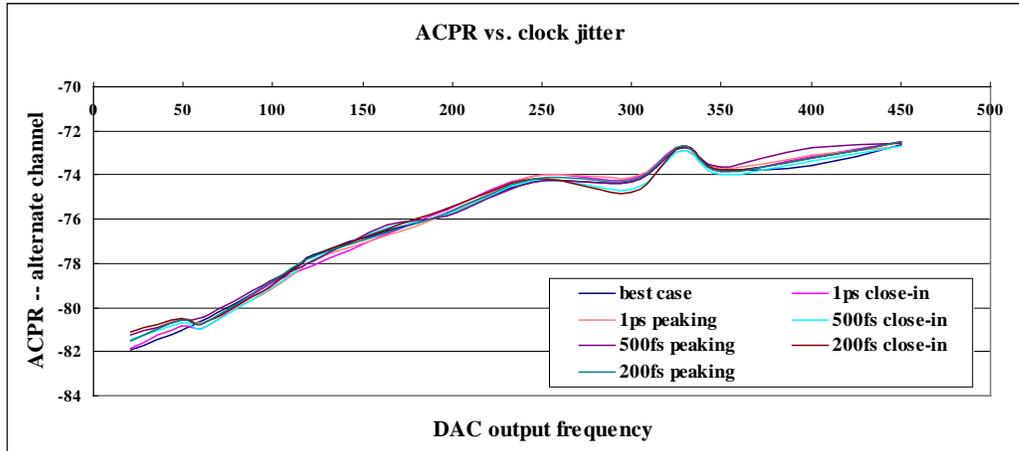
**Table 4. ACPR Results at 122.88-MHz DAC Output**

Clock Jitter (ps)	Jitter Type	Adjacent Channel ACPR (dBc)	Alternate Channel ACPR (dBc)
0.2	Close-in dominated	75.18	77.69
0.2	Peaking dominated	75.29	77.66
0.5	Close-in dominated	75.50	77.82
0.5	Peaking dominated	75.40	77.88
1	Close-in dominated	75.29	77.86
1	Peaking dominated	75.26	78.06

Now that the clock noise floor is so low that it nearly reaches  $-150$  dBc/Hz when the frequency offset is larger than several MHz, an assumption can be introduced that the DAC ACPR is not influenced by such low clock noise. Figure 14 and Figure 15 confirm this assumption. Figure 14 shows when clock frequency is 983.04 MHz with 150-fs, 200-fs, 500-fs, and 1-ps jitter values, adjacent channel ACPR remains nearly the same under different clock jitter and phase noise shapes. The *best case* in Figure 14 means the clock used in the test has the best phase noise performance and the total jitter from 100 Hz to 40 MHz is only 150 fs. The *1ps close-in* means the clock has 1-ps jitter, and this jitter is dominated by close-in phase noise. The *1ps peaking* means the clock has 1-ps jitter and this jitter is dominated by peaking in phase noise curve. Figure 15 shows the alternate channel case. It is also obvious that clock noise has little influence on the alternate channel ACPR.



**Figure 14. Adjacent Channel ACPR Measured Under 7 Clocks**



**Figure 15. Alternate Channel ACPR Measured Under 7 Clocks**

## 5 Conclusion

This application note discusses how clock noise influences DAC performance. Two models and equations are introduced for evaluation and prediction. Test results and analysis indicate that the DAC can be modeled as a clock divider plus a mixer. The divider can lower noise from the clock regarding as the ratio of clock frequency to DAC output frequency. Also, DAC intrinsic noise can influence the total DAC output noise. The two noise sources can be seen as non-correlated, so the DAC output noise is a simple summation of clock noise and DAC intrinsic noise. When using the two models in application, designers must translate the EVM and ACPR specification to NSD specification and use the two models and equations to make quick or accurate evaluation.

## References

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3. *DAC3482 EVM User's Guide*, Texas Instruments Inc., 2012 ([SLAU432](#))
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