Application Report
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Interfacing the ADS786x to the MSP430F2013

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ABSTRACT

This application report presents methods of interfacing the ADS7866/67/68 12/10/8-bit SAR analog-to-digital converter to the MSP430F2013 universal serial interface (USI) in SPI mode. The flexible clocking scheme of the USI port, along with the internal 16-bit shift register, provides an easy hardware/software interface to this series of high-speed, micro-power SAR converters. Project collateral discussed in this application report can be downloaded from the following URL: www.ti.com/lit/zip/SLAA308.

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Trademarks

Embedded Workbench is a trademark of IAR Systems.

1 Introduction

The ADS7866/67/68 are low-power, miniature, 12/10/8-bit A/D converters, each with a unipolar, single-ended input. These devices can operate from a single 1.6-V to 3.6-V supply with a 200-KSPS throughput for ADS7866.These devices can maintain at least a 100-KSPS throughput with a supply as low as 1.2 V, making them ideal candidates for low-power MSP430 applications requiring high-speed data acquisition.

MSP430 devices such as the new MSP430F2013, which contain a universal serial interface (USI), can be used in a simple and straightforward interface that requires no *glue logic* and little software overhead.

2 Hardware

The hardware used to produce the timing diagrams found throughout this application report includes the eZ430-F2013 Development Tool and the ADS7866/67/68 evaluation module (EVM).

2.1 ADS7866/67/68EVM

The ADS7866/67/68EVM is a member of the modular EVM series of serial ADCs available from Texas Instruments. The EVM provides a platform to demonstrate the functionality of the ADS7866, ADS7867, or ADS7868 ADC with various Texas Instruments DSPs and microcontrollers, while allowing easy access to all analog and digital signals for customized end-user applications. For more information on the EVM, see the user's guide SLAU181.

2.2 eZ430-F2013 Development Tool

The eZ430-F2013 is a complete MSP430 development tool including all the hardware and software necessary to evaluate the MSP430F2013. The hardware is provided in a convenient USB stick form factor. The eZ430-F2013 uses the IAR Embedded Workbench™ Integrated Development Environment (IDE) to provide full emulation with the option of designing with a stand-alone system or detaching the removable target board to integrate into an existing design. To learn more about the tool, search the Texas Instruments home page for *eZ430* .

2.3 Hardware Interface

A simple three-wire interface is the minimum requirement to connect the eZ430-F2013 and the ADS7866/67/68 EVM. Figure 1 shows the hardware connections. The chip select ($\overline{CS}$), serial data output (SDO), and serial clock (SCLK) pins from the ADC are connected to SDO, serial data in (SDI) , and SCLK pins, respectively, of the USI port.

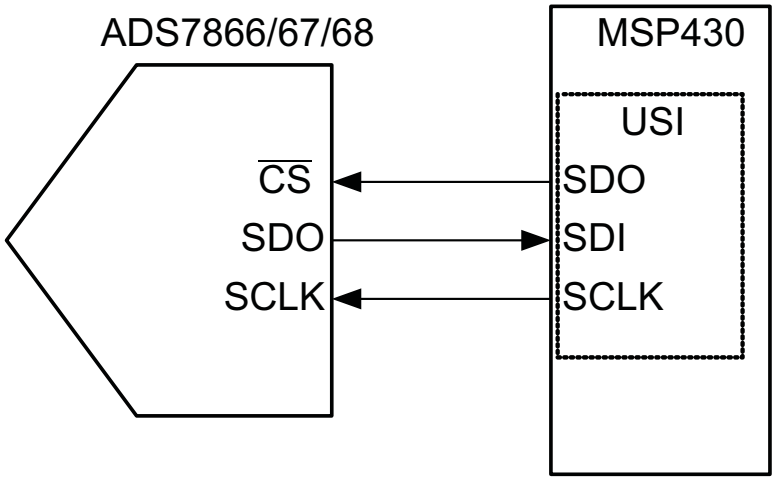

Figure 1. Hardware Interface Block Diagram

Table 1. Cable Requirements

ADS7866/67/68EVM	eZ430-F2013
J2.1 – Chip Select	P1.6 - SDO (GPIO is alternate choice)
J2.3 – CLOCK	P1.5 - SCLK
J2.13 – Data Out	P1.7 - SDI

3 Software Interface

The software was written and compiled using the Kickstart version of Embedded Workbench™ for the MSP430 from IAR. This software is the free version of the IDE and is available for download from the TI Web site, http://www.ti.com. The code used in these examples is available on request.

3.1 USI Settings

USI Control registers 0 and 1 (USICTL0 and USICTL1) set up the basic operation of the serial interface. The port is configured in SPI master mode by setting bits 3, 5, 6, and 7 in USICTL0. The USI Counter Interrupt is set in USICTL1 to provide an efficient means of SPI communication with minimal software overhead.

The serial clock polarity, source, and speed are controlled by settings in the USI Clock Control register (USICKCTL). For the purposes of this document, the polarity of the clock is set to one (dwells high) and the clock source was the SMCLK with a division factor of one.

Bit clocking and shift register configuration is controlled in the USI port by the bit settings in the USI Bit Count register (USICNT). By setting the USICNT to 0x11, 17 serial clocks are transmitted from the MSP430 to the ADS7866/67/68 on each conversion cycle. Setting the USI16B bit in the USICNT register causes the shift register to act as a 16-bit transmit/receive buffer. Transmitted data is MSB aligned and commences with the first SCLK cycle.

3.2 Starting a Conversion

Connecting the SDO output of the USI port to the $\overline{CS}$ input on the ADS7866/67/68EVM starts a conversion cycle with timing fixed to the USI port transmitter. This ensures adequate setup time for the ADC to resume operation from its auto power-down state and provides three SCLK periods of sample time. The conversion results are presented on the serial data output pins of the ADC at the start of the sixth SCLK cycle.

The $\overline{CS}$ pin also can be controlled by GPIO. In this case, care must be taken to ensure proper setup and hold times are met. Using GPIO to control the start of conversion allows the user to implement a 16 SCLK transfer by setting USICNT to 0x10. This would be useful in situations where additional slave SPI devices, such as a DAC, are used in the system.

The ADC begins to output the conversion results (MSB first) on the fifth SCLK cycle after the $\overline{CS}$ pin toggles. Because the shift register holds the last 16 bits of received data, the entire conversion result is captured (LSB aligned) for further processing. Figure 2 shows the entire process of this timing diagram.

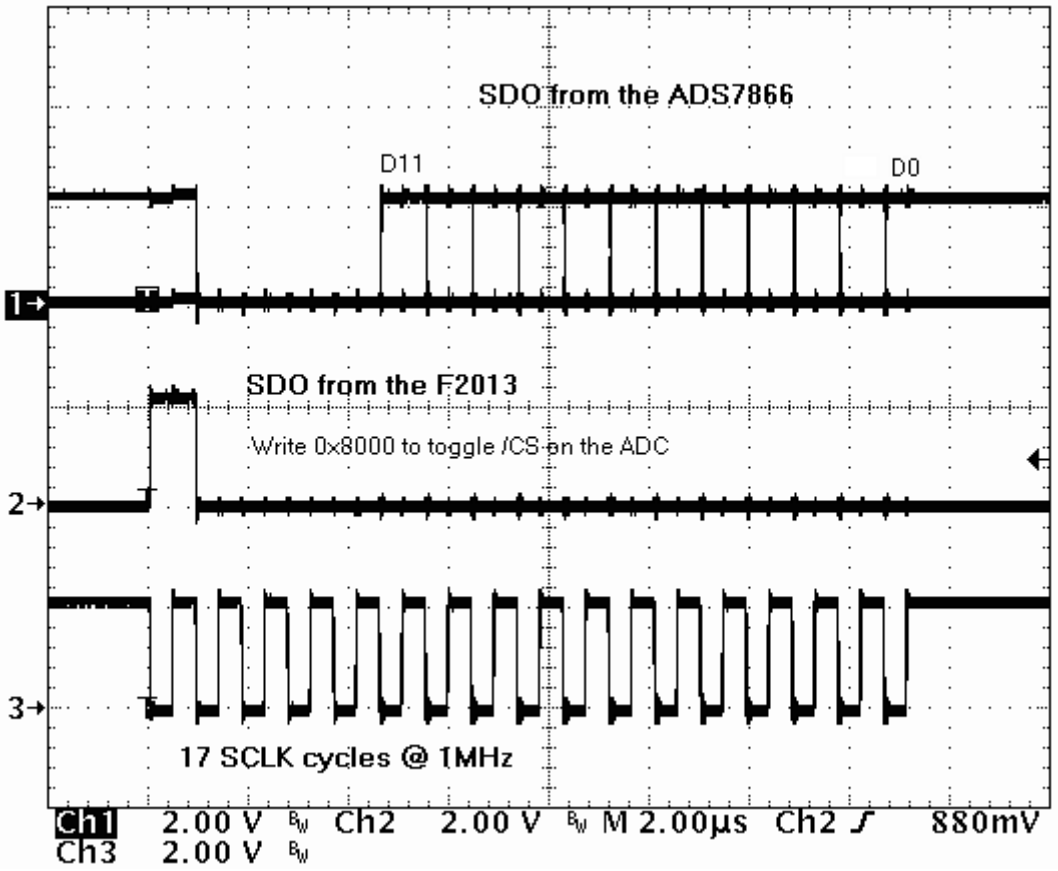

Figure 2. Complete Conversion Cycle – Single Channel

4 Power and Performance

The combining of low-power and high-performance ADS7866, ADS7867, and ADS7868 with the USI port of MSP430 processors is a relatively simple and straightforward task. System performance characteristics of 71-dB SNR, –83-dB THD, and ±1.5-LSB linearity are possible using as little power as 743 µW.

For this application report, the MSP430F2013 target board from the eZ430-F2013 Development Kit and ADS7866 both were powered at 2.2 V. The ADC sample rate was approximately 24 KSPS. Total current drawn from the 2.2V supply was approximately 337.5 μA, the ADS7866 drew 85.5 μA.

5 Conclusion

The combining of low-power and high-performance ADS7866, ADS7867, and ADS7868 with the USI port of MSP430 processors is a relatively simple and straightforward task. In low-power or battery applications requiring high-performance data acquisition, the combination of the MSP430 and ultralow power ADCs from Texas Instruments provides a perfect combination of price and performance.

6 References

1. ADS7866/67/68 data sheet (SLAS465)
2. MSP430Fx2xx User's Guide (SLAU144)

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