Functional Safety Information

INA79X-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for INA79X-Q1 (DEK (VQFN – 15) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

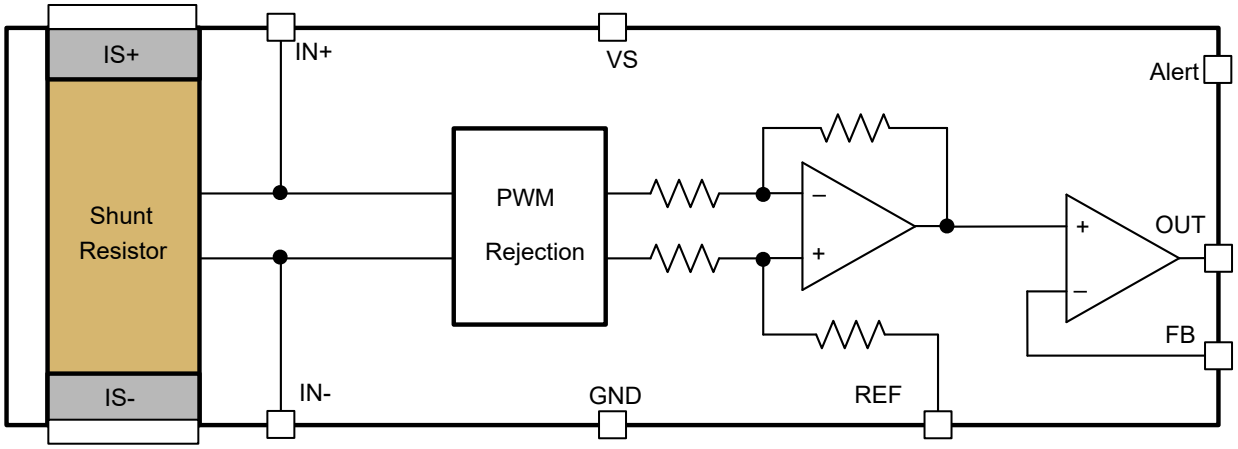

Figure 1-1. Functional Block Diagram

INA79X-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DEK (VQFN – 15) Package

This section provides functional safety failure in time (FIT) rates for the DEK (VQFN – 15) package of INA79X-Q1 (INA790A, INA790B, INA791A, and INA791B) based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	26
Die FIT rate	9
Package FIT rate	17

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 2250mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs, analog and mixed ≤ 50V Supply	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA79X-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT OPEN (Hi-Z)	5
VOUT stuck (high or low)	30
VOUT is functional, not in specification	35
Alert (false trip or failure to trip)	30

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the INA79X-Q1 (DEK (VQFN – 15) package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = –40°C to +125°C
- V_S = 5.0V
- V_{CM} = $V_{IN–}$ = 48V

4.1 DEK (VQFN – 15) Package

Figure 4-1 shows the INA79X-Q1 pin diagrams for the DEK (VQFN – 15) package. For a detailed description of the device pins please refer to the corresponding *Pin Configuration and Functions* sections in the INA790x and INA791x datasheets.

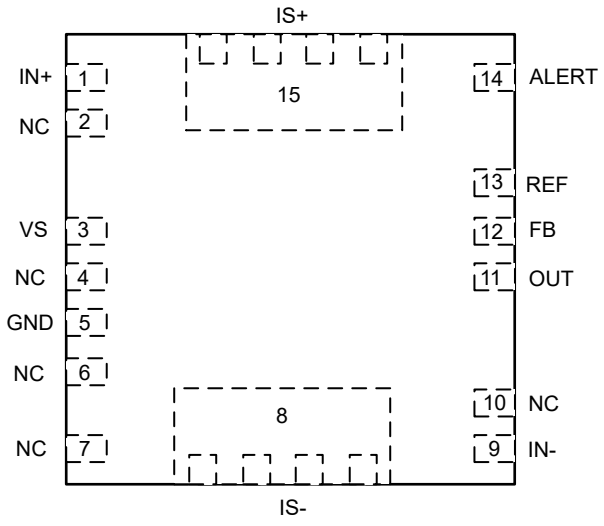

Figure 4-1. Pin Diagram DEK (VQFN – 15) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	A short from the bus supply to GND occurs. High current flows from the bus supply to GND. Damage to the internal bond wires is possible.	A
NC	2	The device operates as normal.	D
VS	3	The power supply is shorted to GND. There is no power to the device.	B
NC	4	The device operates as normal.	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	5	The device operates as normal.	D
NC	6	The device operates as normal.	D
NC	7	The device operates as normal.	D
IS–	8	In a high-side configuration, a short from the bus supply to GND occurs. High current flows from the bus supply to GND. The shunt is potentially damaged due to high current.	A
		In a low-side configuration, normal operation.	D
IN–	9	In a high-side configuration, a short from the bus supply to GND occurs. High current flows from the bus supply to GND. Damage to the internal bond wires is possible.	A
		In a low-side configuration, normal operation.	D
NC	10	The device operates as normal.	D
OUT	11	The output is shorted to GND.	B
FB	12	The output voltage becomes unpredictable.	B
REF	13	The device operates as normal if REF = GND by design.	D
		If REF ≠ GND by design, the functionality of the device is affected.	B
ALERT	14	The ALERT pin is forced to active mode. There is a loss of the functionality of the ALERT pin.	B
IS+	15	A short from the bus supply to GND occurs in a high-side configuration. The functionality of the system is affected in a high-side or low-side configuration.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	The device operates as normal.	D
NC	2	The device operates as normal.	D
VS	3	There is no power to the device.	B
NC	4	The device operates as normal.	D
GND	5	There is no power to the device.	B
NC	6	The device operates as normal.	D
NC	7	The device operates as normal.	D
IS–	8	The bus supply to the load path is cut off and load current does not flow.	C
IN–	9	The device operates as normal.	D
NC	10	The device operates as normal.	D
OUT	11	The output can be left open.	C
FB	12	The output becomes unpredictable	B
REF	13	The output becomes unpredictable	B
ALERT	14	The ALERT pin is open. There is a loss of the functionality of the ALERT pin.	B
IS+	15	The bus supply to the load path is cut off and load current does not flow.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN+	1	2 – NC	The device operates as normal.	D
NC	2	3 – VS	The device operates as normal.	D
VS	3	4 – NC	The device operates as normal.	D
NC	4	5 – GND	The device operates as normal.	D
GND	5	6 – NC	The device operates as normal.	D
NC	6	7 – NC	The device operates as normal.	D
NC	7	8 – IS–	The device operates as normal.	D
IS–	8	9 – IN–	The device operates as normal.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN–	9	10 – NC	The device operates as normal.	D
NC	10	11 – OUT	The device operates as normal.	D
OUT	11	12 – FB	The device operates as normal if the OUT pin is shorted to the FB pin by design	D
			If the OUT pin is not shorted to the FB pin by design, the functionality of the device is affected.	C
FB	12	13 – REF	The functionality of the output is affected.	C
REF	13	14 – ALERT	The functionalities of both the output and ALERT pins are affected.	B
ALERT	14	15 – IS+	In a high-side configuration, damage to the device is possible.	A
			In a low-side configuration, there is a loss of the functionality of the ALERT pin.	B
IS+	15	1 – IN+	The device operates as normal.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	In a low-side configuration, a short from the pin VS to GND occurs. In a high-side configuration, the bus supply is shorted to the VS pin. Damage to the device is possible.	A
NC	2	The device operates as normal.	D
VS	3	The device operates as normal.	D
NC	4	The device operates as normal.	D
GND	5	The power supply is shorted to GND. There is no power to the device.	B
NC	6	There is a slight increase in quiescent current. The device functionality not affected.	C
NC	7	The device operates as normal.	D
IS–	8	In a high-side configuration, a short from the bus supply to the VS pin occurs. High current flows from the bus supply to the VS pin or from the VS pin to the bus supply. Damage to the device is possible.	A
		In a low-side configuration, the functionality of the system is affected negatively but the device is not negatively affected.	C
IN–	9	In a high-side configuration, a short from the bus supply to the VS pin occurs. High current flows from the bus supply to the VS pin or from the VS pin to the bus supply. Damage to the device is possible.	A
		In a low-side configuration, the functionality of the system is affected negatively but the device is not negatively affected.	C
NC	10	The device operates as normal.	D
OUT	11	The output is shorted to the power supply.	B
FB	12	The output becomes unpredictable.	B
REF	13	The device operates as normal if REF = VS by design.	D
		If REF ≠ VS by design, the functionality of the device is affected.	B
ALERT	14	There is a loss of the functionality of the ALERT pin.	B
IS+	15	In a low-side configuration, a short from the VS pin to GND occurs. In a high-side configuration, the bus supply is shorted to the VS pin. Damage to the device is possible.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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