Functional Safety Information

TPS7B4256-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS7B4256-Q1 (D and DDA packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

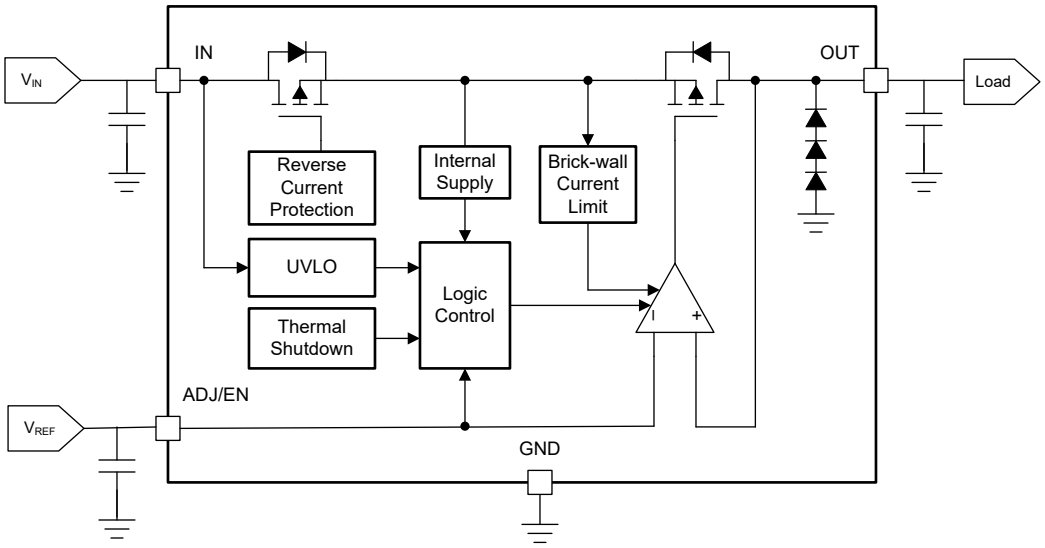

Figure 1-1. Functional Block Diagram

The TPS7B4256-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 D Package

This section provides functional safety failure in time (FIT) rates for the D package of the TPS7B4256-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	4
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 150mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator ≤ 1 Watt – (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DDA Package

This section provides functional safety failure in time (FIT) rates for the DDA package of the TPS7B4256-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	12
Die FIT rate	3
Package FIT rate	9

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 150mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator ≤ 1 Watt – (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B4256-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output (output low)	45
Output high (following input)	45
Short any two adjacent pins	5
Output not in specification	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B4256-Q1 (D and DDA packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device operates at free-air temperatures between -40°C and 150°C.
- The ADJ/EN pin is driven from an external source.
- The device operates at an input voltage of at least 3V and no more than 40V.
- The device operates according to all recommended operating conditions, and the absolute maximum ratings in the device-specific data sheet are not exceeded.
- The NC pins are floating.

4.1 D Package

Figure 4-1 shows the TPS7B4256-Q1 pin diagram for the D package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B4256-Q1 data sheet.

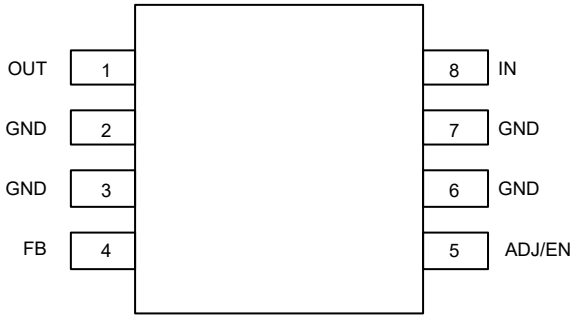

Figure 4-1. Pin Diagram (D) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
GND	2	No effect. Normal operation.	D
GND	3	No effect. Normal operation.	D
FB	4	If FB is directly connected to OUT, regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown. If FB is connected by a resistor divider, V_{OUT} tracks V_{IN} minus the dropout voltage.	B
ADJ/EN	5	The device is disabled, resulting in no output voltage.	B
GND	6	No effect. Normal operation.	D
GND	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
GND	2	No effect. Normal operation.	D
GND	3	No effect. Normal operation.	D
FB	4	The error amplifier input is not connected. Output voltage is indeterminate.	B
ADJ/EN	5	The device state is unknown. If the device is on, the output voltage is indeterminate.	B
GND	6	Ground loop parasitics are increased and transient performance can be degraded.	C
GND	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	GND	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
GND	2	GND	No effect. Normal operation.	D
GND	3	FB	If FB is directly connected to OUT, regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown. If FB is connected by a resistor divider, V_{OUT} tracks V_{IN} minus the dropout voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ADJ/EN	5	GND	The device is disabled, resulting in no output voltage.	B
GND	6	GND	No effect. Normal operation.	D
GND	7	IN	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible. $V_{OUT} = V_{IN}$.	B
NC	2	No effect. Normal operation.	D
GND	3	Power is not supplied to the device. System performance depends on upstream current limiting.	B
FB	4	Device channel is closed. If FB is tied to OUT, then $V_{OUT} = V_{IN}$. If FB is connected with a resistor divider, V_{OUT} equals V_{IN} if there is no loading on the device. If the loading on the device exceeds the leakage through the top feedback resistor, V_{OUT} is pulled to 0V.	B
ADJ/EN	5	V_{OUT} tracks V_{IN} minus the dropout voltage.	B
GND	6	Power is not supplied to the device. System performance depends on upstream current limiting.	B
NC	7	No effect. Normal operation.	D
IN	8	No effect. Normal operation.	D

4.2 DDA Package

Figure 4-2 shows the TPS7B4256-Q1 pin diagram for the DDA package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B4256-Q1 data sheet.

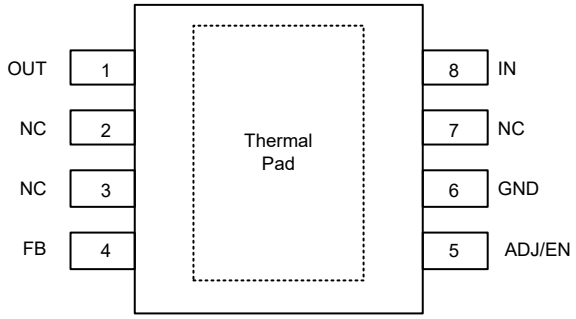

Figure 4-2. Pin Diagram (DDA Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
FB	4	If FB is directly connected to OUT, regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown. If FB is connected by a resistor divider, V_{OUT} tracks V_{IN} minus the dropout voltage.	B
ADJ/EN	5	The device is disabled, resulting in no output voltage.	B
GND	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
FB	4	The error amplifier input is not connected. Output voltage is indeterminate.	B
ADJ/EN	5	The device state is unknown. If the device is on, the output voltage is indeterminate.	B
GND	6	Ground loop parasitics are increased and transient performance can be degraded.	C
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC	No effect. Normal operation.	D
NC	2	NC	No effect. Normal operation.	D
NC	3	FB	No effect. Normal operation.	D
ADJ/EN	5	GND	The device is disabled, resulting in no output voltage.	B
GND	6	NC	No effect. Normal operation.	D
NC	7	IN	No effect. Normal operation.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible. $V_{OUT} = V_{IN}$.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
FB	4	Device channel is closed. If FB is tied to OUT, then $V_{OUT} = V_{IN}$. If FB is connected with a resistor divider, V_{OUT} equals V_{IN} if there is no loading on the device. If the loading on the device exceeds the leakage through the top feedback resistor, V_{OUT} is pulled to 0V.	B
ADJ/EN	5	V_{OUT} tracks V_{IN} minus the dropout voltage.	B
GND	6	Power is not supplied to the device. System performance depends on upstream current limiting.	B
NC	7	No effect. Normal operation.	D
IN	8	No effect. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

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