Functional Safety Information

TPS6289xx-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS6289xx-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

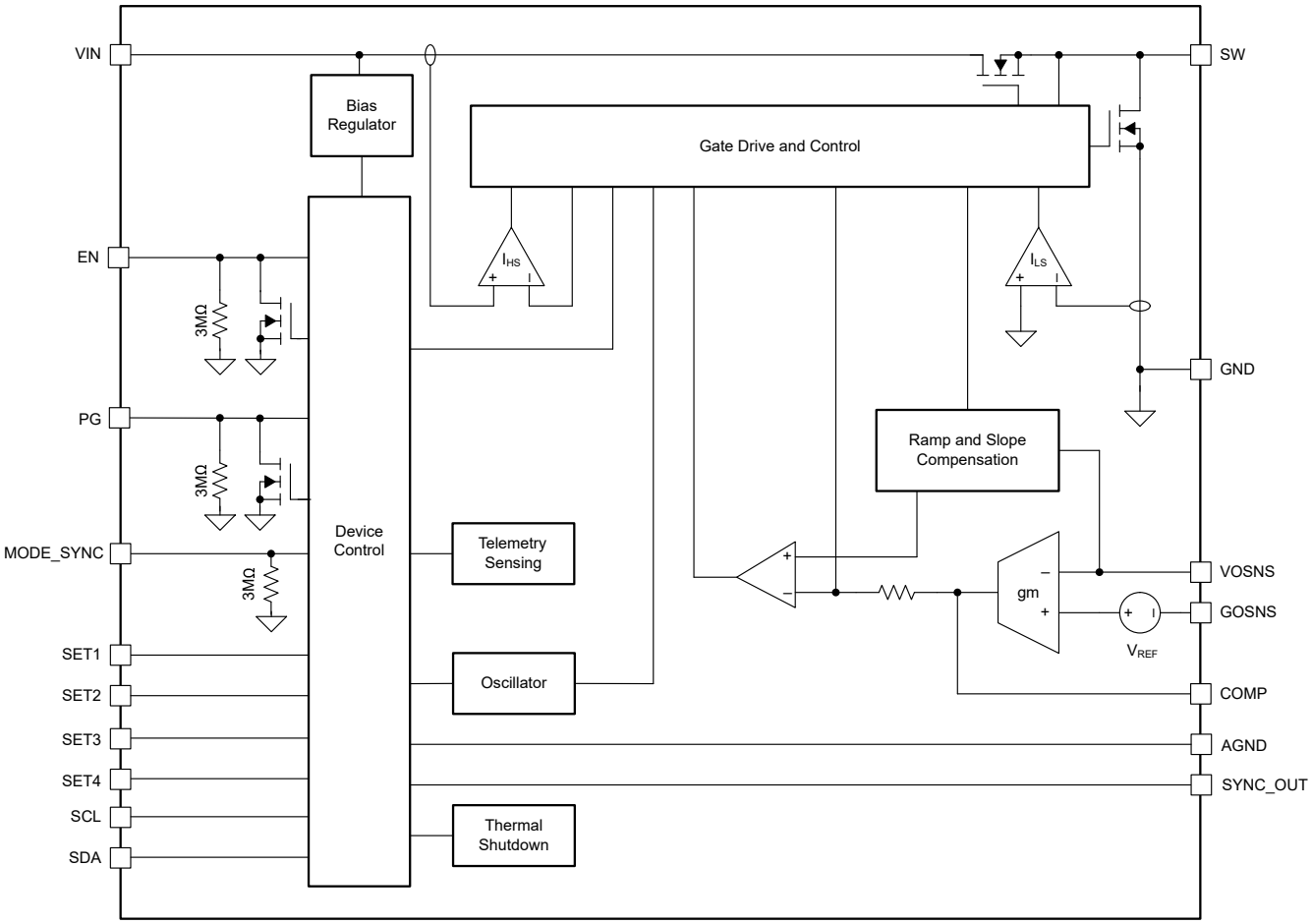

Figure 1-1. Functional Block Diagram

The TPS6289xx-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS6289xx-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	29
Die FIT rate	8
Package FIT rate	21

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor control from table 11 or figure 16
- Power dissipation: 2500mW
- Climate type: World-wide from table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS6289xx-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output not in specification – voltage or timing	25
High-side or low-side FET stuck on	45
EN, PG, or INT false trip or fails to trip	10
Switching frequency or output voltage range not in specification	10
No device communication, wrong register content	10

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS6289xx-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS6289xx-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS6289xx-Q1 data sheet.

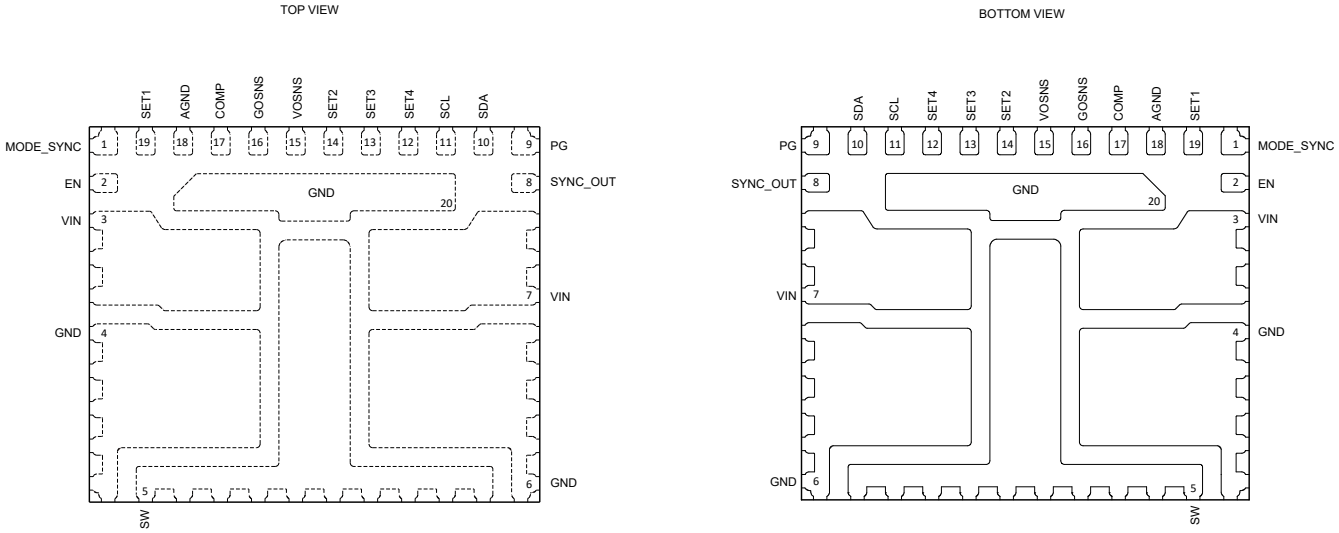

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Assumes the device is running in the typical application, please refer to the *Simplified Schematics* in the *TPS6287x-Q12.7V to 6V Input, 6-A/9-A/12-A/15-A, Automotive, Stackable, Synchronous Step-Down Converters With Fast Transient Response* data sheet.

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MODE/SYNC	1	Power-save mode is enabled. Normal operation.	C
EN	2	The device is disabled. Normal operation.	B
VIN	3	The device does not power up and there is no output voltage.	B
GND	4	Normal operation.	D
SW	5	Potential device damage.	A
GND	6	Normal operation.	D
VIN	7	The device does not power up and there is no output voltage.	B
SYNC_OUT	8	No regulated output voltage.	B
PG	9	Normal operation and loss of PG indication.	B
SDA	10	Normal operation and no I^2C communication.	B
SCL	11	Normal operation and no I^2C communication.	B
SET4	12	Normal operation. Defines I^2C address.	B
SET3	13	Normal operation. Defines output voltage range and mode of operation.	B
SET2	14	Normal operation. Defines start-up voltage, phase shift, and I^2 address.	B
VOSNS	15	Maximum duty cycle operation and no regulated output voltage. Output voltage follows the input voltage.	B
GOSNS	16	Normal operation, but output voltage accuracy declines.	C
COMP	17	The device does not power up and there is no output voltage.	B
AGND	18	Normal operation.	D
SET1	19	Normal operation. Defines start-up voltage, phase shift, and I^2 address.	D
GND	20	Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MODE/SYNC	1	Power-save mode is enabled. Normal operation.	C
EN	2	The device is disabled. Normal operation.	B
VIN	3	Normal operation. Pin 7 is still connected.	C
GND	4	Normal operation. Pin 6 and Pin 20 are still connected.	C
SW	5	No output voltage.	B
GND	6	Normal operation. Pin 4 and Pin 20 are still connected.	C
VIN	7	Normal operation. Pin 3 is still connected.	C
SYNC_OUT	8	Normal operation.	D
PG	9	Normal operation and loss of PG indication.	B
SDA	10	Normal operation and no I^2C communication.	B
SCL	11	Normal operation and no I^2C communication.	B
SET4	12	Normal operation. I^2C address is undefined.	B
SET3	13	Normal operation. Output voltage range and mode of operation are undefined.	B
SET2	14	Normal operation. Start-up voltage, phase shift, and I^2 address are undefined.	B
VOSNS	15	No output voltage regulation, which can cause the output voltage to oscillate. Oscillation frequency cannot be predicted.	B
GOSNS	16	No output voltage regulation, which can cause the output voltage to oscillate. Oscillation frequency cannot be predicted.	B
COMP	17	No loop compensation, which can cause the output voltage to oscillate. Oscillation frequency cannot be predicted.	B
AGND	18	Normal operation. Pin 4, Pin 6, and Pin 20 are still connected.	C
SET1	19	Normal operation. Start-up voltage, phase shift, and I^2 address are undefined.	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	20	Normal operation. Pin 4 and Pin 6 are still connected.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
MODE/SYNC	1	2	Forced PWM operation if EN is high. Device disabled otherwise.	C
EN	2	3	Potential device damage.	A
VIN	3	4	The device does not power up and there is no output voltage.	B
GND	4	5	Potential device damage.	A
SW	5	6	Potential device damage.	A
GND	6	7	The device does not power up and there is no output voltage.	B
VIN	7	8	No output voltage.	B
SYNC_OUT	8	9	Potential device damage.	A
PG	9	10	Normal operation, loss of PG indication, and no I^2C communication.	B
SDA	10	11	Normal operation and no I^2C communication.	B
SCL	11	12	Normal operation. I^2C address is undefined.	B
SET4	12	13	Normal operation. I^2C address, output voltage range, and mode of operation is undefined.	B
SET3	13	14	Normal operation. Output voltage range, mode of operation and start-up voltage, phase shift, and I^2 address is undefined.	B
SET2	14	15	Output voltage regulation is undefined, maximum duty cycle operation, and no regulated output voltage. Output voltage follows the input voltage, or no output voltage.	B
VOSNS	15	16	Maximum duty cycle operation and no regulated output voltage. Output voltage follows the input voltage.	B
GOSNS	16	17	The device does not power up and there is no output voltage.	B
COMP	17	18	The device does not power up and there is no output voltage.	B
AGND	18	19	Normal operation. Defines start-up voltage, phase shift, and I^2 address.	B
SET1	19	20	Normal operation. Defines start-up voltage, phase shift, and I^2 address.	B
GND	20	1	Normal operation. Power-save mode is enabled.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MODE/SYNC	1	Forced PWM operation. Normal operation.	C
EN	2	Potential device damage.	A
VIN	3	Normal operation.	D
GND	4	The device does not power up and there is no output voltage.	B
SW	5	Potential device damage.	A
GND	6	The device does not power up and there is no output voltage.	B
VIN	7	Normal operation.	D
SYNC_OUT	8	Potential device damage.	A
PG	9	Potential device damage.	A
SDA	10	Potential device damage.	A
SCL	11	Potential device damage.	A
SET4	12	Normal operation. Defines I^2C address.	B
SET3	13	Normal operation. Defines output voltage range and mode of operation.	B

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Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SET2	14	Normal operation. Defines start-up voltage, phase shift, and I^2 address.	B
VOSNS	15	The device does not start up. Output voltage stays low.	B
GOSNS	16	Potential device damage.	A
COMP	17	Potential device damage.	A
AGND	18	The device does not power up and there is no output voltage. Potential device damage.	B
SET1	19	Normal operation. Defines start-up voltage, phase shift, and I^2 address.	B
GND	20	The device does not power up and there is no output voltage.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

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