Functional Safety Information

LM644xx-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LM644xx-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

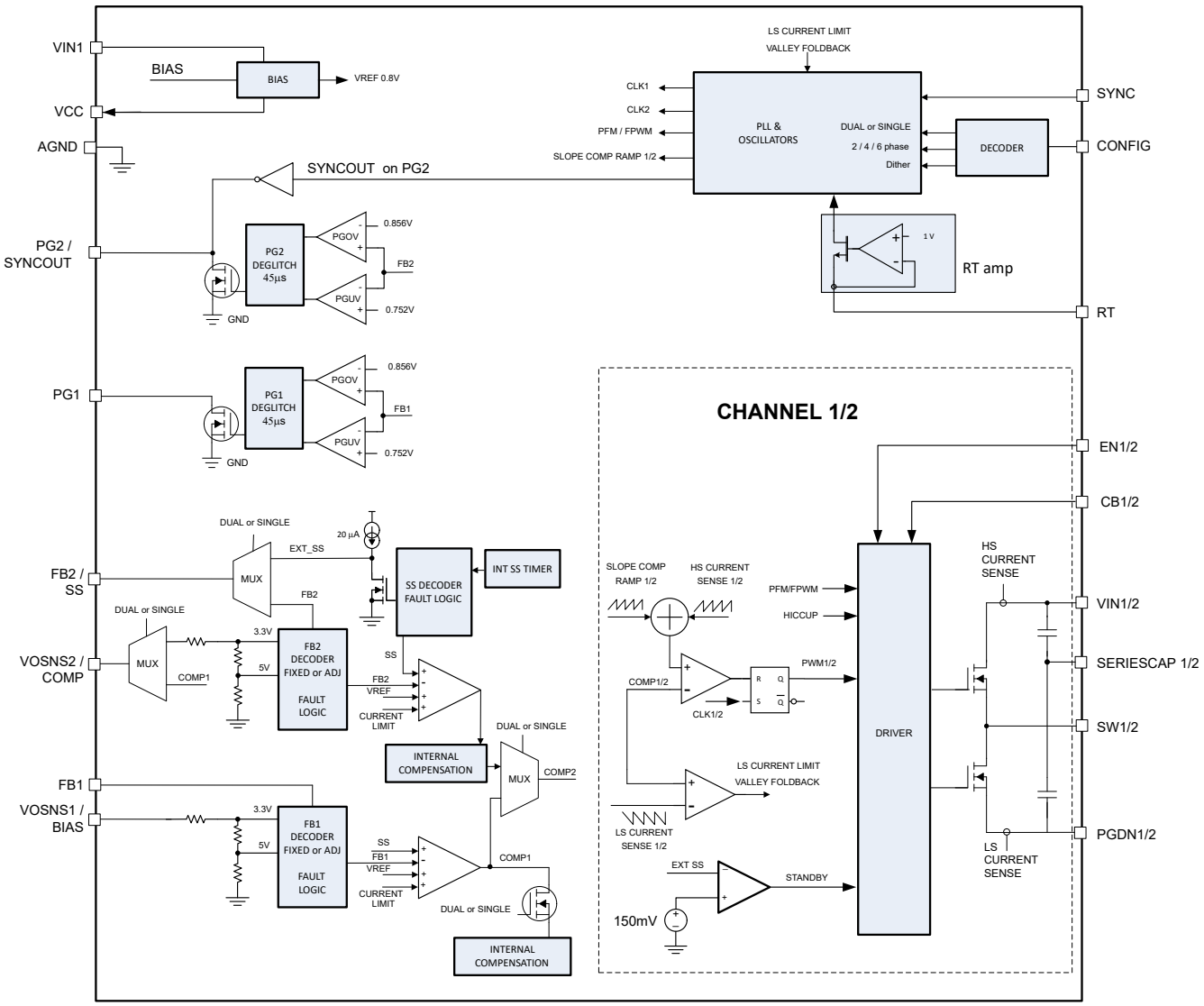

Figure 1-1. Functional Block Diagram

LM644xx-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LM644xx-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	17
Die FIT rate	4
Package FIT rate	13

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1250mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs analog and mixed = < 50V supply	25	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM644xx-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	50
SW output not in specification - voltage or timing	40
SW power FET stuck on	5
PGOOD false trip, fails to trip	5

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM644xx-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1, Figure 4-2, and Figure 4-3 show the LM644xx-Q1 pin diagrams. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM644xx-Q1 data sheet.

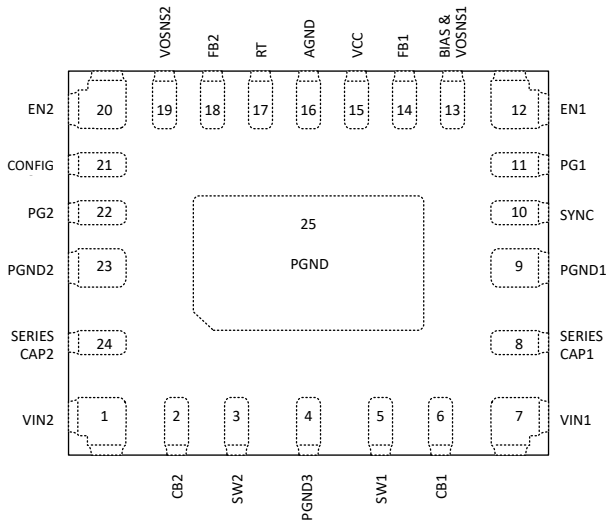

Figure 4-1. Dual Pin Diagram

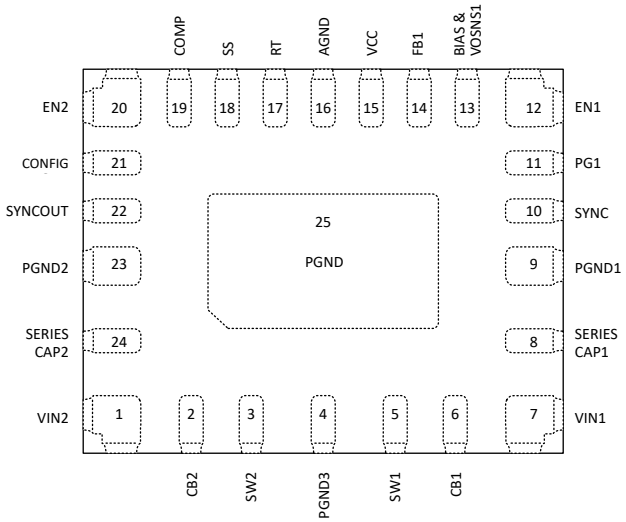

Figure 4-2. Single Primary Pin Diagram

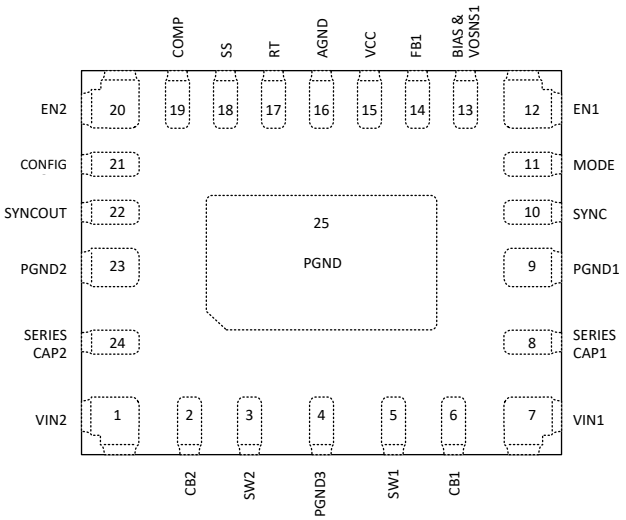

Figure 4-3. Single Secondary Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, per the LM644A2-Q1 data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
VIN2	1	VOUT = 0V.	B
CB2	2	VOUT = 0V.	B
SW2	3	Potential damage to high-side FET.	A
PGND3	4	Normal operation.	D
SW1	5	Potential damage to high-side FET.	A
CB1	6	VOUT = 0V.	B
VIN1	7	VOUT = 0V.	B
SERIES_CAP1	8	Series capacitor is shorted internally. Device bypassing capacitance increases as two-series capacitors become single capacitor.	D
PGND1	9	Normal operation.	D
SYNC	10	Normal operation for PFM mode.	C
PG1	11	Loss of power good flag.	B
MODE	11	Normal operation for PFM mode.	C
EN1	12	Device is disabled.	C
BIAS/VOSNS1	13	VOUT1 = 0V short circuit.	B
FB1	14	If configured as 3.3V fixed, normal operation. If configured for other Vout, then Vout1 is out of specification and outputs 3.3V.	B
VCC	15	Device is disabled.	B
AGND	16	Normal operation.	D
RT	17	VOUT = 0V. No switching.	B
FB2	18	If configured as 3.3V fixed, normal operation. If configured for other Vout, then Vout2 is out of specification and outputs 3.3V.	B
SS	18	VOUT = 0V.	B
VOSNS2	19	VOUT2 = 0V, if FB2 = VCC or GND.	B/C
COMP	19	VOUT = 0V.	B
EN2	20	Second channel is disabled.	B
CONFIG	21	Device is configured as dual output voltage.	B
PG2	22	Loss of power good flag.	B
SYNCOUT	22	If primary, secondary, and tertiary devices do not switch. If secondary or tertiary device does not switch. If tertiary, no effect.	B
PGND2	23	Normal operation.	D
SERIES_CAP2	24	Series capacitor is shorted internally. Device bypassing capacitance increases as two-series capacitors become single capacitor.	D
PGND	25	Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
VIN2	1	VOUT2 = 0V.	B
CB2	2	VOUT2 collapses under load as FET gate voltage is not enough to fully enhance. Damage can occur if current is pulled from switch.	A
SW2	3	VOUT2 = 0V.	B
PGND3	4	Normal operation.	D
SW1	5	VOUT1 = 0V.	B
CB1	6	VOUT1 collapses under load as FET gate voltage is not enough to fully enhance. Damage can occur if current is pulled from switch.	A
VIN1	7	VOUT1 = 0V.	B
SERIES_CAP1	8	Normal operation.	D
PGND1	9	Normal operation.	D
SYNC	10	Device can toggle between PFM and PWM modes.	C
PG1	11	Loss of power good flag.	B
MODE	11	Device can toggle between PFM and PWM modes.	C
EN1	12	Loss of disable function.	C
BIAS/VOSNS1	13	If in fixed output configuration, Vout is greater than set point. If in adjustable Vout configuration, slight increase in input current.	B
FB1	14	Part configuration is randomly selected between fixed 5V or adjustable.	B/C
VCC	15	Part can turn on and off as VCC UVLO is triggered.	B
AGND	16	Normal operation.	D
RT	17	VOUT = 0V. No switching.	B
FB2	18	Part configuration is randomly selected between fixed 5V or adjustable.	B/C
SS	18	Fast soft start.	D
VOSNS2	19	If in fixed output configuration, Vout is greater than set point.	B
COMP	19	Device can have oscillations on VOUT.	B
EN2	20	Loss of disable function.	C
CONFIG	21	VOUT = 0V. No switching.	B
PG2	22	Loss of power good flag.	B
SYNCOUT	22	If primary, secondary, and tertiary devices do not switch. If secondary or tertiary device does not switch. If tertiary, no effect.	B
PGND2	23	Normal operation.	D
SERIES_CAP2	24	Normal operation.	D
PGND	25	Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VIN2	1	CB2	Boot driver is damaged.	A
CB2	2	SW2	VOUT2 = 0.	B
SW2	3	PGND3	Potential damage to high-side FET.	A
PGND3	4	SW1	Potential damage to high-side FET.	A
SW1	5	CB1	VOUT1 = 0.	B
CB1	6	VIN1	Boot driver is damaged.	A
VIN1	7	SERIES_CAP1	Series capacitor is shorted internally. Device bypassing capacitance increases as two-series capacitors become single capacitor.	D
SERIES_CAP1	8	PGND1	Series capacitor is shorted internally. Device bypassing capacitance increases as two-series capacitors become single capacitor.	D
PGND1	9	SYNC	Normal operation for AUTO mode.	C
SYNC	10	PG1	For PG < 5.5V, device starts in PFM and transition to PWM after start up. For PG > 5.5V, damage can occur. For mode, part can enter PFWM of PWM mode based on SYNC logic.	A
PG1	11	MODE	For EN < 20V, device damage can occur if PG FET current limit is exceeded. For EN > 20V, PGOOD FET can be damaged.	A
MODE	11	EN1	For EN < 20V, normal operation. For EN > 20V, PGOOD FET can be damaged.	A
EN1	12	BIAS/VOSNS1	For EN < 5V, output voltage out of range. For EN > 5V, device damage can occur if current is not limited.	A
BIAS/VOSNS1	13	FB1	If configured as 3.3V fixed, normal operation. If configured for other Vout, then Vout1 is out of specification and outputs 3.3V.	B
FB1	14	VCC	If configured as 5V fixed, normal operation. If configured for other Vout, then Vout1 is out of specification and output 5V.	B
VCC	15	AGND	Vout1 = Vout2 = 0V.	B
AGND	16	RT	VOUT = 0V. No switching.	B
RT	17	FB2	Switching frequency and output voltage is incorrect.	B
FB2	18	SS	If FB2 is grounded, Vout2 is greater than set point. If FB2 is VCC then VCC is pulled to 5V, damage is unlikely to occur. If FB2 is resistor divider, the Vout is 3.3Vout and there is a load from the FB resistance to ground.	B
SS	18	VOSNS2	Fast soft start.	C
VOSNS2	19	COMP	VOUT2is greater than set point.	B
COMP	19	EN2	EN > 5.5V, damage of comparator if not current limited.	A
EN2	20	CONFIG	EN2 < 5.5V, device is configured as dual output voltage. EN2 > 5.5, damage if not current limited.	A
CONFIG	21	PG2	Device is configured as dual output voltage.	B
PG2	22	SYNCOUT	Loss of power good flag.	B
SYNCOUT	22	PGND2	If primary, secondary, and tertiary devices do not switch. If secondary or tertiary device does not switch. If tertiary, no effect.	B
PGND2	23	SERIES_CAP2	Normal operation.	D
SERIES_CAP2	24	PGND	Series capacitor is shorted internally. Device bypassing capacitance increases as two-series capacitors become single capacitor.	D
PGND	25	VIN2	Series capacitor is shorted internally. Device bypassing capacitance increases as two-series capacitors become single capacitor.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
VIN2	1	Normal operation.	D
CB2	2	Boot driver is damaged.	A
SW2	3	Potential damage to low-side FET.	A
PGND3	4	VOUT = 0V.	B
SW1	5	Potential damage to low-side FET.	A
CB1	6	Boot driver is damaged.	A
VIN1	7	Normal operation.	D
SERIES_CAP1	8	Series capacitor is shorted internally. Device bypassing capacitance increases as two-series capacitors become single capacitor.	D
PGND1	9	VOUT = 0V.	B
SYNC	10	Potential damage for VIN > 5.5V.	A
PG1	11	Loss of power good flag. Potential damage if not current limited.	A
MODE	11	Normal operation for PWM mode. Potential damage for VIN > 5.5V.	A
EN1	12	Device is enabled.	C
BIAS/VOSNS1	13	Potential damage from permanent short across converter.	A
FB1	14	Potential damage for VIN > 5.5V.	A
VCC	15	Potential damage for VIN > 5.5V.	A
AGND	16	VOUT = 0V.	B
RT	17	Potential damage for VIN > 5.5V.	A
FB2	18	Potential damage for VIN > 5.5V.	A
SS	18	Potential damage for VIN > 5.5V.	A
VOSNS2	19	Potential damage for VIN > 5.5V.	A
COMP	19	Potential damage for VIN > 5.5V.	A
EN2	20	Second channel is enabled.	C
CONFIG	21	Potential damage for VIN > 5.5V.	A
PG2	22	Potential damage for VIN > 20V, or lower, if not current limited.	A
SYNCOUT	22	Potential damage for VIN > 5.5V, or lower, if not current limited.	A
PGND2	23	VOUT = 0V.	B
SERIES_CAP2	24	Series capacitor is shorted internally. Device bypassing capacitance increases as two-series capacitors become single capacitor.	D
PGND	25	VOUT = 0V.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2024	*	Initial Release

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