Functional Safety Information

LM5109B-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the LM5109B-Q1 (WSON (8) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

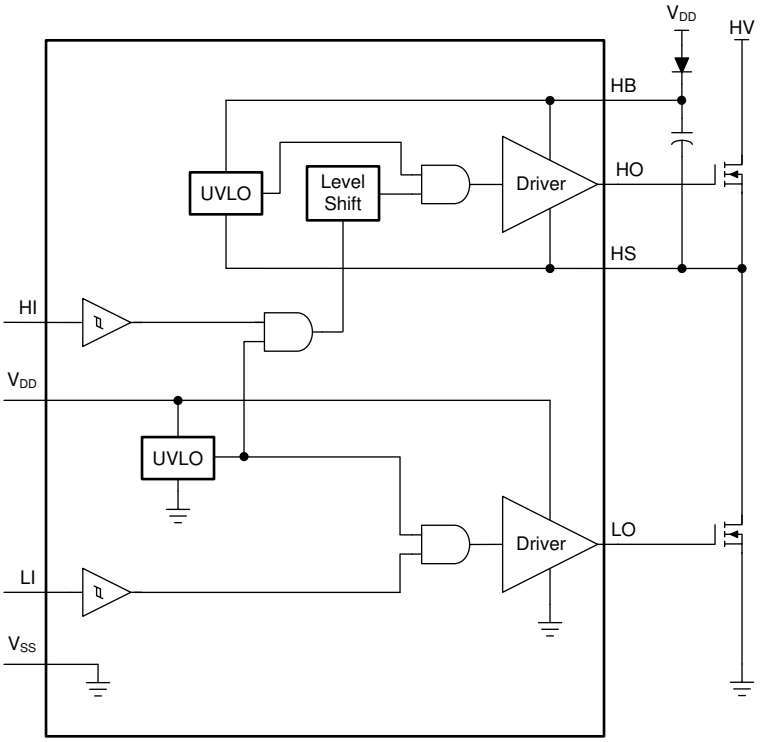

Figure 1-1. Functional Block Diagram

The LM5109B-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LM5109B-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power dissipation (mW)	FIT (Failures Per 10^9 Hours)
Total component FIT rate	50	9
	550	11
Die FIT rate	50	3
	550	5
Package FIT rate	50	6
	550	6

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 50mW, 550 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20	55

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM5109B-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
LO stuck high	16.5
LO stuck low	16.5
LO unknown	16.5
HO stuck low	16.5
HO stuck high	16.5
HO unknown	16.5
Low side UVLO not functional	<1
High side UVLO not functional	<1

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM5109B-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM5109B-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM5109B-Q1 data sheet.

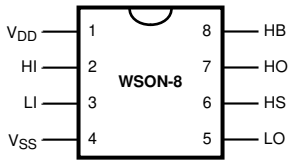

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Short between VDD and HB is not considered.
- Short between VSS and LO is not considered.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	The device is not powered.	C
HI	2	HO is pulled low (sinking is on). HI is stuck low.	C
LI	3	LO is pulled low (sinking is on). LI is stuck low.	C
VSS	4	No impact. Short to same potential.	D
LO	5	LO is stuck low.	A
HS	6	HS is stuck low. Power FET short circuit HV and HS when HI = H is commanded.	D
HO	7	HO is stuck low. Device damage is possible when HI = H is commanded.	A
HB	8	HO is stuck low. Boot diode damage is possible.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	The device is not powered.	D
HI	2	HI is pulled down by the internal pulldown resistor. HO is pulled down (sinking is on).	C
LI	3	LI is pulled down by the internal pulldown resistor. LO is pulled down (sinking is on).	C
VSS	4	HI and LI float to VDD level. HO and LO float to VDD level.	C
LO	5	LO is disconnected from the gate of the power FET.	D
HS	6	Low side output has no supply. LO is pulled down (sinking is on).	C
HO	7	HO is disconnected from the gate of the power FET.	D
HB	8	High-side output has no supply. HO is pulled down (sinking is on).	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDD	1	HI	HI is stuck high. HO is pulled up (sourcing is on).	C
HI	2	LI	HI and LI are undefined.	C
LI	3	VSS	LI is stuck low.	C
VSS	4	N/A	N/A	N/A
LO	5	HS	LO is in an overvoltage condition and potentially exposed to VIN level when HI = H is commanded.	A
HS	6	HO	High-side HO output level is 0 (HO-HS). High-side power FET is off (VGS is stuck low).	A
HO	7	HB	HO is stuck high. HO is pulled up to VDD level. Power FET damage is possible when LI = H is commanded.	A
HB	8	N/A	N/A	N/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	No impact. Short to same potential.	D
HI	2	HI is stuck high. HO is pulled up (sourcing is on).	C
LI	3	LI is stuck high. LO is pulled up (sourcing is on).	C
VSS	4	VDD short to VSS The device is not powered.	C
LO	5	LO is stuck high and device damage is possible. Power FET damage is possible when HI = H is commanded.	A
HS	6	HO (and HS) is pulled to VDD level.	C
HO	7	HO is stuck high and device damage is possible. Power FET damage is possible when LI = H is commanded.	A
HB	8	HO output voltage (sourcing on) is lower than the specified range.	C

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