Functional Safety Information

CD74HCT4051-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the CD74HCT4051-Q1 SOIC package to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

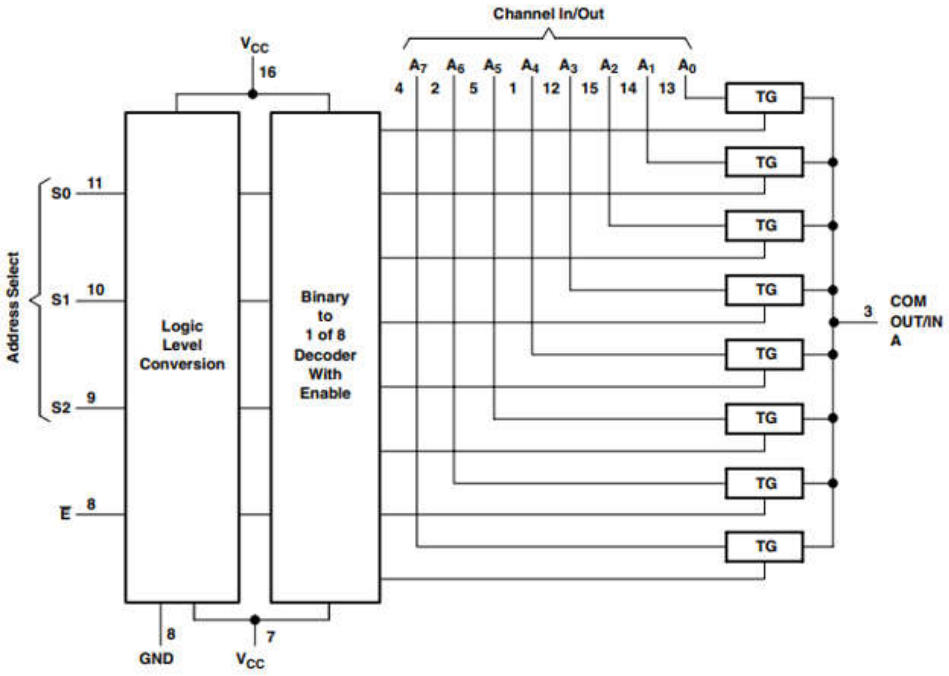

Figure 1-1. Functional Block Diagram

The CD74HCT4051-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the SOIC package of the CD74HCT4051-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	22
Die FIT rate	3
Package FIT rate	19

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 169 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS ASICs Analog and Mixed =< 50V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the CD74HCT4051-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
MUX no output (HIZ)	30
MUX channel stuck on	15
MUX channel stuck off	15
MUX functional out of specification voltage or timing	40

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the CD74HCT4051-Q1 (SOIC package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)
- Pin short-circuited to VEE (see Table 4-6)

Table 4-2 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the CD74HCT4051-Q1 pin diagram for the SOIC package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the CD74HCT4051-Q1data sheet.

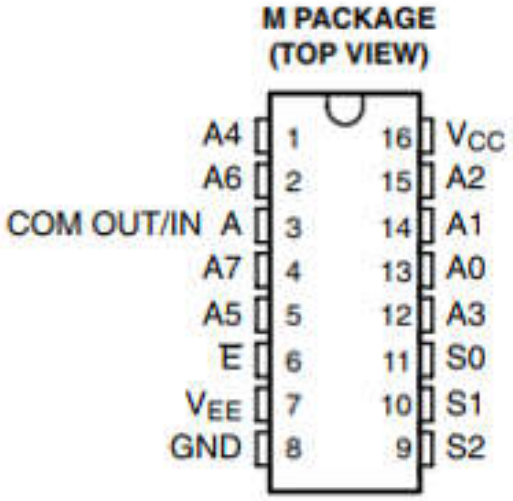

Figure 4-1. Pin Diagram (SOIC) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A4	1	Corruption of analog signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, device damage is possible.	A
A6	2	Corruption of analog signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, device damage is possible.	A
COM OUT/IN A	3	Corruption of analog signal passed onto the Ax pins. If there is no limiting resistor in the switch path, device damage is possible.	A
A7	4	Corruption of analog signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, device damage is possible.	A
A5	5	Corruption of analog signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, device damage is possible.	A
E	6	E stuck low. Cannot control switch states.	B
VEE	7	There is no effect; this is normal operation, if the switch path signal voltages are positive. Possible damage to the device if the switch path signal voltages are negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
GND	8	There is no effect; this is normal operation.	D
S2	9	Control of the address pin is lost. Cannot control switch.	B
S1	10	Control of the address pin is lost. Cannot control switch.	B
S0	11	Control of the address pin is lost. Cannot control switch.	B
A3	12	Corruption of analog signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, device damage is possible.	A
A0	13	Corruption of analog signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, device damage is possible.	A
A1	14	Corruption of analog signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, device damage is possible.	A
A2	15	Corruption of analog signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, device damage is possible.	A
VCC	16	Device unpowered. Device not functional.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A4	1	Corruption of analog signal passed onto the COM OUT/IN A pin.	B
A6	2	Corruption of analog signal passed onto the COM OUT/IN A pin.	B
COM OUT/IN A	3	Corruption of analog signal passed onto the Ax pins.	B
A7	4	Corruption of analog signal passed onto the COM OUT/IN A pin.	B
A5	5	Corruption of analog signal passed onto the COM OUT/IN A pin.	B
E	6	Loss of control of E pin. Cannot disable switch. Defaults to switches enabled.	B
VEE	7	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
GND	8	Device unpowered. Device not functional.	B
S2	9	Control of the address pin is lost. Cannot control switch.	B
S1	10	Control of the address pin is lost. Cannot control switch.	B
S0	11	Control of the address pin is lost. Cannot control switch.	B
A3	12	Corruption of analog signal passed onto the COM OUT/IN A pin.	B
A0	13	Corruption of analog signal passed onto the COM OUT/IN A pin.	B
A1	14	Corruption of analog signal passed onto the COM OUT/IN A pin.	B
A2	15	Corruption of analog signal passed onto the COM OUT/IN A pin.	B
VCC	16	Device unpowered. Device not functional.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effects	Failure Effect Class
A4	1	A6	Possible corruption of analog signal passed onto Ax and COM pin.	B
A6	2	COM OUT/IN A	Possible corruption of analog signal passed onto Ax and COM pin.	B
COM OUT/IN A	3	A7	Possible corruption of analog signal passed onto Ax and COM pin.	B
A7		A5	Possible corruption of analog signal passed onto Ax and COM pin.	B
A5	5	E	Possible corruption of the signal passed onto the COM pin. Switch state will be undefined.	B
E	6	VEE	Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
VEE	7	GND	Possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
GND	8	S2	Not considered; corner pin.	D
S2	9	S1	Control of the switch state is lost.	B
S1	10	S0	Control of the switch state is lost.	B
S0	11	A3	Possible corruption of the signal passed onto the Ax and COM pin. Control of the switch state is lost.	B
A3	12	A0	Possible corruption of the signal passed onto the Ax and COM pin.	B
A0	13	A1	Possible corruption of the signal passed onto the Ax and COM pin.	B
A1	14	A2	Possible corruption of the signal passed onto the Ax and COM pin.	B
A2	15	VCC	Corruption of the signal passed onto the Ax pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	16	A4	Not considered, corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A4	1	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
A6	2	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
COM OUT/IN A	3	Corruption of the signal passed onto the Ax pins. If there is no limiting resistor in the switch path, then device damage is possible.	A
A7	4	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
A5	5	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
E	6	E stuck high. Can no longer enable the device. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
VEE	7	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
GND	8	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
S2	9	Address stuck high. Cannot control switch states.	B
S1	10	Address stuck high. Cannot control switch states.	B
S0	11	Address stuck high. Cannot control switch states.	B
A3	12	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
A0	13	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
A1	14	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
A2	15	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	16	No effect. Normal operation.	D

Table 4-6. Pin FMA for Device Pins Short-Circuited to VEE

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A4	1	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
A6	2	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
COM OUT/IN A	3	Corruption of the signal passed onto the Ax pins. If there is no limiting resistor in the switch path, then device damage is possible.	A
A7	4	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
A5	5	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
E	6	Possible damage to the device if signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
VEE	7	No effect. Normal operation.	D
GND	8	Possible damage to the device if signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
S2	9	Possible damage to the device if signal voltage is negative. Cannot control switch states. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
S1	10	Possible damage to the device if signal voltage is negative. Cannot control switch states. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
S0	11	Possible damage to the device if signal voltage is negative. Cannot control switch states. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
A3	12	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
A0	13	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
A1	14	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
A2	15	Corruption of the signal passed onto the COM OUT/IN A pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	16	Possible damage to the device if signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A

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