Functional Safety Information

TMCS1123-Q1, TMCS1126-Q1, TMCS1127-Q1, and TMCS1133-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TMCS1123-Q1, TMCS1126-Q1, TMCS1127-Q1, and TMCS1133-Q1 (SOIC package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram of TMCS1123-Q1 for reference. Refer to the individual data sheets for the function block diagram of the actual product.

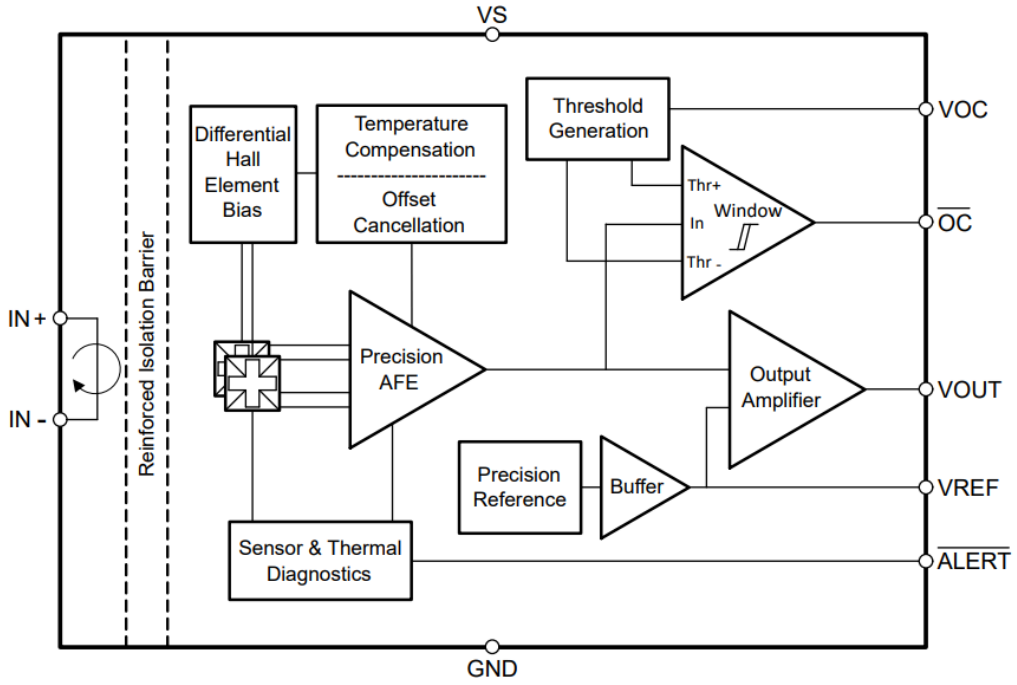

Figure 1-1. TMCS1123-Q1Functional Block Diagram

The TMCS1123-Q1, TMCS1126-Q1, TMCS1127-Q1, and TMCS1133-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TMCS1123-Q1, TMCS1126-Q1, TMCS1127-Q1, and TMCS1133-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	62
Die FIT rate	26
Package FIT rate	36

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 4500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs Analog and Mixed = <50V supply	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimations covered in this document are for:

- TMCS1123-Q1 (see Table 3-1)
- TMCS1126-Q1 (see Table 3-2)
- TMCS1127-Q1 (see Table 3-3)
- TMCS1133-Q1 (see Table 3-4)

The failure mode distribution estimation comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. TMCS1123-Q1 Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	5
VOUT stuck (high or low)	25
VOUT functional, not in specification	25
VREF open (Hi-Z)	5
VREF stuck (high or low)	5
VREF functional, not in specification	5
$\overline{OC}$ false trip, failure to trip	15
$\overline{ALERT}$ false trip, failure to trip	15

Table 3-2. TMCS1126-Q1 Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	10
VOUT stuck (high or low)	20
VOUT functional, not in specification	20
VREF open (Hi-Z)	10
VREF stuck (high or low)	10
VREF functional, not in specification	10
$\overline{OC}$ false trip, failure to trip	20

Table 3-3. TMCS1127-Q1 Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT Stuck (high or low)	45
VOUT functional, not in specification	45
VOUT open (Hi-Z)	10

Table 3-4. TMCS1133-Q1 Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	5
VOUT stuck (high or low)	30
VOUT functional, not in specification	30
$\overline{OC}$ false trip, failure to trip	15
$\overline{ALERT}$ false trip, failure to trip	20

The FMD in Table 3-1, Table 3-2, Table 3-3, and Table 3-4 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

4.1 TMCS1123-Q1 Pin FMA

This section provides a failure mode analysis (FMA) for the pins of the TMCS1123-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TMCS1123-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMCS1123-Q1 data sheet.

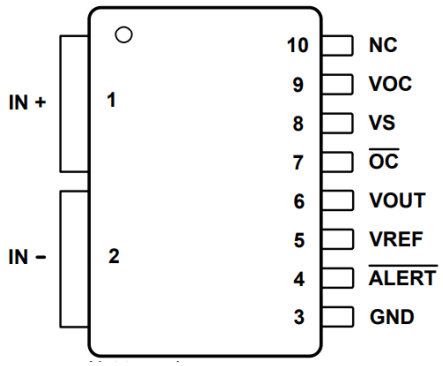

Figure 4-1. TMCS1123-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 3V to 5.5V
- V_{CM} = -1.3kV to 1.3kV

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	For forward current, hall-sensor bypassed, providing no signal to be sensed and amplified. If the IN+ pin is at a large potential above GND, this state results in a large amount of current being sunk. Depending upon layout and configuration, this result can damage the input current system supply, the load device, or the actual device.	A
IN-	2	For reverse current, hall-sensor bypassed, providing no signal to be sensed and amplified. If the IN- pin is at a large potential above GND, this state results in a lot of current being sunk. Depending upon layout and configuration, this result can damage the input current system supply, the load device, or the actual device.	A
GND	3	Normal operation.	D
$\overline{\text{ALERT}}$	4	The alert is not able to trigger since $\overline{\text{ALERT}}$ is shorted to GND.	B
VREF	5	VREF is shorted to GND and the output current is short circuit limited.	B
VOUT	6	Output is pulled to GND and the output current is short circuit limited. When left in this configuration, while VS is connected to a high-load-capable supply and for certain high-load conditions through the IN+ and IN- pins, the die temperature can approach or exceed 150°C.	A
$\overline{\text{OC}}$	7	The alert is not able to trigger since $\overline{\text{OC}}$ is shorted to GND.	B
VS	8	Power supply is shorted to ground.	B
VOC	9	The threshold at GND means that all voltages trip the alert. As a result, the alert is stuck in active mode.	B
NC	10	Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	No current running through inputs.	B
IN-	2	No current running through inputs.	B
GND	3	GND is floating. Output is incorrect as the output is no longer referenced to GND.	B
$\overline{\text{ALERT}}$	4	Alert open; cannot read alert.	B
VREF	5	Normal operation.	D
VOUT	6	Output is present at the pin, having no loading does not affect the output. However, the user sees unpredictable results further down on the signal chain.	B
$\overline{\text{OC}}$	7	Alert open, cannot read alert.	B
VS	8	No power to the device. VOUT stays close to GND.	B
VOC	9	No alert threshold is set. The alert output is unpredictable.	B
NC	10	Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN+	1	IN-	IN+ is shorted to IN-. This state creates a current divider which increases sensitivity error inversely proportional to the resistance of the short.	C
IN-	2	GND	For reverse current, hall-sensor bypassed, providing no signal to be sensed and amplified. If the IN- pin is at a large potential above GND, this state results in a large amount of current being sunk. Depending upon layout and configuration, this result can damage the input current system supply, the load device, or the actual device.	A
GND	3	$\overline{\text{ALERT}}$	Alert is not able to trigger since $\overline{\text{ALERT}}$ is shorted to GND.	B
$\overline{\text{ALERT}}$	4	VREF	Alert is not able to trigger.	B
VREF	5	VOUT	The output is potentially incorrect.	B
VOUT	6	$\overline{\text{OC}}$	$\overline{\text{OC}}$ and output are incorrect.	A
$\overline{\text{OC}}$	7	VS	$\overline{\text{OC}}$ is shorted to VS. Large current can be pulled from VS.	A
VS	8	VOC	VOC is shorted to VS, the overcurrent threshold is at the wrong threshold.	B
VOC	9	NC	No alert threshold is set. The alert output is unpredictable.	B
NC	10	IN+	If IN+ > 6V, the device can be damaged. If NC is at VS and IN+ < Vs, or if NC is at GND and IN+ is at a large potential above ground, large current can be flowing between VS and the input current system supply.	A if IN+ > 6V
				B otherwise

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	If IN+ > 6V, the device is damaged. If IN+ < Vs, a large amount of current can be pulled from VS.	A
IN-	2	If IN- > 6V, the device is damaged. If IN- < Vs, a large amount of current can be pulled from VS.	A
GND	3	VS is shorted to GND.	B
$\overline{\text{ALERT}}$	4	The $\overline{\text{ALERT}}$ pin is stuck high and potentially has too high of a current draw when triggered.	B
VREF	5	VREF is shorted to VS and the output current is short circuit limited.	B
VOUT	6	Output is pulled to VS and the output current is short circuit limited. When left in this configuration, while VS is connected to a high-load-capable VS and for certain high-load conditions through the IN+ and IN- pins, the die temperature can approach or exceed 150°C.	A
$\overline{\text{OC}}$	7	The $\overline{\text{OC}}$ pin is stuck high and potentially has too high of a current draw when triggered.	B
VS	8	Normal operation.	D
VOC	9	The overcurrent threshold at the wrong threshold.	B
NC	10	Normal operation.	D

4.2 TMCS1126-Q1 Pin FMA

This section provides a failure mode analysis (FMA) for the pins of the TMCS1126-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-6)
- Pin open-circuited (see Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-8)
- Pin short-circuited to supply (see Table 4-9)

Table 4-6 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Figure 4-2 shows the TMCS1126-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMCS1126-Q1 data sheet.

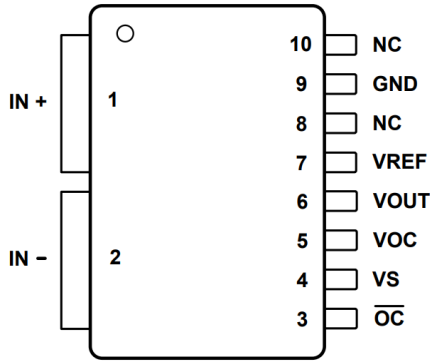

Figure 4-2. TMCS1126-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 3V to 5.5V
- V_{CM} = -1.3kV to 1.3kV

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	For forward current, hall-sensor bypassed, providing no signal to be sensed and amplified. If the IN+ pin is at a large potential above GND, this state results in a large amount of current being sunk. Depending upon layout and configuration, this result can damage the input current system supply, the load device, or the actual device.	A
IN-	2	For reverse current, hall-sensor bypassed, providing no signal to be sensed and amplified. If the IN- pin is at a large potential above GND, this state results in a large amount of current being sunk. Depending upon layout and configuration, this result can damage the input current system supply, the load device, or the actual device.	A
$\overline{OC}$	3	Alert is not able to trigger since $\overline{OC}$ is shorted to GND.	B
VS	4	Power supply is shorted to ground.	B
VOC	5	Threshold at GND means that all voltages trip the alert. As a result, the alert is stuck in active mode.	B
VOUT	6	Output pulled to GND and output current are short circuit limited. When left in this configuration, while VS is connected to a high-load-capable supply and for certain high-load conditions through the IN+ and IN- pins, the die temperature can potentially approach or exceed 150°C.	A
VREF	7	VREF is shorted to GND and the output current is short circuit limited.	B
NC	8	Normal operation.	D
GND	9	Normal operation.	D
NC	10	Normal operation.	D

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	No current running through inputs.	B
IN-	2	No current running through inputs.	B
$\overline{OC}$	3	Alert open; cannot read alert.	B
VS	4	No power to device. VOUT stays close to GND.	B
VOC	5	No alert threshold is set. Alert output is unpredictable.	B
VOUT	6	Output is present at the pin, having no loading does not affect the output. However, the user sees unpredictable results further down on the signal chain.	B
VREF	7	VREF is present at the pin, no loading does not affect the device. However, the user sees unpredictable results further down on the signal chain.	B
NC	8	Normal operation.	D
GND	9	GND is floating. Output is incorrect as the output is no longer referenced to GND.	B
NC	10	Normal operation.	D

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN+	1	IN-	IN+ is shorted to IN-. This creates a current divider which increases sensitivity error inversely proportional to the resistance of the short.	C
IN-	2	$\overline{OC}$	IN- is shorted to $\overline{OC}$. If IN- > 6V, the device is damaged. If IN- < OC, large current can be pulled from VS.	A
$\overline{OC}$	3	VS	$\overline{OC}$ is shorted to VS. Large current can be pulled from VS.	A
VS	4	VOC	VOC is shorted to VS, overcurrent threshold is at the wrong threshold.	B
VOC	5	VOUT	VOC is shorted to VOUT. Overcurrent threshold varies, alert response is unpredictable.	B
VOUT	6	VREF	Output is shorted to VREF. Based on the voltage level of each, the output current can potentially be short circuit limited. When left in this configuration, while VS is connected to a high-load-capable supply and for certain high-load conditions through the IN+ and IN- pins, the die temperature can approach or exceed 150°C.	A
VREF	7	NC	Normal operation.	D
NC	8	GND	Normal operation.	D
GND	9	NC	Normal operation.	D
NC	10	IN+	If IN+ > 6V, the device can be damaged. If NC is at VS and IN+ < Vs, or if NC is at GND and IN+ is at a large potential above ground, large current can be flowing between VS and the input current system supply.	A if IN+ > 6V B otherwise

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	If IN+ > 6V, the device is damaged. If IN+ < Vs, a large amount of current can be pulled from VS.	A
IN-	2	If IN- > 6V, the device is damaged. If IN- < Vs, a large amount of current can be pulled from VS.	A
$\overline{OC}$	3	$\overline{OC}$ pin stuck high, potentially has too high of a current draw when triggered.	B
VS	4	Normal operation.	D
VOC	5	Overcurrent threshold at the wrong threshold.	B
VOUT	6	Output pulled to VS and output current is short circuit limited. When left in this configuration, while VS is connected to a high-load-capable VS and for certain high-load conditions through the IN+ and IN- pins, the die temperature can approach or exceed 150°C.	A
VREF	7	VREF is shorted to VS and the output current is short circuit limited.	B
NC	8	Normal operation.	D
GND	9	VS is shorted to GND.	B
NC	10	Normal operation.	D

4.3 TMCS1127-Q1 Pin FMA

This section provides a failure mode analysis (FMA) for the pins of the TMCS1127-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-10)
- Pin open-circuited (see Table 4-11)
- Pin short-circuited to an adjacent pin (see Table 4-12)
- Pin short-circuited to supply (see Table 4-13)

Table 4-10 through Table 4-13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Figure 4-3 shows the TMCS1127-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMCS1127-Q1 data sheet.

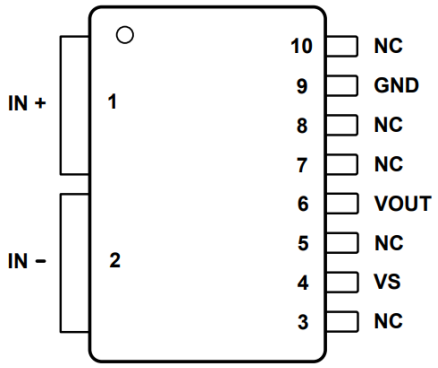

Figure 4-3. TMCS1127-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 3V to 5.5V
- V_{CM} = -1.3kV to 1.3kV

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	For forward current, hall-sensor bypassed, providing no signal to be sensed and amplified. If the IN+ pin is at a large potential above GND, this state results in a lot of current being sunk. Depending upon layout and configuration, this result can damage the input current system supply, the load device, or the actual device.	A
IN-	2	For reverse current, hall-sensor bypassed, providing no signal to be sensed and amplified. If the IN- pin is at a large potential above GND, this state results in a lot of current being sunk. Depending upon layout and configuration, this result can damage the input current system supply, the load device, or the actual device.	A
NC	3	Normal operation.	D
VS	4	Power supply is shorted to ground.	B
NC	5	Normal operation.	D
VOUT	6	Output is pulled to GND and the output current is short circuit limited. When left in this configuration, while VS connected to a high-load-capable supply and for certain high-load conditions through the IN+ and IN- pins, the die temperature can approach or exceed 150°C.	A
NC	7	Normal operation.	D
NC	8	Normal operation.	D
GND	9	Normal operation.	D
NC	10	Normal operation.	D

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	No current running through inputs.	B
IN-	2	No current running through inputs.	B
NC	3	Normal operation.	D
VS	4	No power to the device. VOUT stays close to GND.	B
NC	5	Normal operation.	D
VOUT	6	Output is present at the pin, having no loading does not affect the output. However, the user sees unpredictable results further down on the signal chain.	B
NC	7	Normal operation.	D
NC	8	Normal operation.	D
GND	9	GND is floating. Output is incorrect as the output is no longer referenced to GND.	B
NC	10	Normal operation.	D

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN+	1	IN-	IN+ shorted to IN-. This creates a current divider which increases sensitivity error inversely proportional to the resistance of the short.	C
IN-	2	NC	If IN- > 6V, the device can be damaged. If NC is at VS and IN- < Vs, or if NC is at GND and IN- is at a large potential above ground, large current can be flowing between VS and the input current system supply.	A if IN- > 6V
				B otherwise
NC	3	VS	Normal operation.	D
VS	4	NC	Normal operation.	D
NC	5	VOUT	Normal operation.	D
VOUT	6	NC	Normal operation.	D
NC	7	NC	Normal operation	D
NC	8	GND	Normal operation.	D
GND	9	NC	Normal operation.	D
NC	10	IN+	If IN+ > 6V, the device can be damaged. If NC is at VS and IN+ < Vs, or if NC is at GND and IN+ is at a large potential above ground, large current can be flowing between VS and the input current system supply.	A if IN+ > 6V
				B otherwise

Table 4-13. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	If IN+ > 6V, the device is damaged. If IN+ < Vs, a large amount of current can be pulled from VS.	A
IN-	2	If IN- > 6V, the device is damaged. If IN- < Vs, a large amount of current can be pulled from VS.	A
NC	3	Normal operation.	D
VS	4	Normal operation.	D
NC	5	Normal operation.	NC
VOUT	6	The output is pulled to VS and the output current is short circuit limited. When left in this configuration, while VS is connected to a high-load-capable VS and for certain high-load conditions through the IN+ and IN- pins, the die temperature can approach or exceed 150°C.	A
NC	7	Normal operation.	D
NC	8	Normal operation.	D
GND	9	VS is shorted to GND.	B
NC	10	Normal operation.	D

4.4 TMCS1133-Q1 Pin FMA

This section provides a failure mode analysis (FMA) for the pins of the TMCS1133-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-14)
- Pin open-circuited (see Table 4-15)
- Pin short-circuited to an adjacent pin (see Table 4-16)
- Pin short-circuited to supply (see Table 4-17)

Table 4-14 through Table 4-17 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Figure 4-4shows the TMCS1133-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMCS1133-Q1 data sheet.

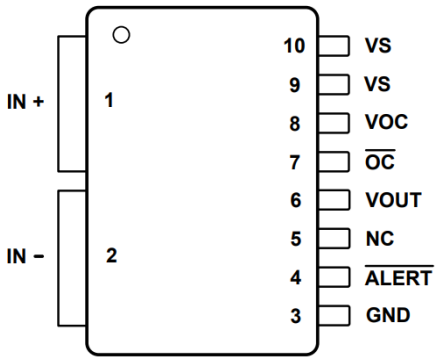

Figure 4-4. TMCS1133-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 3V to 5.5V
- V_{CM} = -1.3kV to 1.3kV

Table 4-14. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	For forward current, hall-sensor bypassed, providing no signal to be sensed and amplified. If the IN+ pin is at a large potential above GND, this state results in a large amount of current being sunk. Depending upon layout and configuration, this result can damage the input current system supply, the load device, or the actual device.	A
IN-	2	For reverse current, hall-sensor bypassed, providing no signal to be sensed and amplified. If the IN- pin is at a large potential above GND, this state result in a large amount of current being sunk. Depending upon layout and configuration, this result can damage the input current system supply, the load device, or the actual device.	A
GND	3	Normal operation.	D
$\overline{\text{ALERT}}$	4	Alert is not able to trigger since $\overline{\text{ALERT}}$ is shorted to GND.	B
NC	5	Normal operation.	D
VOUT	6	Output is pulled to GND and the output current is short circuit limited. When left in this configuration, while VS is connected to a high-load-capable supply and for certain high-load conditions through the IN+ and IN- pins, the die temperature can approach or exceed 150°C.	A
$\overline{\text{OC}}$	7	Alert is not able to trigger since $\overline{\text{OC}}$ is shorted to GND.	B
VOC	8	The threshold at GND means that all voltages trip the alert. As a result, the alert is stuck in active mode.	B
VS	9	Power supply is shorted to ground.	B
VS	10	Power supply is shorted to ground.	B

Table 4-15. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	No current running through inputs.	B
IN-	2	No current running through inputs.	B
GND	3	GND is floating. The output is incorrect as the output is no longer referenced to GND.	B
$\overline{\text{ALERT}}$	4	Alert open; cannot read alert.	B
NC	5	Normal operation.	D
VOUT	6	Output is present at the pin, having no loading does not affect the output. However, the user sees unpredictable results further down on the signal chain.	B
$\overline{\text{OC}}$	7	Alert open, cannot read alert.	B
VOC	8	No alert threshold set. Alert output is unpredictable.	B
VS	9	No power to the device if both VS pins are open.	B if both VS pins open
			D otherwise
VS	10	No power to the device if both VS pins are open.	B if both VS pins open
			D otherwise

Table 4-16. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN+	1	IN-	IN+ shorted to IN-. This creates a current divider which increases sensitivity error inversely proportional to the resistance of the short.	C
IN-	2	GND	For reverse current, hall-sensor bypassed, providing no signal to be sensed and amplified. If the IN- pin is at a large potential above GND, this state result in a large amount of current being sunk. Depending upon layout and configuration, this result can damage the input current system supply, the load device, or the actual device.	A
GND	3	$\overline{\text{ALERT}}$	Alert is not able to trigger since $\overline{\text{ALERT}}$ is shorted to GND.	B
$\overline{\text{ALERT}}$	4	NC	Normal operation.	D
NC	5	VOUT	Normal operation.	D
VOUT	6	$\overline{\text{OC}}$	$\overline{\text{OC}}$ and output are incorrect.	A
$\overline{\text{OC}}$	7	VOC	$\overline{\text{OC}}$ is unpredictable.	B
VOC	8	VS	VOC is shorted to VS, overcurrent threshold is at the wrong threshold.	B
VS	9	VS	Normal operation.	D
VS	10	IN+	If IN+ > 6V, the device can be damaged. If IN+ < Vs and IN+ is at a large potential above ground, large current can be flowing between VS and the input current system supply.	A if IN+ > 6V B otherwise

Table 4-17. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	If IN+ > 6V, the device is damaged. If IN+ < Vs, a large amount of current can be pulled from VS.	A
IN-	2	If IN- > 6V, the device is damaged. If IN- < Vs, a large amount of current can be pulled from VS.	A
GND	3	VS is shorted to GND.	B
$\overline{\text{ALERT}}$	4	The $\overline{\text{ALERT}}$ pin is stuck high and potentially has too high of a current draw when triggered.	B
NC	5	Normal operation.	D
VOUT	6	Output is pulled to VS and the output current is short circuit limited. When left in this configuration, while VS is connected to a high-load-capable VS and for certain high-load conditions through the IN+ and IN- pins, the die temperature can approach or exceed 150°C.	A
$\overline{\text{OC}}$	7	The $\overline{\text{OC}}$ pin is stuck high and potentially has too high of a current draw when triggered.	B
VOC	8	The overcurrent threshold is at the wrong threshold.	B
VS	9	Normal operation.	D
VS	10	Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2024) to Revision A (May 2025) **Page**

- Added TMCS1123-Q1, TMCS1127-Q1, and TMCS1133-Q1 devices..... 2

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