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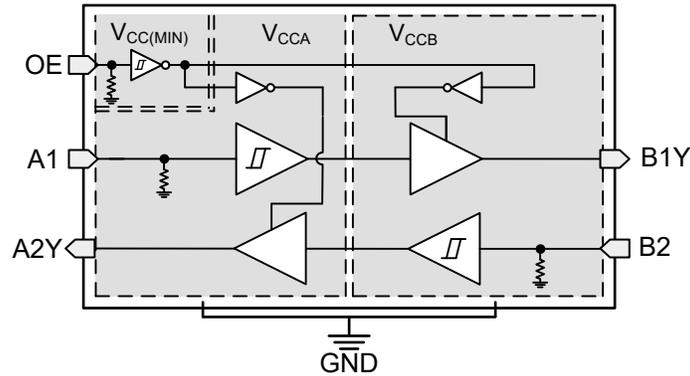
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## 1 Overview

This document contains information for TXU0202-Q1 (VSSOP and SON package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



**Figure 1-1. Functional Block Diagram**

TXU0202-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for VSSOP package of TXU0202-Q1 based on industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per 10 <sup>9</sup> Hours) |
|------------------------------|--|
| Total Component FIT Rate     | 4  |
| Die FIT Rate                 | 2  |
| Package FIT Rate             | 2  |

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 15 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category                          | Reference FIT Rate | Reference Virtual T <sub>J</sub> |
|-------|-----------------------------------|--------------------|----------------------------------|
| 5     | CMOS Analog switch, Bus Interface | 8 FIT              | 55°C                             |

The Reference FIT Rate and Reference Virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TXU0202-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes                                       | Failure Mode Distribution (%) |
|---|-------------------------------|
| Driver HIZ; no output                                   | 35%                           |
| Functional fail (voltage, timing; out of specification) | 24%                           |
| Driver stuck at fault high                              | 11%                           |
| Driver stuck at fault low                               | 13%                           |
| Driver stuck at undetermined state                      | 17%                           |

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TXU0202-Q1 (VSSOP and SON package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#) and [Table 4-6](#))

[Table 4-2](#) through [Table 4-6](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

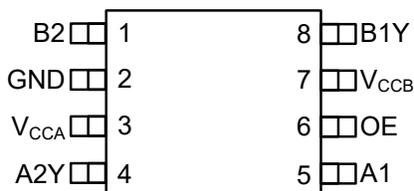
**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects   |
|-------|---|
| A     | Potential device damage that affects functionality          |
| B     | No device damage, but loss of functionality                 |
| C     | No device damage, but performance degradation               |
| D     | No device damage, no impact to functionality or performance |

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

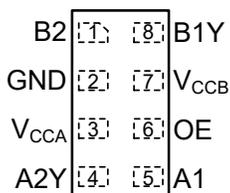
- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#) and [Table 4-6](#))

[Figure 4-1](#) shows the TXU0202-Q1 pin diagram for the VSSOP package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TXU0202-Q1 data sheet.



**Figure 4-1. Pin Diagram (VSSOP) Package**

[Figure 4-2](#) shows the TXU0202-Q1 pin diagram for the SON package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TXU0202-Q1 data sheet.



**Figure 4-2. Pin Diagram (SON Package)**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s)   | Failure Effect Class |
|----------|---------|--|----------------------|
| B2       | 1       | Bx will be LOW, if corresponding Ax is HIGH, there will be potential damage to the device if the current is not limited. If corresponding Ax is LOW, then nothing will occur, no damage. | B                    |
| GND      | 2       | Normal operation.  | D                    |
| VCCA     | 3       | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario.  | B                    |
| A2Y      | 4       | Ax will be LOW, if corresponding Bx is HIGH, there will be potential damage to the device if the current is not limited. If corresponding Bx is LOW, then nothing will occur, no damage. | B                    |
| A1       | 5       |  | B                    |
| OE       | 6       | All I/Os will be fixed into high impedance (tri-state).  | B                    |
| VCCB     | 7       | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario.  | B                    |
| B1Y      | 8       | Bx will be LOW, if corresponding Ax is HIGH, there will be potential damage to the device if the current is not limited. If corresponding Ax is LOW, then nothing will occur, no damage. | B                    |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s)                 | Failure Effect Class |
|----------|---------|--|----------------------|
| B2       | 1       | Bx pin will be grounded internally.                        | D                    |
| GND      | 2       | Device will not be powered.                                | B                    |
| VCCA     | 3       | Device will not be powered.                                | B                    |
| A2Y      | 4       | Normal operation.  | D                    |
| A1       | 5       | Ax pin will be grounded internally.                        | B                    |
| OE       | 6       | I/Os may be high impedance or active, unknown input state. | A                    |
| VCCB     | 7       | Device will not be powered.                                | B                    |
| B1Y      | 8       | Normal operation.  | D                    |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s)  | Failure Effect Class |
|----------|---------|------------|---|----------------------|
| B2       | 1       | GND        | Bx will be LOW, if corresponding Ax is HIGH, there will be potential damage to the device if the current is not limited. If corresponding Ax is LOW, then nothing will occur, no damage.  | B                    |
| GND      | 2       | VCCA       | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario.   | B                    |
| VCCA     | 3       | A2         | Ax will be HIGH, if corresponding Bx is LOW, there will be potential damage to the device if the current is not limited. If corresponding Bx is HIGH, then nothing will occur, no damage.   | B                    |
| A2Y      | 4       | A1         | One output on VCCA supply is shorted to one input of VCCA supply. Based on the external bus driving this connection, potential high current can be expected if the $V_{ILA} < \text{Input Voltage } A1 < V_{IHA}$ or if A2Y output gets an undeterministic voltage forced on it in presence of a valid input. | A                    |
| A1       | 5       | OE         | If A1 is HIGH, device will be enabled. If A1 is LOW, device will be disabled  | B                    |
| OE       | 6       | VCCB       | All I/Os will be active, device cannot be disabled.   | B                    |
| VCCB     | 7       | B1Y        | Bx will be HIGH, if corresponding Ax is LOW, there will be potential damage to the device if the current is not limited. If corresponding Ax is HIGH, then nothing will occur, no damage.   | B                    |
| B1Y      | 8       | B2         | One output on VCCB supply is shorted to one input of VCCB supply. Based on the external bus driving this connection, potential high current can be expected if the $V_{ILB} < \text{Input Voltage } B2 < V_{IHB}$ or if B1Y output gets an undeterministic voltage forced on it in presence of a valid input. | A                    |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply VCCA**

| Pin Name | Pin No. | Description of Potential Failure Effect(s)  | Failure Effect Class |
|----------|---------|---|----------------------|
| B2       | 1       | Bx will be HIGH, if corresponding Ax is LOW, there will be potential damage to the device if the current is not limited. If corresponding Ax is HIGH, then nothing will occur, no damage. | B                    |
| GND      | 2       | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario.   | B                    |
| VCCA     | 3       | Normal operation.   | D                    |
| A2Y      | 4       | Ax will be HIGH, if corresponding Bx is LOW, there will be potential damage to the device if the current is not limited. If corresponding Bx is HIGH, then nothing will occur, no damage. | B                    |
| A1       | 5       |   | B                    |
| OE       | 6       | All I/Os will be active, device cannot be disabled.   | B                    |
| VCCB     | 7       | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario.   | B                    |
| B1Y      | 8       | Bx will be HIGH, if corresponding Ax is LOW, there will be potential damage to the device if the current is not limited. If corresponding Ax is HIGH, then nothing will occur, no damage. | B                    |

**Table 4-6. Pin FMA for Device Pins Short-Circuited to supply VCCB**

| Pin Name | Pin No. | Description of Potential Failure Effect(s)  | Failure Effect Class |
|----------|---------|---|----------------------|
| B2       | 1       | Bx will be HIGH, if corresponding Ax is LOW, there will be potential damage to the device if the current is not limited. If corresponding Ax is HIGH, then nothing will occur, no damage. | B                    |
| GND      | 2       | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario.   | B                    |
| VCCA     | 3       | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario.   | B                    |
| A2Y      | 4       | Ax will be HIGH, if corresponding Bx is LOW, there will be potential damage to the device if the current is not limited. If corresponding Bx is HIGH, then nothing will occur, no damage. | B                    |
| A1       | 5       |   | B                    |
| OE       | 6       | All I/Os will be active, device cannot be disabled.   | B                    |
| VCCB     | 7       | Normal operation.   | D                    |
| B1Y      | 8       | Bx will be HIGH, if corresponding Ax is LOW, there will be potential damage to the device if the current is not limited. If corresponding Ax is HIGH, then nothing will occur, no damage. | B                    |

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