*Functional Safety Information*

# *TXU0304-Q1*
# *Functional Safety FIT Rate, FMD and Pin FMA*

## Table of Contents



## Trademarks

# 1 Overview

This document contains information for TXU0304-Q1 (TSSOP-14 and VQFN-14 packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

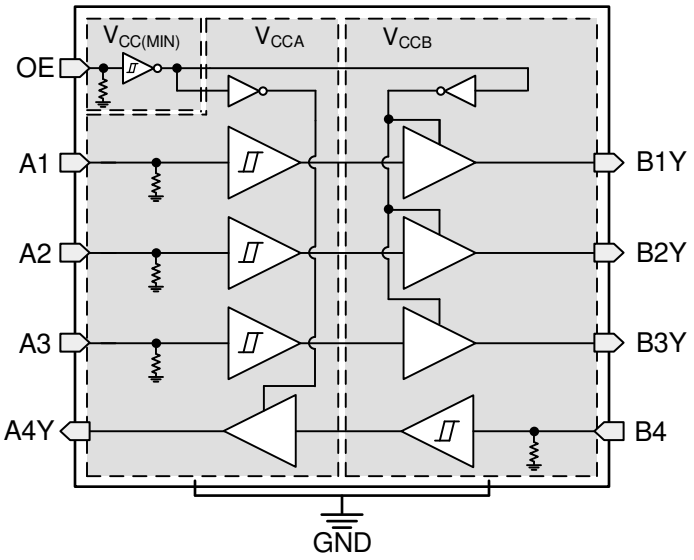


**Figure 1-1. Functional Block Diagram**

TXU0304-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

# 2 Functional Safety Failure In Time (FIT) Rates

## 2.1 TSSOP-14 Package

This section provides Functional Safety Failure In Time (FIT) rates for TSSOP-14 package of TXU0304-Q1 based on industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 8 |
| Die FIT Rate | 2 |
| Package FIT Rate | 6 |

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 30 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

## 2.2 VQFN-14 Package

This section provides Functional Safety Failure In Time (FIT) rates for the VQFN-14 package of TXU0304-Q1 based on industry-wide used reliability standards:

- Table 2-2 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

**Table 2-2. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 9 |
| Die FIT Rate | 2 |
| Package FIT Rate | 7 |

The failure rate and mission profile information in Table 2-2 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 30 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

## 2.3 TSSOP-14 and VQFN-14 Package

This section provides Functional Safety Failure In Time (FIT) rates for TSSOP-14 andVQFN-14 package of TXU0304-Q1 based on industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

**Table 2-3. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS Analog switch, Bus Interface | 5 FIT | 55°C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-3 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TXU0304-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| Die Failure Modes | Failure Mode Distribution (%) |
| Driver HIZ no output | 23% |
| Functional fail (voltage, timing, out of specification) | 26% |
| Driver stuck at fault high | 16% |
| Driver stuck at fault low | 15% |
| Driver stuck at undetermined state | 20% |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TXU0304-Q1 (TSSOP-14 and VQFN-14 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5 and Table 4-6)

Table 4-2 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5 and Table 4-6)

## 4.1 TSSOP-14 and VQFN-14 Packages

Figure 4-1 shows the TXU0304-Q1 pin diagram for the TSSOP-14 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TXU0304-Q1 data sheet.

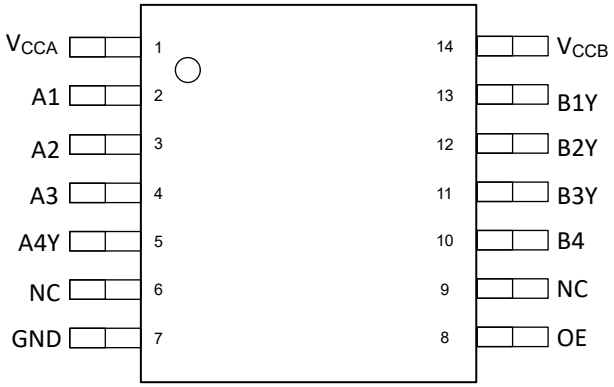


**Figure 4-1. Pin Diagram (TSSOP-14) Package**

Figure 4-2 shows the TXU0304-Q1 pin diagram for the VQFN-14 package. For a detailed description of the device pins, refer to the *Pin Configuration and Functions* section in the TXU0304-Q1 data sheet.

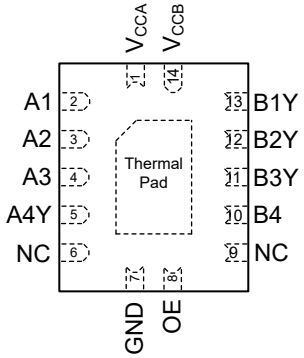


**Figure 4-2. Pin Diagram (VQFN-14 Package)**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VCCA | 1 | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario. | B |
| A1 | 2 | Ax will be LOW, if corresponding Bx is HIGH, there will be potential damage to the device if the current is not limited. If corresponding Bx is LOW, then nothing will occur, no damage. | B |
| A2 | 3 | | B |
| A3 | 4 | | B |
| A4Y | 5 | | B |
| NC | 6 | Normal operation. | D |
| GND | 7 | Normal operation. | D |
| OE | 8 | All I/Os will be fixed into high impedance (tri-state). | B |
| NC | 9 | Normal operation. | D |
| B4 | 10 | Bx will be LOW, if corresponding Ax is HIGH, there will be potential damage to the device if the current is not limited. If corresponding Ax is LOW, then nothing will occur, no damage. | B |
| B3Y | 11 | | B |
| B2Y | 12 | | B |
| B1Y | 13 | | B |
| VCCB | 14 | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VCCA | 1 | Device will not be powered. | B |
| A1 | 2 | Ax input pins will be grounded internally. Ax output pin will in HiZ if device is disabled. If device is enabled, it will be HIGH or LOW depending on the input. | D |
| A2 | 3 | | D |
| A3 | 4 | | D |
| A4Y | 5 | | D |
| NC | 6 | Normal operation. | D |
| GND | 7 | Device will not be powered. | B |
| OE | 8 | I/Os may be High Impedance or active, unknown input state. | A |
| NC | 9 | Normal operation. | D |
| B4Y | 10 | Bx input pin will be grounded internally. Bx output pins will in HiZ if device is disabled. If device is enabled, it will be HIGH or LOW depending on the input. | D |
| B3Y | 11 | | D |
| B2Y | 12 | | D |
| B1Y | 13 | | D |
| VCCB | 14 | Device will not be powered. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| VCCA | 1 | A1 | Ax will be HIGH, if corresponding Bx is LOW, there will be potential damage to the device if the current is not limited. If corresponding Bx is HIGH, then nothing will occur, no damage. | B |
| A1 | 2 | A2 | Two inputs shorted together will not cause damage unless there is external bus contention that drives the input such that VIL < Input Voltage < VIH in which case excessive supply current to GND may cause damage. One output on VCCA supply is shorted to one input of VCCA supply. Based on the external bus driving this connection, potential high current can be expected if the VILA < Input Voltage A3 < VIHA or if A4Y output gets an undeterministic voltage forced on it in presence of a valid input. | B |
| A2 | 3 | A3 | | B |
| A3 | 4 | A4Y | | B |
| A4Y | 5 | NC | Normal operation. | D |
| NC | 6 | GND | Normal operation. | D |
| GND | 7 | OE | All I/Os will be fixed into high impedance (tri-state). | B |
| OE | 8 | NC | Normal operation. | D |
| NC | 9 | B4 | Normal operation. | D |
| B4 | 10 | B3Y | Two outputs shorted together may cause damage if there is external bus contention that drives one output low while driving the other output high. If both outputs are high or both outputs are low, then nothing will occur, no damage. One output on VCCB supply is shorted to one input of VCCB supply. Based on the external bus driving this connection, potential high current can be expected if the VILB < Input Voltage B4 < VIHA or if B3Y output gets an undeterministic voltage forced on it in presence of a valid input. | A |
| B3Y | 11 | B2Y | | A |
| B2Y | 12 | B1Y | | A |
| B1Y | 13 | VCCB | Bx will be HIGH, if corresponding Ax is LOW, there will be potential damage to the device if the current is not limited. If corresponding Ax is HIGH, then nothing will occur, no damage. | B |
| VCCB | 14 | VCCA | Device will not be powered or damaged, because short is external to device System level damage may occur in this scenario. | B |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply VCCA**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VCCA | 1 | Normal operation. | D |
| A1 | 2 | Ax will be HIGH, if corresponding Bx is LOW, there will be potential damage to the device if the current is not limited. If corresponding Bx is HIGH, then nothing will occur, no damage. | B |
| A2 | 3 | | B |
| A3 | 4 | | B |
| A4Y | 5 | | B |
| NC | 6 | Normal operation. | D |
| GND | 7 | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario. | B |
| OE | 8 | All I/Os will be active, device cannot be disabled. | B |
| NC | 9 | Normal operation. | D |
| B4 | 10 | Bx will be HIGH, if corresponding Ax is LOW, there will be potential damage to the device if the current is not limited. If corresponding Ax is HIGH, then nothing will occur, no damage. | B |
| B3Y | 11 | | B |
| B2Y | 12 | | B |
| B1Y | 13 | | B |
| VCCB | 14 | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario. | B |

**Table 4-6. Pin FMA for Device Pins Short-Circuited to supply VCCB**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VCCA | 1 | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario. | B |
| A1 | 2 | Ax will be HIGH, if corresponding Bx is LOW, there will be potential damage to the device if the current is not limited. If corresponding Bx is HIGH, then nothing will occur, no damage. | B |
| A2 | 3 | | B |
| A3 | 4 | | B |
| A4Y | 5 | | B |
| NC | 6 | Normal operation. | D |
| GND | 7 | Device will not be powered or damaged, because short is external to device. System level damage may occur in this scenario. | B |
| OE | 8 | All I/Os will be active, device cannot be disabled. | B |
| NC | 9 | Normal operation. | D |
| B4 | 10 | Bx will be HIGH, if corresponding Ax is LOW, there will be potential damage to the device if the current is not limited. If corresponding Ax is HIGH, then nothing will occur, no damage. | B |
| B3Y | 11 | | B |
| B2Y | 12 | | B |
| B1Y | 13 | | B |
| VCCB | 14 | Normal operation. | D |

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