Functional Safety Information

LMQ644xx-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LMQ644xx-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

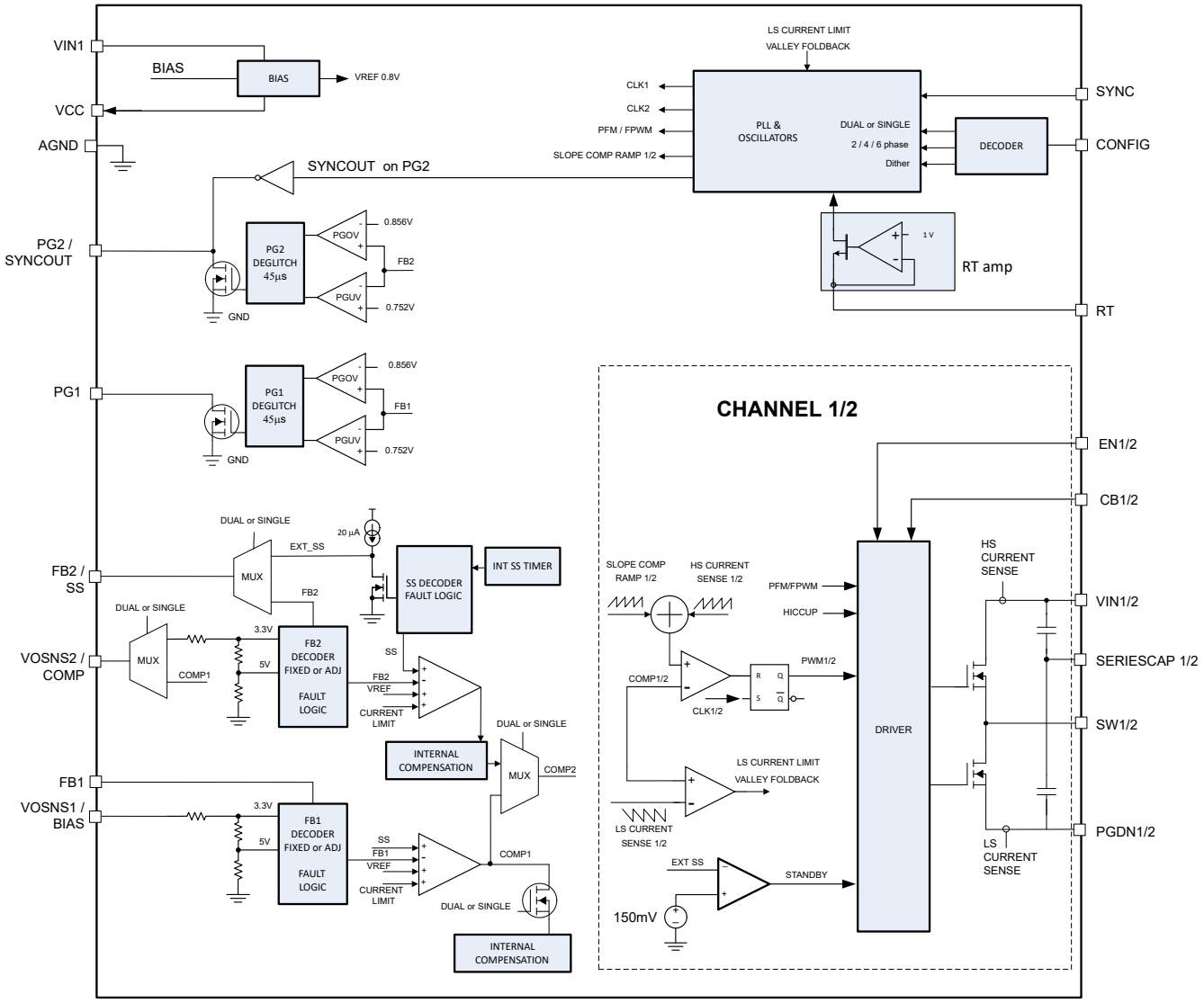

Figure 1-1. Functional Block Diagram

LMQ644xx-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LMQ644xx-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	17
Die FIT Rate	4
Package FIT Rate	13

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1250mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed = < 50-V supply	25	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMQ644xx-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW No output	50%
SW output not in specification - voltage or timing	40%
SW power FET stuck on	5%
PGOOD false trip, fails to trip	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LMQ644xx-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1, Figure 4-2, and Figure 4-3 show the LMQ644xx-Q1 pin diagrams. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMQ644xx-Q1 data sheet.

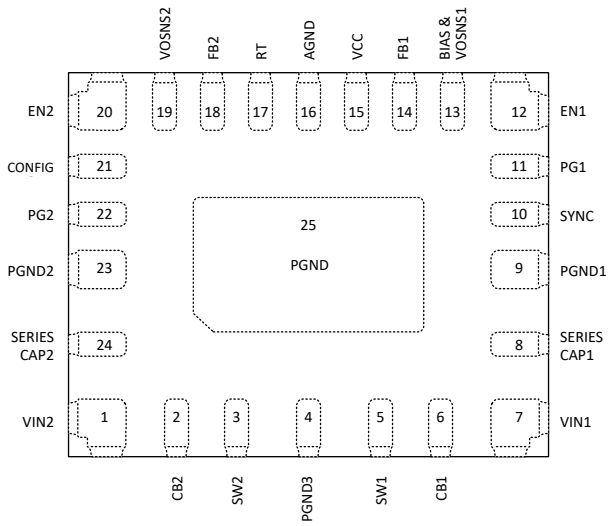

Figure 4-1. Dual Pin Diagram

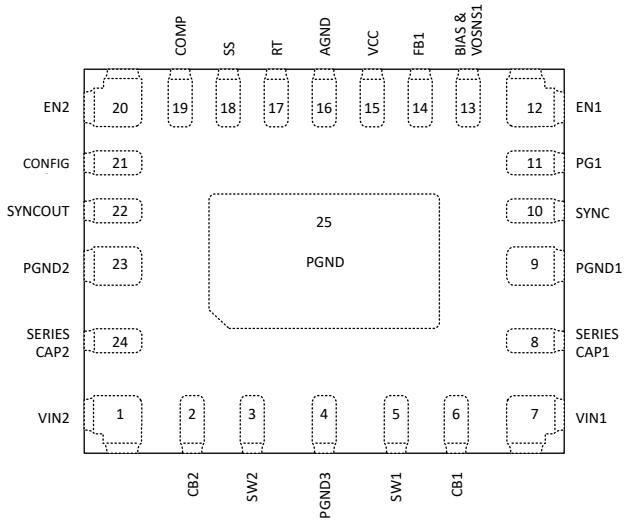

Figure 4-2. Single Primary Pin Diagram

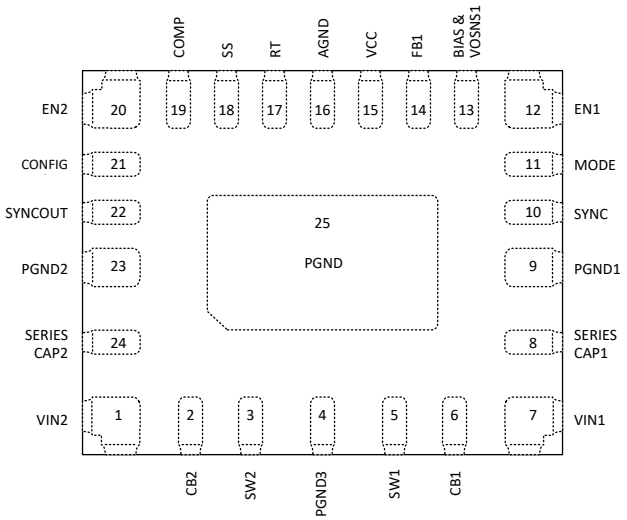

Figure 4-3. Single Secondary Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the LMQ644A2-Q1 data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
VIN2	1	VOUT = 0 V	B
CB2	2	VOUT = 0 V	B
SW2	3	Potential Damage to HS FET	A
PGND3	4	Normal Operation	D
SW1	5	Potential Damage to HS FET	A
CB1	6	VOUT = 0 V	B
VIN1	7	VOUT = 0 V	B
SERIES_CAP1	8	Series Capacitor is shorted internally. Device bypassing capacitance will increase as two series capacitors becomes single capacitor.	D
PGND1	9	Normal Operation	D
SYNC	10	Normal operation for PFM mode.	C
PG1	11	Loss of Power Good Flag	B
MODE	11	Normal operation for PFM mode.	C
EN1	12	Device is Disabled	C
BIAS/VOSNS1	13	VOUT1 = 0V short circuit	B
FB1	14	If configured as 3.3V fixed, normal operation. If configured for other Vout, then Vout1 will be out of specification and output 3.3V	B
VCC	15	Device is Disabled	B
AGND	16	Normal Operation	D
RT	17	VOUT = 0 V. No switching.	B
FB2	18	If configured as 3.3V fixed, normal operation. If configured for other Vout, then Vout2 will be out of specification and output 3.3V	B
SS	18	VOUT = 0 V	B
VOSNS2	19	VOUT2 = 0V if FB2=VCC or GND.	B/C
COMP	19	VOUT = 0 V	B
EN2	20	Second Channel is disabled	B
CONFIG	21	Device is Configured as Dual Output Voltage	B
PG2	22	Loss of Power Good Flag	B
SYNCOUT	22	If primary, secondary and tertiary devices will not switch. If secondary, tertiary device will not switch. If tertiary, no effect	B
PGND2	23	Normal Operation	D
SERIES_CAP2	24	Series Capacitor is shorted internally. Device bypassing capacitance will increase as two series capacitors becomes single capacitor.	D
PGND	25	Normal Operation	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
VIN2	1	VOUT2 = 0V	B
CB2	2	VOUT2 will collapse under load as FET gate voltage is not enough to fully enhance. Damage may occur if current is pulled from switch.	A
SW2	3	VOUT2 = 0V	B
PGND3	4	Normal Operation	D
SW1	5	VOUT1 = 0V	B
CB1	6	VOUT1 will collapse under load as FET gate voltage is not enough to fully enhance. Damage may occur if current is pulled from switch.	A
VIN1	7	VOUT1 = 0V	B
SERIES_CAP1	8	Normal Operation	D
PGND1	9	Normal Operation	D
SYNC	10	Device can toggle between PFM and PWM modes	C
PG1	11	Loss of Power Good Flag	B
MODE	11	Device can toggle between PFM and PWM modes	C
EN1	12	Loss of Disable Function	C
BIAS/VOSNS1	13	If in fixed output configuration, Vout >> than set point. If in adjustable Vout configuration, slight increase in input current.	B
FB1	14	Part configuration will be randomly selected between Fixed 5V or Adjustable.	B/C
VCC	15	Part can turn on and off as VCC uvlo is triggered.	B
AGND	16	Normal Operation	D
RT	17	VOUT = 0 V. No switching.	B
FB2	18	Part configuration will be randomly selected between Fixed 5V or Adjustable.	B/C
SS	18	Fast Soft Start	D
VOSNS2	19	If in fixed output configuration, Vout >> than set point.	B
COMP	19	Device can have oscillations on VOUT	B
EN2	20	Loss of Disable Function	C
CONFIG	21	VOUT = 0 V. No switching.	B
PG2	22	Loss of Power Good Flag	B
SYNCOUT	22	If primary, secondary and tertiary devices will not switch. If secondary, tertiary device will not switch. If tertiary, no effect	B
PGND2	23	Normal Operation	D
SERIES_CAP2	24	Normal Operation	D
PGND	25	Normal Operation	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
VIN2	1	Boot driver will be damaged	A
CB2	2	VOUT2 = 0	B
SW2	3	Potential Damage to HS FET	A
PGND3	4	Potential Damage to HS FET	A
SW1	5	VOUT1 = 0	B
CB1	6	Boot driver will be damaged	A
VIN1	7	Series Capacitor is shorted internally. Device bypassing capacitance will increase as two series capacitors becomes single capacitor.	D
SERIES_CAP1	8	Series Capacitor is shorted internally. Device bypassing capacitance will increase as two series capacitors becomes single capacitor.	D
PGND1	9	Normal operation for AUTO mode.	C
SYNC	10	For PG < 5.5V. Device will start in PFM and transition to PWM after start up. For PG > 5.5V damage may occur. For mode, part might enter PFWM of PWM mode based on SYNC logic	A
PG1	11	For EN < 20V. Device damage could occur if PG FET current limit is exceed. For EN > 20V, PGOOD FET can be damaged.	A
MODE	11	For EN < 20V. Normal Operation For EN > 20V, PGOOD FET can be damaged.	A
EN1	12	For EN < 5V. Output voltage out of range. For EN > 5V, device damge can occur if current is not limited	A
BIAS/VOSNS1	13	If configured as 3.3V fixed, normal operation. If configured for other Vout, then Vout1 will be out of specification and output 3.3V	B
FB1	14	If configured as 5V fixed, normal operation. If configured for other Vout, then Vout1 will be out of specification and output 5V	B
VCC	15	Vout1 = Vout 2 = 0V	B
AGND	16	VOUT = 0 V. No switching.	B
RT	17	Switching Frequency and output voltage will be incorrect.	B
FB2	18	If FB2 is grounded, Vout2 >> than set point. If FB2 is VCC then VCC will be pulled to 5V, no damage should occur. If FB2 is resistor divider the Vout will be 3.3Vout and see a load from the FB resistance to ground.	B
SS	18	Fast Soft Start	C
VOSNS2	19	VOUT2 >> than set point	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	19	EN > 5.5V. Damage of comparator if not current limited.	A
EN2	20	EN2 < 5.5V. Device is Configured as Dual Output Voltage. EN2 > 5.5 damge if not current limited	A
CONFIG	21	Device is Configured as Dual Output Voltage	B
PG2	22	Loss of Power Good Flag	B
SYNCOUT	22	If primary, secondary and tertiary devices will not switch. If secondary, tertiary device will not switch. If tertiary, no effect	B
PGND2	23	Normal Operation	D
SERIES_CAP2	24	Series Capacitor is shorted internally. Device bypassing capacitance will increase as two series capacitors becomes single capacitor.	D
PGND	25	Series Capacitor is shorted internally. Device bypassing capacitance will increase as two series capacitors becomes single capacitor.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
VIN2	1	Normal Operation	D
CB2	2	Boot driver will be damaged	A
SW2	3	Potential Damage to LS FET	A
PGND3	4	VOUT = 0 V	B
SW1	5	Potential Damage to LS FET	A
CB1	6	Boot driver will be damaged	A
VIN1	7	Normal Operation	D
SERIES_CAP1	8	Series Capacitor is shorted internally. Device bypassing capacitance will increase as two series capacitors becomes single capacitor.	D
PGND1	9	VOUT = 0 V	B
SYNC	10	Potential Damage for VIN > 5.5V	A
PG1	11	Loss of Power Good Flag. Potential Damage if not current limited	A
MODE	11	Normal operation for PWM mode. Potential Damage for VIN > 5.5V	A
EN1	12	Device is enabled	C
BIAS/VOSNS1	13	Potential damage from permanent short across converter	A
FB1	14	Potential Damage for VIN > 5.5V	A
VCC	15	Potential Damage for VIN > 5.5V	A
AGND	16	VOUT = 0 V	B
RT	17	Potential Damage for VIN > 5.5V	A
FB2	18	Potential Damage for VIN > 5.5V	A
SS	18	Potential Damage for VIN > 5.5V	A
VOSNS2	19	Potential Damage for VIN > 5.5V	A
COMP	19	Potential Damage for VIN > 5.5V	A
EN2	20	Second Channel is enabled	C
CONFIG	21	Potential Damage for VIN > 5.5V	A
PG2	22	Potential Damage for VIN > 20V or lower if not current limited	A
SYNCOUT	22	Potential Damage for VIN > 5.5V or lower if not current limited	A
PGND2	23	VOUT = 0 V	B
SERIES_CAP2	24	Series Capacitor is shorted internally. Device bypassing capacitance will increase as two series capacitors becomes single capacitor.	D
PGND	25	VOUT = 0 V	B

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