Functional Safety Information

TPS62874-Q1, TPS62875-Q1, TPS62876-Q1 and TPS62877-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview....2
2 Functional Safety Failure In Time (FIT) Rates....3
3 Failure Mode Distribution (FMD)....4
4 Pin Failure Mode Analysis (Pin FMA)....5

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1 Overview

This document contains information for the TPS62874-Q1, TPS62875-Q1, TPS62876-Q1 and TPS62877-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

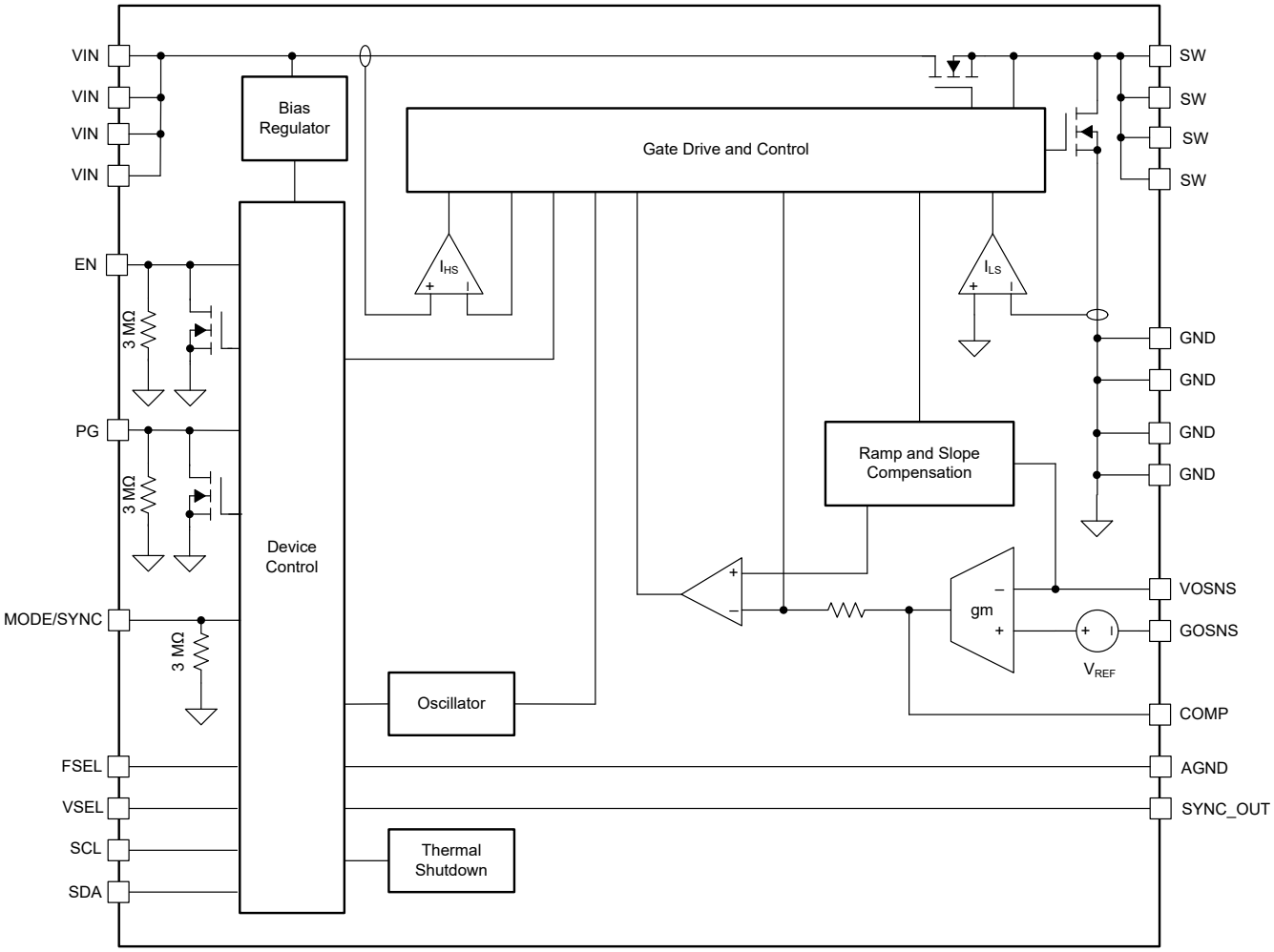

Figure 1-1. Functional Block Diagram

The TPS6287x-Q1 family was developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TPS6287x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)	
Output Current	15A	20A
Total Component FIT Rate	14	18
Die FIT Rate	5	8
Package FIT Rate	9	10

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor control from table 11
- Power dissipation:
  - 1196 mW (Ouput current 15A)
  - 1660 mW (Output current 20A)
- Climate type: World-wide table 8
- Package factor (lambda 3): table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The reference FIT rate and reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS6287x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	20%
SW output not in specification – voltage or timing	15%
SW power HS or LS FET stuck on	35%
EN or PG false trip or fails to trip	10%
Switching frequency or output voltage range not in spec	10%
No device communication	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS6287x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS6287x-Q1 pin diagram. For a detailed description of the device pins see the *Pin Configuration and Functions* section in the TPS6287x-Q1 data sheet.

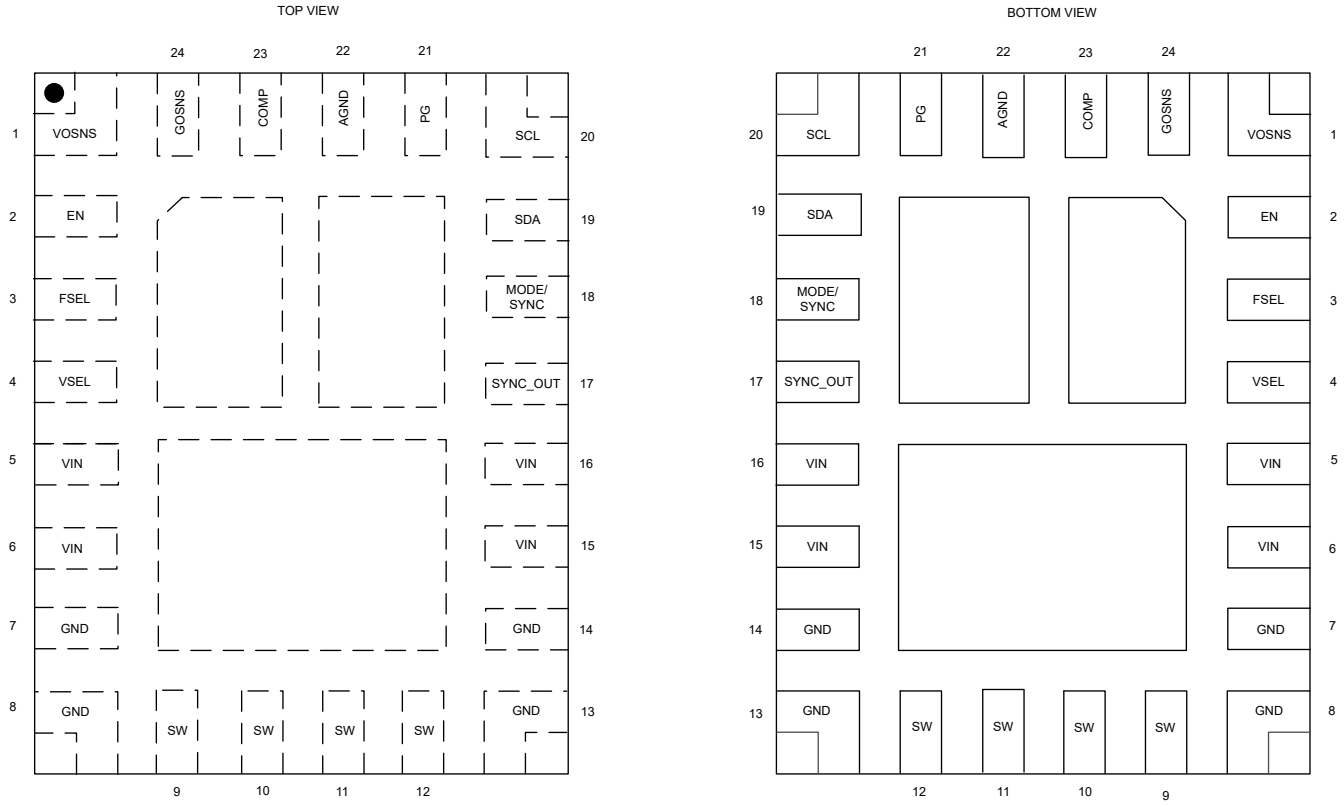

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Assumption the device is running in the typical application, see the *Simplified Schematic* on the first page in the *TPS6287x-Q1 2.7-V to 6-V Input, 15-A/ 20-A/ 25-A/ 30-A, Automotive, Stackable, Synchronous Step-Down Converters with Fast Transient Response* data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VOSNS	1	Maximum duty cycle operation and no regulated output voltage. Output voltage follows the input voltage.	B
EN	2	The device is disabled. Normal operation.	C
FSEL	3	Normal operation. Defines switching frequency.	C
VSEL	4	Normal operation. Defines start-up voltage.	C
VIN	5-6, 15-16	The device does not power up and there is no output voltage.	B
GND	7-8, 13-14	Normal operation.	D
SW	9-12	Potential device damage.	A
SYNC_OUT	17	Potential device damage.	A
MODE/SYNC	18	Normal operation. Power save mode is enabled.	C
SDA	19	Normal operation and no I^2C communication.	B
SCL	20	Normal operation and no I^2C communication.	B
PG	21	Normal operation and loss of PG indication.	B
AGND	22	Normal operation, but variations of the switching frequency may occur.	B
COMP	23	The device does not power up and there is no output voltage.	B
GOSNS	24	Normal operation, but output voltage accuracy decreases.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VOSNS	1	No output voltage regulation and can cause the output voltage to oscillate. Oscillation frequency cannot be predicted.	B
EN	2	Undetermined device operation. The device can power up and operate normal. Stays turned off.	B
FSEL	3	Normal operation. Switching frequency is undefined.	B
VSEL	4	Normal operation. Start-up voltage is undefined.	B
VIN	5-6, 15-16	Normal operation. Alternative VIN Pins are still connected.	C
GND	7-8, 13-14	Normal operation. Alternative GND Pins and the exposed thermal pad are still connected.	C
SW	9-12	No output voltage.	B
SYNC_OUT	17	Normal operation.	D
MODE/SYNC	18	Normal operation. Operation mode is undefined.	B
SDA	19	Normal operation and no I^2C communication.	B
SCL	20	Normal operation and no I^2C communication.	B
PG	21	Normal operation and loss of PG indication.	B
AGND	22	Undetermined device operation. Possible suharmonic oscillations	B
COMP	23	No loop compensation and can cause the output voltage to oscillate. Oscillation frequency cannot be predicted.	B
GOSNS	24	No output voltage regulation and can cause the output voltage to oscillate. Oscillation frequency cannot be predicted.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VOSNS	1	2	The device does not power up or there is potential device damage.	A
EN	2	3	Normal operation. Defines switching frequency	B
FSEL	3	4	Normal operation. Defines start-up voltage and switching frequency	B
VSEL	4	5	Normal operation. Defines start-up voltage.	C
VIN	5	6	Normal operation.	D
VIN	6	7	The device does not power up and there is no output voltage.	B
GND	7	8	Normal operation.	D
GND	8	9	Potential device damage.	A
SW	9	10	Normal operation.	D
SW	10	11	Normal operation.	D
SW	11	12	Normal operation.	D
SW	12	13	Potential device damage.	A
GND	13	14	Normal operation.	D
GND	14	15	The device does not power up and there is no output voltage.	B
VIN	15	16	Normal operation.	D
VIN	16	17	Potential device damage.	A
SYNC_OUT	17	18	Potential device damage.	A
MODE/SYNC	18	19	Potential device damage if MODE/SYNC is tied high. No I^2C communication.	A
SDA	19	20	Normal operation and no I^2C communication.	B
SCL	20	21	Loss of PG indication. No I^2C communication.	B
PG	21	22	Normal operation and loss of PG indication.	B
AGND	22	23	The device does not power up and there is no output voltage.	B
COMP	23	24	The device does not power up and there is no output voltage.	B
GOSNS	24	1	Maximum duty cycle operation and no regulated output voltage. Output voltage follows the input voltage.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VOSNS	1	The device does not start up. Output voltage stays low or potential device damage.	A
EN	2	Potential device damage.	A
FSEL	3	Normal operation. Defines switching frequency.	C
VSEL	4	Normal operation. Defines start-up voltage.	C
VIN	5-6, 15-16	Normal operation.	D
GND	7-8, 13-14	The device does not power up and there is no output voltage.	A
SW	9-12	Potential device damage.	A
SYNC_OUT	17	Potential device damage.	A
MODE/SYNC	18	Normal operation and forced PWM operation.	C
SDA	19	Potential device damage.	A
SCL	20	Potential device damage.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PG	21	Potential device damage.	A
AGND	22	Potential device damage.	A
COMP	23	Potential device damage.	A
GOSNS	24	Potential device damage.	A

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