Functional Safety Information

LM7481-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LM7481-Q1 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

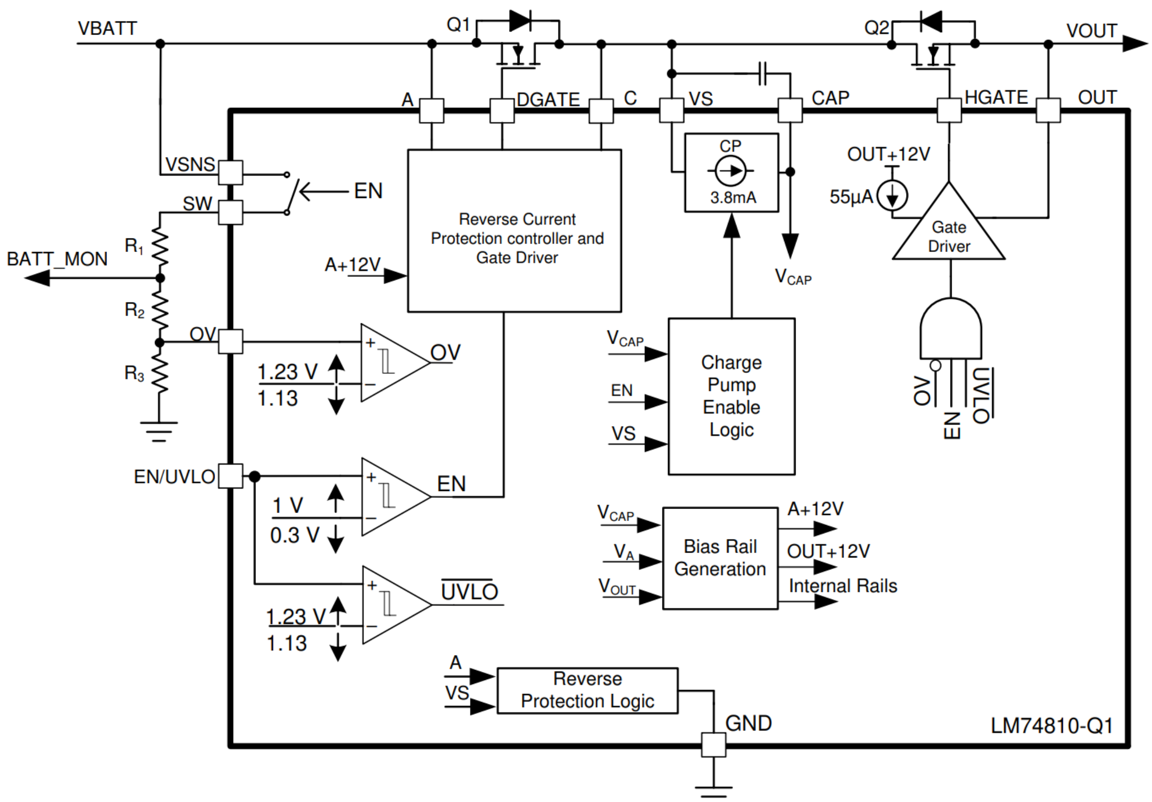

Figure 1-1. Functional Block Diagram

LM7481-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM7481-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 32.5mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM7481-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
DGATE output stuck at Low	30%
HGATE output stuck at Low	25%
DGATE output not in specification – voltage or timing	15%
HGATE output not in specification – voltage or timing	15%
DGATE output stuck at High	5%
HGATE output stuck at High	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM7481-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LM7481-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM7481-Q1 data sheet.

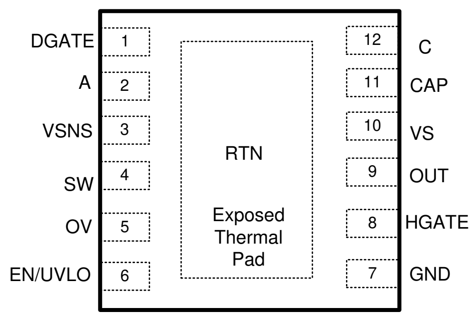

Figure 4-1. Pin Diagram

The pin FMA is provided under the assumption that the device is operating under the specified ranges within the Recommended Operating Conditions section of the data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DGATE	1	Device will damage due to internal conduction. External DGATE FET can also damage due to maximum VGS rating violation.	A
A	2	Input supply shorted to ground. Device will not be functional.	B
VSNS	3	Input supply monitoring feature will not be available.	B
SW	4	No device damage is expected if VSNS is floating. Device will get damaged if VSNS connected to A.	A
OV	5	Overvoltage protection functionality will be disabled.	B
EN/UVLO	6	Device will be in shutdown mode.	B
GND	7	No impact on the device functionality.	D
HGATE	8	HGATE gate drive will be off.	B
OUT	9	No device damage is expected. External FET VGS(max) rating can exceed and damage external FET.	D
VS	10	Device will not power up.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CAP	11	Device will damage due to internal conduction between VS and CAP.	A
C	12	Linear regulation and reverse current blocking functionality will not be available.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DGATE	1	External FET will be off as DGATE drive is open.	B
A	2	Device will not power up.	B
VSNS	3	Input supply monitoring feature will not be available.	B
SW	4	Input supply monitoring feature will not be available.	B
OV	5	Overvoltage functionality is not controlled, it can turn HGATE ON/OFF.	B
EN/UVLO	6	Device will be in shutdown mode due to internal pull-down on EN/UVLO pin.	B
GND	7	Device will not power up.	B
HGATE	8	External high side FET will be off as HGATE gate drive is open.	B
OUT	9	HGATE FET will not be able to turn off as OUT is floating.	B
VS	10	Device will not power up.	B
CAP	11	DGATE and HGATE would turn on and off as part enter CP UVLO cycle due to insufficient decoupling cap.	B
C	12	DGATE drive will be off.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
DGATE	1	A	DGATE FET is always off as external FET GATE to SOURCE is shorted.	B
A	2	VSNS	No impact on device functionality.	D
VSNS	3	SW	Input supply monitoring feature will always be available.	B
SW	4	OV	HGATE will turn off provided SW pin voltage is higher than overvoltage comparator threshold.	B
OV	5	EN/ UVLO	HGATE will be on/off based on EN/UVLO voltage level being lower/higher than overvoltage comparator threshold.	B
EN/UVLO	6	—	No impact on device operation.	D
GND	7	HGATE	HGATE will be pulled low and external FET will be off.	B
HGATE	8	OUT	External HGATE FET will be off as FET GATE to SOURCE is shorted.	B
OUT	9	VS	HGATE FET gets bypassed. Overvoltage protection and load disconnect functionality will not be available.	B
VS	10	CAP	Device will not power up.	B
CAP	11	C	Charge pump will not come up. DGATE and HGATE drives will be off.	B
C	12	—	No impact on device operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DGATE	1	DGATE FET is always off as external FET GATE to SOURCE is shorted.	B
A	2	No impact on device operation.	D
VSNS	3	No impact on device operation.	D
SW	4	Input supply monitoring feature will always be available.	B
OV	5	HGATE will be off due to overvoltage comparator input higher than overvoltage threshold.	B
EN/UVLO	6	Device will be always on. Undervoltage functionality will not be available.	B
GND	7	Input supply shorted to ground. Device will not power up.	B
HGATE	8	HGATE gate drive will be off and device quiescent current can increase	B
OUT	9	Input is shorted to output. Device functionality will not be available.	B
VS	10	DGATE FET is shorted. Reverse polarity and reverse current blocking feature is not available.	B
CAP	11	Charge pump will not power up. DGATE and HGATE drive will remain off.	B
C	12	Linear regulation and reverse current blocking functionality will not be available.	B

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