Functional Safety Information

AFE78201 and AFE88201 Functional Safety FIT Rate, FMD, and Pin FMA

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Trademarks

1 Overview

This document contains information for the AFE78201 and AFE88201 (QFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

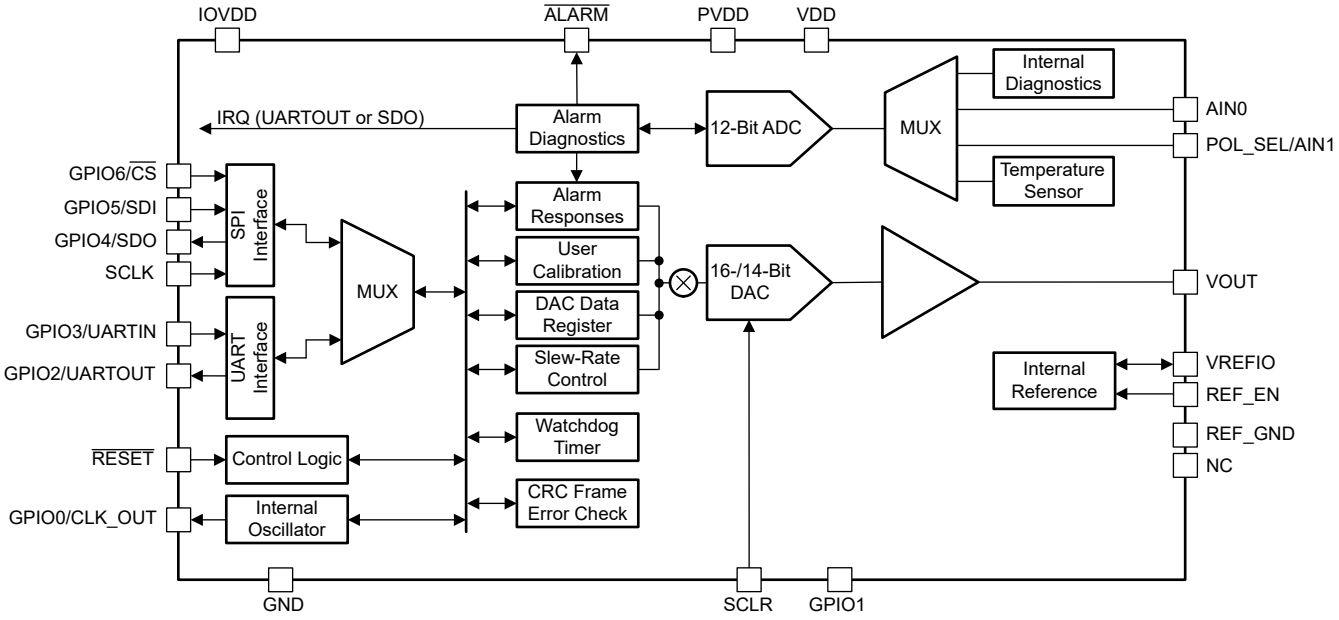

Figure 1-1. Functional Block Diagram

The AFE78201 and AFE88201 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the AFE78201 and AFE88201 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	2
Package FIT rate	11

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the AFE78201 and AFE88201 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
DAC output incorrect or not functional	44
Digital communication error	23
Diagnostic ADC measurement incorrect or not functional	20
Reset at power-on and internal supplies not functional	9
Internal oscillator not functional	4

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the AFE78201 and AFE88201. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the AFE78201 and AFE88201 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the AFE78201 and AFE88201 data sheet.

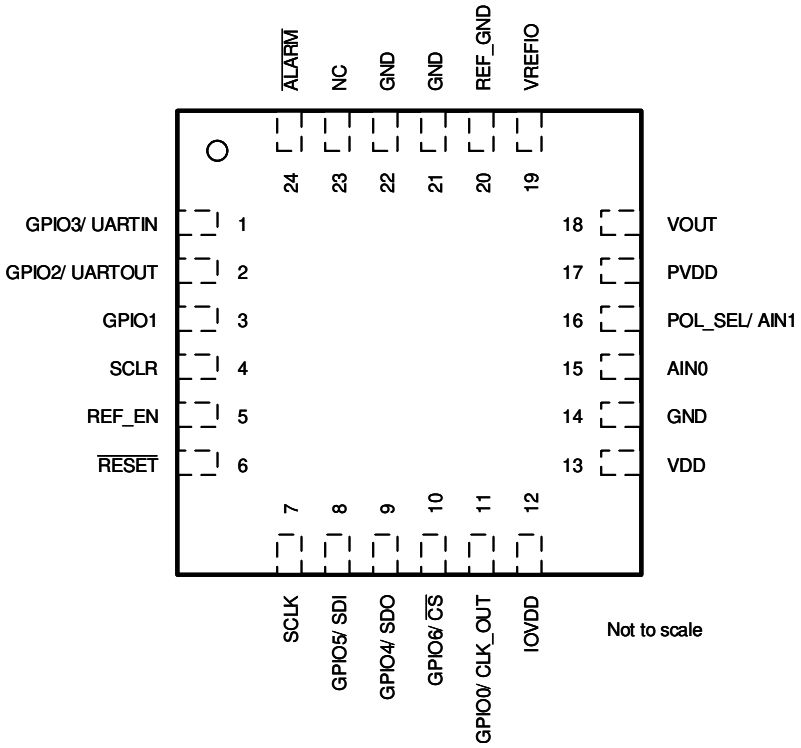

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- At least two SPI devices are present on the SPI bus.
- VDD and IOVDD use the same supply voltage.
- 'Short circuit to GND' means short to GND = REF_GND.
- 'Short circuit to Power' means short to PVDD = IOVDD = 3.3 V.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GPIO3/ UARTIN	1	GPIO3/UARTIN forced low. If configured as a UART input, no UART communication to the device is possible. SPI communication is possible. If configured as a GPIO input or as a GPIO pseudo open-drain output, GPIO is not functional.	B
		GPIO3/UARTIN forced low. If configured as a GPIO push-pull output, GPIO is not functional and is connected to ground for an extended period of time, an increase in supply current can be observed. Device damage is possible.	A
GPIO2/ UARTOUT	2	GPIO2/UARTOUT forced low. If configured as a GPIO input or as a GPIO pseudo open-drain output, GPIO is not functional.	B
		GPIO2/UARTOUT forced low. If configured as a UART output, no UART communication from the device is possible. SPI communication is possible. If configured as a GPIO push-pull output, GPIO is not functional. If pin is configured as a UART output or GPIO push-pull output, and is connected to ground for an extended period of time, an increase in supply current can be observed. Device damage is possible.	A
GPIO1	3	GPIO1 forced low. If configured as a GPIO input or as a GPIO pseudo open-drain output, GPIO is not functional.	B
		GPIO1 forced low. If pin is configured as a GPIO push-pull output, GPIO is not functional. If pin is connected to ground for an extended period of time, an increase in supply current can be observed. Device damage is possible.	A
SCLR	4	SCLR forced low. The device operates normally, but SCLR does not set the DAC output to the clear code value.	B
REF_EN	5	REF_EN forced low. The internal reference is not enabled, and the device does not have the proper output if the internal reference is used. The device operates normally if an external reference is used.	B
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ is forced low. The device is held in reset and does not function.	B
SCLK	7	SCLK forced low. No SPI communication with the device is possible. UART communication is possible.	B
GPIO5/SDI	8	GPIO5/SDI forced low. If configured for SPI, no SPI communication to the device is possible. UART communication is possible. If pin is configured as a GPIO input or as a GPIO pseudo open-drain output, GPIO is not functional.	B
		GPIO5/SDI forced low. If pin is configured as a GPIO push-pull output and is connected to ground for an extended period of time, an increase in supply current can be observed. Device damage is possible.	A
GPIO4/SDO	9	GPIO4/SDO forced low. If configured as a GPIO input or as a GPIO pseudo open-drain output, GPIO is not functional.	B
		GPIO4/SDO forced low. If configured for SPI, no SPI communication from the device is possible. UART communication is possible. If pin is configured as a GPIO push-pull output, GPIO is not functional. If pin is configured as a SPI output or GPIO push-pull output, and is connected to ground for an extended period of time, an increase in supply current can be observed. Device damage is possible.	A
GPIO6/$\overline{\text{CS}}$	10	GPIO6/$\overline{\text{CS}}$ forced low. If configured for SPI, no SPI communication to the device is possible. UART communication is possible. If pin is configured as a GPIO input or as a GPIO pseudo open-drain output, GPIO is not functional.	B
		GPIO6/$\overline{\text{CS}}$ forced low. If pin is configured as a GPIO push-pull output and is connected to ground for an extended period of time, an increase in supply current can be observed. Device damage is possible.	A
GPIO0/ CLK_OUT	11	GPIO0/CLK_OUT forced low. If internal oscillator is disabled, and GPIO is disabled, input appears as Hi-Z, and the device operates normally.	D
		GPIO0/CLK_OUT forced low. If pin is configured as a GPIO input or as a GPIO pseudo open-drain output, GPIO is not functional.	B
		GPIO0/CLK_OUT forced low. If pin is configured with internal oscillator enabled, oscillator output is grounded. If pin is configured as a GPIO push-pull output, GPIO is not functional. If pin is configured as a oscillator output or GPIO push-pull output, and is connected to ground for an extended period of time, an increase in supply current can be observed. Device damage is possible.	A
IOVDD	12	IOVDD supply grounded. The device is not powered and not functional. Verify that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
VDD	13	VDD supply grounded. The device is not functional. The internal LDO is shorted to ground. Shorting pin to ground can increase supply current. Device damage is possible if the pin is connected to ground for an extended period of time.	A
GND	14	No effect. Normal operation.	D
AIN0	15	AIN0 forced low. Conversion results for ADC0 are incorrect.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
POL_SEL/ AIN1	16	POL_SEL/AIN1 forced low; ADC SPECIAL_CFG.AIN1_ENB set to 1. Conversion results for AIN1 are incorrect.	B
		POL_SEL/AIN1 forced low; ADC SPECIAL_CFG.AIN1_ENB set to 0. POL_SEL can be set to the wrong polarity depending on the selected DAC VOUT alarm voltage (ALMV_POL).	B
PVDD	17	PVDD supply grounded. The device is not powered and not functional. Verify that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
VOUT	18	VOUT forced low. DAC output is shorted and not functional. Shorting the pin to ground can increase supply current.	B
VREFIO	19	VREFIO forced low; internal reference disabled, external reference connected. The DAC output is incorrect and not functional.	B
		VREFIO forced low; internal reference enabled. Shorting the pin to ground can increase supply current. Device damage is possible if the internal reference is enabled and VREFIO is connected to ground for an extended period of time.	A
REF_GND	20	No effect. Normal operation.	D
GND	21	No effect. Normal operation.	D
GND	22	No effect. Normal operation.	D
NC	23	NC pin forced low. Shorting the pin to ground can increase supply current. Device damage is possible if the pin is connected to ground for an extended period of time.	A
$\overline{\text{ALARM}}$	24	$\overline{\text{ALARM}}$ pin forced low. Alarm is not functional.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GPIO3/ UARTIN	1	GPIO3/UARTIN is undetermined. If configured as a UART input, no UART communication to the device is possible. SPI communication is possible. In other configurations, GPIO is not functional. Leaving the pin unconnected can increase supply current. Device damage is possible if the pin is unconnected for an extended period of time.	A
GPIO2/ UARTOUT	2	GPIO2/UARTOUT is undetermined. If configured as a UART output, no UART communication to the device is possible. SPI communication is possible.	B
		GPIO2/UARTOUT is undetermined. In other configurations, GPIO is not functional. Leaving the input pin unconnected can increase supply current. Device damage is possible if the pin is unconnected for an extended period of time.	A
GPIO1	3	GPIO1 is undetermined. GPIO is not functional. Leaving the input pin unconnected can increase supply current. Device damage is possible if the pin is unconnected for an extended period of time.	A
SCLR	4	SCLR is undetermined. Device functionality is undetermined. Output can be set to expected output or the DAC clear code.	B
REF_EN	5	REF_EN is undetermined; external reference not connected. Device functionality is undetermined. The reference can operate normally or be disabled.	B
		REF_EN is undetermined; external reference connected. Device damage is possible if an external reference drives VREFIO.	A
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ is undetermined. Device functionality is undetermined. The device can operate normally or be held in reset.	B
SCLK	7	SCLK is undetermined. No SPI communication with the device. UART communication is possible.	B
GPIO5/SDI	8	GPIO5/SDI is undetermined. If configured as an SPI input, no SPI communication to the device is possible. UART communication is possible. In other configurations, GPIO is not functional. Leaving the input pin unconnected can increase supply current. Device damage is possible if the pin is unconnected for an extended period of time.	A
GPIO4/SDO	9	GPIO4/SDO is undetermined. If configured as an SPI output, no SPI communication to the device is possible. UART communication is possible.	B
		GPIO4/SDO is undetermined. In other configurations, GPIO is not functional. Leaving the input pin unconnected can increase supply current. Device damage is possible if the pin is unconnected for an extended period of time.	A
GPIO6/$\overline{\text{CS}}$	10	GPIO6/$\overline{\text{CS}}$ is undetermined. If configured as an SPI input, no SPI communication to the device is possible. UART communication is possible. In other configurations, GPIO is not functional. Leaving the input pin unconnected can increase supply current. Device damage is possible if the pin is unconnected for an extended period of time.	A
GPIO0/ CLK_OUT	11	GPIO0/CLK_OUT unconnected. If configured with internal oscillator enabled, oscillator output is unconnected.	B
		GPIO0/CLK_OUT unconnected. In other configurations, GPIO is not functional. Leaving the input pin unconnected can increase supply current. If internal oscillator and GPIO is disabled, GPIO0/CLK_OUT is similarly unconnected. Device damage is possible if the pin is unconnected for an extended period of time.	A
IOVDD	12	IOVDD supply unconnected. The device is not powered and not functional if all external digital pins are held low. The device can power up through internal ESD diodes to IOVDD if voltages greater than the power-on reset threshold of the device are present on any of the digital pins. Device functionality is undetermined.	B
VDD	13	Output of LDO unconnected. Without connection to capacitor, output can oscillate and device functionality is undetermined.	B
GND	14	Device functionality is undetermined. The device can be unpowered or connected to ground internally to be powered.	B
AIN0	15	AIN0 is undetermined. The conversion results of ADC0 are undetermined.	B
POL_SEL/ AIN1	16	POL_SEL/AIN1 is undetermined. If ADC SPECIAL_CFG.AIN1_ENB set to 1, the conversion results of AIN1 are undetermined.	B
		POL_SEL/AIN1 is undetermined. If ADC SPECIAL_CFG.AIN1_ENB set to 0, the POL_SEL input is undetermined. POL_SEL can be set to the wrong polarity depending on the selected DAC VOUT alarm voltage (ALMV_POL).	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PVDD	17	PVDD supply unconnected. The device is not powered and not functional if all external pins are held low. The device can power up through internal ESD diodes to PVDD if voltages greater than the power-on reset threshold of the device are present on any of the digital pins. Device functionality is undetermined.	B
VOUT	18	VOUT unconnected. DAC output floating.	B
VREFIO	19	VREFIO unconnected. With internal reference enabled, output can oscillate without load capacitance.	B
		VREFIO unconnected. When using an external reference, the DAC reference is disconnected. The DAC output is incorrect.	B
REF_GND	20	REF_GND unconnected. The device reference does not set to proper voltage. The DAC output is incorrect.	B
GND	21	Pin unconnected. No effect. Normal operation.	D
GND	22	Pin unconnected. No effect. Normal operation.	D
NC	23	Pin unconnected. No effect. Normal operation.	D
$\overline{\text{ALARM}}$	24	$\overline{\text{ALARM}}$ unconnected. No $\overline{\text{ALARM}}$ communication back to controller.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GPIO3/ UARTIN	1	GPIO2/ UARTOUT	If configured for UART, no UART communication to the device is possible. SPI communication is possible. Device damage is possible from contention as the UARTIN driver tries to drive the UARTOUT pin. If pins are configured for GPIO, GPIO is not functional. If both pins are configured as GPIO inputs, or if both pins are configured as GPIO open drain outputs, then an increase in supply current can be seen. If either pin is configured as a GPIO push-pull output or an open drain output, an increase in supply or ground current can be observed when there is contention between the GPIO output pin and the other output pin or to the other GPIO input pin driver. Device damage is possible if connected for an extended period of time.	A
GPIO2/ UARTOUT	2	GPIO1	If configured for UART, no UART communication from the device is possible. SPI communication is possible. Device damage is possible from contention from GPIO2/ UARTOUT and GPIO1/CD pin outputs. If pins are configured for GPIO, GPIO is not functional. If both pins are configured as GPIO inputs, or if both pins are configured as GPIO open drain outputs, then an increase in supply current can be seen. If either pin is configured as a GPIO push-pull output or an open drain output, an increase in supply or ground current can be observed when there is contention between the GPIO output pin and the other output pin or to the other GPIO input pin driver. Device damage is possible if connected for an extended period of time.	A
GPIO1	3	SCLR	Contention between GPIO1 pin and SCLR pin. Device damage is possible from output pin contention if connected for an extended period of time. If GPIO1 pin is configured as a GPIO input, then an increase in supply current can be seen with contention between the SCLK pin and the SDI pin driver. If GPIO1 pin is configured as a GPIO push-pull output or an open drain output, an increase in supply or ground current can be observed when there is contention between the GPIO output pin and the RTS output pin.	A
SCLR	4	REF_EN	SCLR pin can be forced high if the REF_EN pin is high. DAC output can be forced to the clear code value. If REF_EN pin is low, the DAC operates normally, but the SCLR pin does not set the DAC to the clear code value.	B
REF_EN	5	$\overline{\text{RESET}}$	REF_EN undetermined; internal reference intended. The device operates normally with the $\overline{\text{RESET}}$ pin set high. Reference is disabled as $\overline{\text{RESET}}$ is set low.	B
			REF_EN undetermined; external reference connected. An external reference can damage the device if connected to VREFIO for an extended period of time.	A
$\overline{\text{RESET}}$	6	SCLK	SPI communication corrupted. No SPI communication with the device. UART communication is possible.	B
SCLK	7	GPIO5/SDI	If configured for SPI, SPI communication corrupted. No SPI communication with the device. UART communication is possible.	B
			If GPIO5/SDI pin is configured for GPIO, GPIO is not functional. If GPIO5/SDI pins is configured as a GPIO input, then an increase in supply current can be seen with contention between the SCLK pin and the SDI pin driver. If either pin is configured as a GPIO push-pull output or an open drain output, an increase in supply or ground current can be observed when there is contention between the GPIO output pin and the other output pin or to the other GPIO input pin driver.	A
GPIO5/SDI	8	GPIO4/SDO	If configured for SPI, SPI communication corrupted. No SPI communication with the device. UART communication is possible. Device damage is possible from contention from SDI input driver and SDO pin outputs. If pins are configured for GPIO, GPIO is not functional. If both pins are configured as GPIO inputs, or if both pins are configured as GPIO open drain outputs, then an increase in supply current can be seen. If either pin is configured as a GPIO push-pull output or an open drain output, an increase in supply or ground current can be observed when there is contention between the GPIO output pin and the other output pin or to the other GPIO input pin driver. Device damage is possible if connected for an extended period of time..	A
GPIO4/SDO	9	GPIO6/$\overline{\text{CS}}$	If configured for SPI, SPI communication corrupted. No SPI communication with the device. UART communication is possible. Device damage is possible from contention from SDO output and $\overline{\text{CS}}$ input driver. If pins are configured for GPIO, GPIO is not functional. If both pins are configured as GPIO inputs, or if both pins are configured as GPIO open drain outputs, then an increase in supply current can be seen. If either pin is configured as a GPIO push-pull output or an open drain output, an increase in supply or ground current can be observed when there is contention between the GPIO output pin and the other output pin or to the other GPIO input pin driver. Device damage is possible if connected for an extended period of time.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GPIO6/$\overline{CS}$	10	GPIO0/ CLK_OUT	If GPIO0 and CLK_OUT are both disabled, device functions normally.	D
			If GPIO0 is configured as an input, then there is contention between the GPIO0 driver and the $\overline{CS}$.	A
			If configured for SPI, SPI communication corrupted. No SPI communication with the device. UART communication is possible. GPIO and CLK_OUT are not functional. An increase in supply current can be observed if either pin is configured as an output to another output driver, or if both pins are configured as outputs. Device damage is possible if connected for an extended period of time. If pins are configured for GPIO, GPIO is not functional. If both pins are configured as GPIO inputs, or if both pins are configured as GPIO open drain outputs, then an increase in supply current can be seen. If either pin is configured as a GPIO push-pull output or an open drain output, an increase in supply or ground current can be observed when there is contention between the GPIO output pin and the other output pin or to the other GPIO input pin driver. Device damage is possible if connected for an extended period of time.	A
GPIO0/ CLK_OUT	11	IOVDD	If internal oscillator is disabled and GPIO0 is disabled as GPIO, GPIO0/CLK_OUT pin appears as Hi-Z, and the device operates normally	D
			If GPIO0/CLK_OUT is configured as a GPIO input, the GPIO is not functional.	B
			If GPIO0/CLK_OUT is configured with internal oscillator enabled, or if GPIO is configured as a GPIO output. An increase in ground current is observed when GPIO0/CLK_OUT pin tries to drive low against IOVDD. Device damage is possible if connected for an extended period of time.	A
IOVDD	12	VDD	The device can be damaged when VDD is driven to a voltage beyond 2.2V.	A
VDD	13	GND	The device is not functional. The internal LDO is shorted to ground. Shorting the pin to ground can increase supply current. Device damage is possible if the pin is connected to GND for an extended period of time.	A
GND	14	AIN0	AIN0 forced low. Conversion results for AIN0 are incorrect.	B
AIN0	15	POL_SEL/ AIN1	AIN0 and POL_SEL/AIN1 voltages undetermined; SPECIAL_CFG.AIN1_ENB set to 1. Either or both ADC conversion results for AIN0 and AIN1 can be incorrect.	B
			AIN0 and POL_SEL/AIN1 voltages undetermined; SPECIAL_CFG.AIN1_ENB is set to 0. POL_SEL can be set to the wrong polarity depending on the selected DAC VOUT alarm voltage (ALMV_POL).	B
POL_SEL/ AIN1	16	PVDD	POL_SEL/AIN1 forced high; SPECIAL_CFG.AIN1_ENB set to 1. Conversion results for AIN1 are incorrect.	B
			POL_SEL/AIN1 forced high; ADC SPECIAL_CFG.AIN1_ENB set to 0. POL_SEL can be set to the wrong polarity depending on the selected DAC VOUT alarm voltage (ALMV_POL).	B
PVDD	17	VOUT	VOUT shorted to PVDD. DAC output is shorted and not functional. Shorting the pin to PVDD can increase supply current. Device damage is possible if connected for an extended period of time.	A
VOUT	18	VREFIO	DAC reference voltage and DAC output voltage are undetermined, and the DAC is not functional. Shorting VOUT to VREFIO can increase supply current. Device damage is possible if connected for an extended period of time.	A
VREFIO	19	REF_GND	VREFIO forced low; external reference connected. The DAC output is incorrect and not functional.	B
			VREFIO forced low; internal reference enabled. The DAC output is incorrect and not functional. Shorting the pin to ground can increase the supply current. Device damage is possible if the internal reference is enabled and the pin is connected to GND for an extended period of time.	A
REF_GND	20	GND	No effect. Normal operation.	B
GND	21	GND	No effect. Normal operation.	B
GND	22	NC	NC pin forced low. Shorting the pin to ground can increase supply current. Device damage is possible if the pin is connected to GND for an extended period of time.	A
NC	23	$\overline{ALARM}$	NC pin forced low, increase in current is possible.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
$\overline{\text{ALARM}}$	24	GPIO3/ UARTIN	$\overline{\text{ALARM}}$ pin not functional and UART communication contention. SPI communication is possible. An increase in supply current can be observed if GPIO3/UARTIN pulls high and open-drain $\overline{\text{ALARM}}$ pulls low. Device damage is possible if connected for an extended period of time.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to PVDD and IOVDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GPIO3/ UARTIN	1	GPIO3/UARTIN forced high. If configured as a UART input, no UART communication to the device is possible. SPI communication is possible. If configured as a GPIO input, GPIO is not functional.	B
		GPIO3/UARTIN forced high. If configured as a GPIO push-pull or pseudo open-drain output, GPIO is not functional. If pin is configured as a GPIO output and is connected to PVDD and IOVDD for an extended period of time, an increase in ground current can be observed. Device damage is possible.	A
GPIO2/ UARTOUT	2	GPIO2/UARTOUT forced high. If configured for UART, no UART communication from the device is possible. SPI communication is possible. If configured as a GPIO push-pull or pseudo open-drain output, GPIO is not functional. If pin is configured as a UART output or GPIO output, and is connected to PVDD and IOVDD for an extended period of time, an increase in ground current can be observed. Device damage is possible.	A
		GPIO2/UARTOUT forced high. If configured as a GPIO input, GPIO is not functional.	B
GPIO1	3	GPIO1 pin forced high. If configured as a GPIO push-pull or pseudo open-drain output, GPIO is not functional. If pin is connected to PVDD and IOVDD for an extended period of time, an increase in ground current can be observed. Device damage is possible.	A
		GPIO1 forced high. If configured as a GPIO input, GPIO is not functional.	B
SCLR	4	SCLR pin forced high. SCLR sets the DAC output to the clear code value. The device is not functional.	B
REF_EN	5	REF_EN forced high. If the internal reference is selected, the device is in normal operation.	D
		REF_EN forced high. If external reference is connected, device damage is possible if external reference drives VREFIO.	A
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ is forced high. The device cannot be reset using the $\overline{\text{RESET}}$ pin, but operates normally.	B
SCLK	7	SCLK forced high. No SPI communication with the device. UART communication is possible.	B
GPIO5/SDI	8	GPIO5/SDI forced high. If configured for SPI, no SPI communication to the device is possible. UART communication is possible. If pin is configured as a GPIO input, GPIO is not functional.	B
		GPIO5/SDI forced high. If pin is configured as a GPIO push-pull or pseudo open-drain output and is connected to PVDD and IOVDD for an extended period of time, an increase in ground current can be observed. Device damage is possible.	A
GPIO4/SDO	9	GPIO4/SDO forced high. If configured for SPI, no SPI communication from the device is possible. UART communication is possible. If pin is configured as GPIO push-pull or pseudo open-drain output , GPIO is not functional. If pin is configured as a SPI output or GPIO output, and is connected to PVDD and IOVDD for an extended period of time, an increase in ground current can be observed. Device damage is possible.	A
		GPIO4/SDO forced high. If pin is configured as a GPIO input, GPIO is not functional.	B
GPIO6/$\overline{\text{CS}}$	10	GPIO6/$\overline{\text{CS}}$ forced low. If configured for SPI, no SPI communication to the device is possible. UART communication is possible. If pin is configured as a GPIO input, GPIO is not functional.	B
		GPIO6/$\overline{\text{CS}}$ forced low. If pin is configured as a GPIO push-pull or pseudo open-drain output and is connected to PVDD and IOVDD for an extended period of time, an increase in ground current can be observed. Device damage is possible.	A
GPIO0/ CLK_OUT	11	GPIO0/CLK_OUT forced high. If internal oscillator is disabled and GPIO is disabled, GPIO0/CLK_OUT input appears as Hi-Z, and the device operates normally.	D
		GPIO0/CLK_OUT forced high. If pin is configured as a GPIO input, GPIO is not functional.	B
		GPIO0/CLK_OUT forced high. If pin is configured with internal oscillator enabled, oscillator output is grounded. If pin is configured as a GPIO push-pull or pseudo open-drain output, GPIO is not functional. If pin is configured as a SPI output or GPIO output, and is connected to PVDD and IOVDD for an extended period of time, an increase in supply current can be observed. Device damage is possible.	A
IOVDD	12	For this case, IOVDD = PVDD = 3.3V. No effect. Normal operation.	D
VDD	13	VDD driven to supply. The device can be damaged when VDD is driven to a voltage beyond 2.2V.	A
GND	14	GND tied to supply. The device is not powered and not functional. The supply can draw excessive current. Verify that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
AIN0	15	AIN0 forced high. The conversion results for ADC0 are incorrect.	B
POL_SEL/ AIN1	16	POL_SEL/AIN1 forced high; SPECIAL_CFG.AIN1_ENB set to 1. The conversion results for AIN1 are incorrect.	B
		POL_SEL/AIN1 forced high; SPECIAL_CFG.AIN1_ENB set to 0. POL_SEL can be set to the wrong polarity depending on the selected DAC VOUT alarm voltage (ALMV_POL).	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to PVDD and IOVDD (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PVDD	17	No effect. Normal operation.	D
VOUT	18	VOUT shorted to supply. The DAC output is shorted and not functional. Shorting the pin to supply can increase the supply current.	B
VREFIO	19	VREFIO shorted to supply. The DAC output is not functional. Shorting the pin to supply can increase the supply current. Device damage is possible if the pin is connected to supply.	A
REF_GND	20	REF_GND shorted to supply. The DAC is not functional. The supply can draw excessive current. Verify that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
GND	21	GND shorted to supply. The DAC is not functional. The supply can draw excessive current. Device damage is possible if the pin is connected to supply.	A
GND	22	GND shorted to supply. The DAC is not functional. The supply can draw excessive current. Device damage is possible if the pin is connected to supply.	A
NC	23	NC pin shorted to supply. Device damage is possible if the pin is connected to supply.	A
$\overline{\text{ALARM}}$	24	$\overline{\text{ALARM}}$ pin forced high. The pin is not functional. Open-drain $\overline{\text{ALARM}}$ pin can be damaged during alarm if directly connected to PVDD.	A

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