Functional Safety Information

TPS785-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS785-Q1 (VSON and TO-252 packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the fixed version functional block diagram of the device for reference.

Figure 1-2 shows the adjustable version functional block diagram of the device for reference.

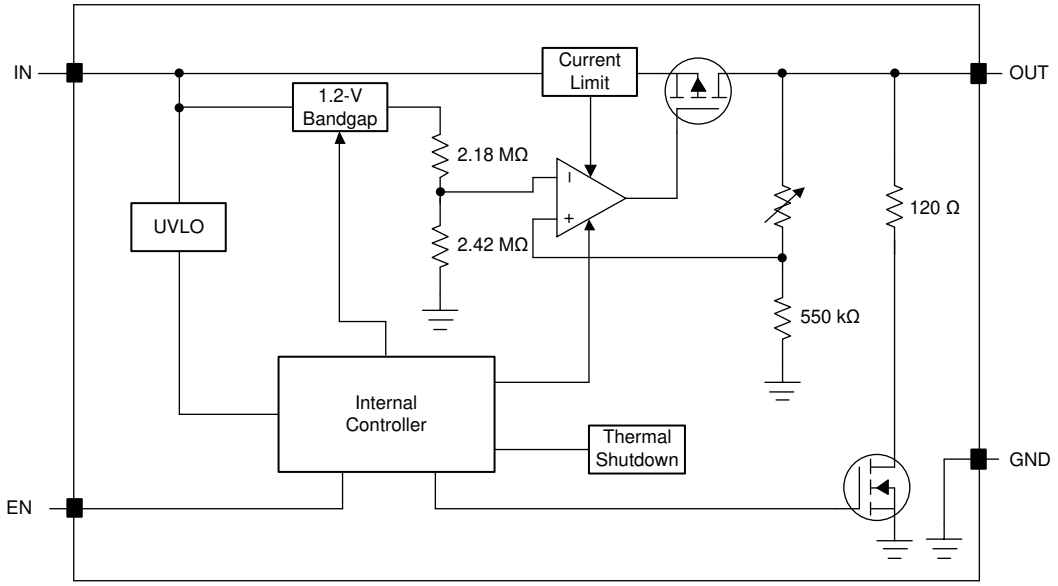

Figure 1-1. Fixed Version Functional Block Diagram

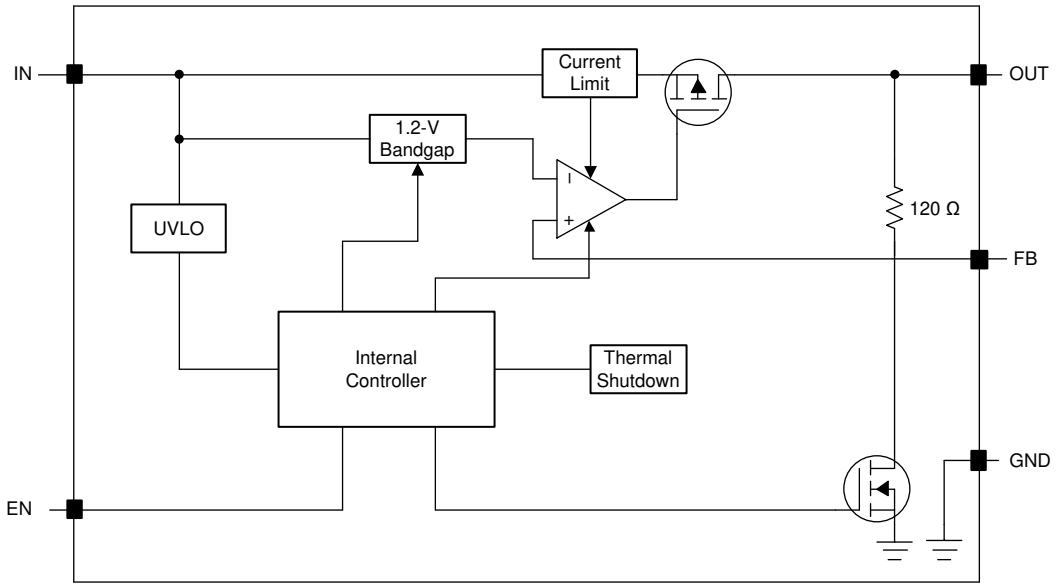

Figure 1-2. Adjustable Version Functional Block Diagram

The TPS785-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSON Package

This section provides functional safety failure in time (FIT) rates for the VSON package of the TPS785-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	19
Die FIT rate	14
Package FIT rate	5

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 2000mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 TO-252 Package

This section provides functional safety failure in time (FIT) rates for the TO-252 package of the TPS785-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	33
Die FIT rate	14
Package FIT rate	19

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 2500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS785-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
V_{OUT} high (following V_{IN})	60
V_{OUT} not in specification – voltage or timing	10
V_{OUT} low (no output)	20
Short circuit any two pins	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS785-Q1 (VSON and TO-252 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-10)
- Pin open-circuited (see Table 4-3 and Table 4-11)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-12)
- Pin short-circuited to supply (see Table 4-5 and Table 4-13)

Table 4-2 through Table 4-13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

4.1 VSON Package

Figure 4-1 shows the TPS785-Q1 pin diagram for the VSON package with a fixed output. Figure 4-2 shows the TPS785-Q1 pin diagram for the VSON package with an adjustable output. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS785-Q1 datasheet.

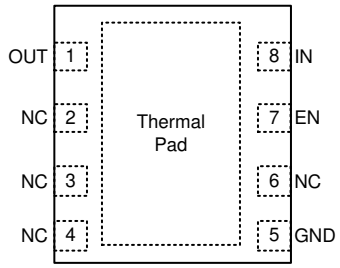

Figure 4-1. Pin Diagram (VSON Package), Fixed Version

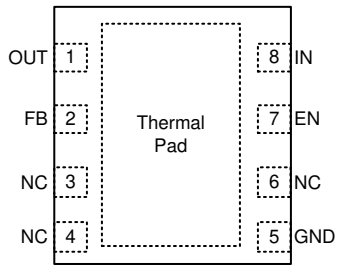

Figure 4-2. Pin Diagram (VSON Package), Adjustable Version

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device hits the current limit state. If power dissipation is significant, the device hits the thermal shutdown state. If the fault condition is not removed, the device can continue to cycle in and out of thermal shutdown. Continuously running the device above the rated current degrades the reliability of the device.	B
NC	2	NC Pin (Fixed Output): There is no impact to the device. The device operates as normal with improved thermal performance.	D
FB		FB Pin (Adjustable Output): The output voltage is not regulated. The device operates as a switch and V_{OUT} tracks V_{IN}.	B
NC	3	There is no impact to the device. The device operates as normal with improved thermal performance.	D
NC	4	There is no impact to the device. The device operates as normal with improved thermal performance.	D
GND	5	There is no impact to the device. The device operates as normal.	D
NC	6	NC Pin (Regular Version): There is no impact to the device. The device operates as normal with improved thermal performance.	D
EN	7	EN Pin (Regular Version): The device remains in a disabled state.	B
IN	8	The output voltage is not regulated and remains low at 0V.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output voltage is pulled to GND and the downstream devices do not receive power.	B
NC	2	NC Pin (Fixed Output): There is no impact to the device. The device operates as normal.	D
FB		FB Pin (Adjustable Output): The feedback loop is open, as a result, the output voltage is not regulated and remains in an indeterminate state. V_{OUT} is potentially pulled down to GND.	B
NC	3	There is no impact to the device. The device operates as normal.	D
NC	4	There is no impact to the device. The device operates as normal.	D
GND	5	With the reference pin floating, the voltages at the remaining pins are floating as well and the device is not functional. There is a risk of violating absolute maximum ratings.	B
NC	6	NC Pin (Regular Version): There is no impact to the device. The device operates as normal.	D
EN	7	EN Pin (Regular Version): The output voltage remains in an indeterminate state.	B
IN	8	There is no input to the LDO. The output voltage is not regulated.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC (pin 2)	(Fixed output.) There is no effect on the device. The device operates as normal.	D
		FB (pin 2)	(Adjustable output.) The output voltage is set to the internal reference voltage.	B
FB	2	NC (pin 3)	There is no effect on the device. The device operates as normal.	D
NC	3	NC (pin 4)	There is no effect on the device. The device operates as normal.	D
GND	5	NC (pin 6)	There is no effect on the device. The device operates as normal.	D
NC	6	EN (pin 7)	There is no effect on the device. The device operates as normal.	D
EN	7	IN (pin 8)	The device is always enabled. The peripherals connected to the EN pin are at risk of EOS.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device does not regulate.	B
NC	2	(Fixed output.) There is no effect on the device. The device operates as normal.	D
FB		(Adjustable output.) The absolute maximum rating for the FB pin (2V max) can be violated, resulting in the device being destroyed. If the absolute maximum rating is not violated, the error amplifier closes the channel and there is no output voltage.	A
NC	3	There is no effect on the device. The device operates as normal.	D
NC	4	There is no effect on the device. The device operates as normal.	D
GND	5	There is no output voltage. The performance of the system depends on upstream overcurrent protection.	B
NC	6	There is no effect on the device. The device operates as normal.	D
EN	7	The device is always enabled.	B
IN	8	There is no effect on the device. The device operates as normal.	D

4.2 VSON Package B Version

Figure 4-3 shows the TPS785-Q1 pin diagram for the VSON package (B Version) with a fixed output. Figure 4-4 shows the TPS785-Q1 pin diagram for the VSON package (B Version) with an adjustable output. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS785-Q1 datasheet.

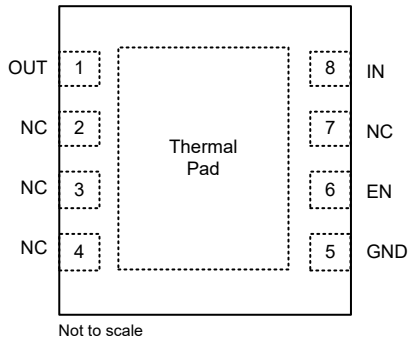

Figure 4-3. Pin Diagram (VSON Package), Fixed and B Version

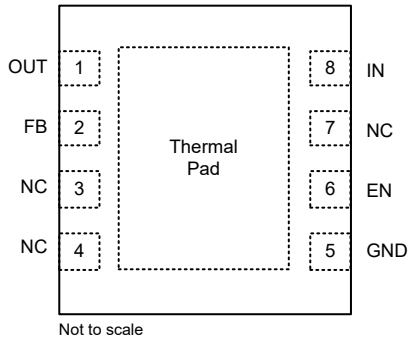

Figure 4-4. Pin Diagram (VSON Package), Adjustable and B Version

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
NC	2	(Fixed output.) There is no effect on the device. The device operates as normal.	D
FB		(Adjustable output.) The output voltage is input voltage minus dropout voltage because the error amplifier drives the pass transistor gate to the rail.	B
NC	3	There is no effect on the device. The device operates as normal.	D
NC	4	There is no effect on the device. The device operates as normal.	D
GND	5	There is no effect on the device. The device operates as normal.	D
EN	6	The device is disabled, resulting in no output voltage.	B
NC	7	There is no effect on the device. The device operates as normal.	D
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
NC	2	(Adjustable output.) There is no effect on the device. The device operates as normal.	D
FB		(Fixed output.) The error amplifier input is not connected. The output voltage is indeterminate.	B
NC	3	There is no effect on the device. The device operates as normal.	D
NC	4	There is no effect on the device. The device operates as normal.	D
GND	5	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
EN	6	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
NC	7	There is no effect on the device. The device operates as normal.	D
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC (pin 2)	(Fixed output.) There is no effect on the device. The device operates as normal. (Adjustable output.) The output voltage is set to the internal reference voltage.	D
		FB (pin 2)		B
NC/FB	2	NC (pin 3)	There is no effect on the device. The device operates as normal.	D
NC	3	NC (pin 4)	There is no effect on the device. The device operates as normal.	D
GND	5	EN (pin 6)	The device is always disabled, resulting in no output.	B
EN	6	NC (pin 7)	There is no effect on the device. The device operates as normal.	D
NC	7	IN (pin 8)	There is no effect on the device. The device operates as normal.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply (VIN)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device does not regulate. A violation of the absolute maximum rating of the downstream device is possible.	B
NC	2	(Fixed output.) There is no effect on the device. The device operates as normal.	D
FB		(Adjustable output.) The absolute maximum rating for the FB pin (2V max) can be violated, resulting in the device being destroyed. If the absolute maximum rating is not violated, the error amplifier closes the channel and there is no output voltage.	A
NC	3	There is no effect on the device. The device operates as normal.	D
NC	4	There is no effect on the device. The device operates as normal.	D
GND	5	There is no output voltage. Either the input supply is at 0V, or an input fuse is blown.	B
EN	6	The device is always enabled.	B
NC	7	There is no effect on the device. The device operates as normal.	D
IN	8	There is no effect on the device. The device operates as normal.	D

4.3 TO-252 Package

Figure 4-5 shows the TPS785-Q1 pin diagram for the TO-252 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS785-Q1 datasheet.

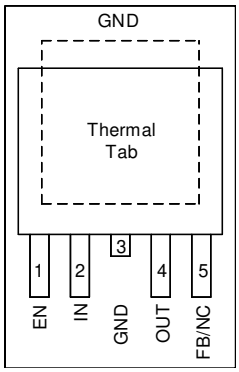

Figure 4-5. Pin Diagram (TO-252 Package)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	The device remains in the disabled state, providing no output voltage.	B
IN	2	There is no input to the LDO. The output voltage is not regulated.	B
GND	3	There is no impact to the device. The device operates as normal.	D
OUT	4	The device hits the current limit state. If power dissipation is significant, the device hits the thermal shutdown state. If the fault condition is not removed, the device continues to cycle in and out of thermal shutdown. Continuously running the device above the rated current degrades the reliability of the device.	B A
NC	5	NC Pin (Fixed Output): There is no impact to the device. The device operates as normal with improved thermal performance.	D
FB		FB Pin (Adjustable Output): The output voltage is not regulated. The device operates as a switch and V_{OUT} tracks V_{IN}.	B

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	The output voltage remains in an indeterminate state. V_{OUT} is likely pulled to GND.	B
IN	2	There is no input to the LDO. The output voltage is not regulated.	B
GND	3	With the reference pin floating, the voltages at the remaining pins are floating as well and the device is not functional. There is a risk of violating the absolute maximum ratings.	B
			A
OUT	4	The downstream devices do not receive power.	B
NC	5	NC Pin (Fixed Output): There is no impact to the device. The device operates as normal.	D
FB		FB Pin (Adjustable Output): The feedback loop is open, as a result, the output voltage is not regulated and remains in an indeterminate state.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN	1	IN	The device remains ON regardless of the enable signal value.	B
IN	2	GND	There is no input to the LDO. The output voltage is not regulated.	B
GND	3	OUT	The device hits current limit state. If power dissipation is significant, the device hits thermal shutdown state. If the fault condition is not removed, the device continues to cycle in and out of thermal shutdown. Continuously running the device above the rated current degrades the reliability of the device.	B
				A
OUT	4	NC	NC Pin (Fixed Output): There is no impact to the device. The device operates as normal.	D
		FB	FB Pin (Adjustable Output): The output voltage is held at 1.2V and does not regulate at target value.	B
NC	5	EN	NC Pin (Fixed Output): There is no impact to the device. The device operates as normal.	D/B/A
FB			FB Pin (Adjustable Output): The output voltage is not regulated at target value and for V_{EN} > 2V, this is an absolute maximum rating violation.	

Table 4-13. Pin FMA for Device Pins Short-Circuited to Supply (V_{IN})

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	The device remains ON regardless of the enable signal value.	B
IN	2	There is no impact to the device. The device operates as normal.	D
GND	3	The device does not turn ON. The output voltage stays low at 0V.	B
OUT	4	The output voltage is not regulated and equals V_{IN}. A violation of the absolute maximum ratings of the downstream device is possible.	B
NC	5	NC Pin (Fixed Output): There is no impact to the device. The device operates as normal.	D/B/A
FB		FB Pin (Adjustable Output): The output voltage is not regulated at the target value, and for V_{IN} > 2V, this is an absolute maximum rating violation.	

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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