Functional Safety Information

ISO6760L/ISO6760LN Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for ISO6760L and ISO6760LN (16-DW package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram of one channel of ISO6760L and ISO6760LN for reference.

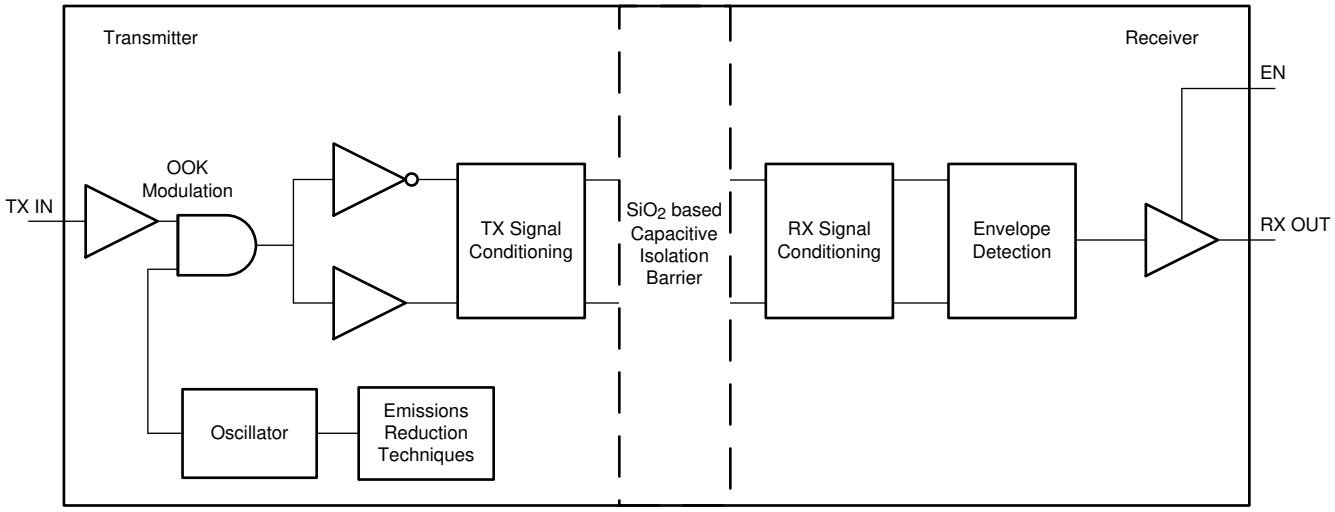

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Figure 1-1. Functional Block Diagram

ISO6760L and ISO6760LN was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 16-SOIC (wide-body SOIC) Package

This section provides Functional Safety Failure In Time (FIT) rates for the 16-SOIC package of ISO6760L and ISO6760LN based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	33
Die FIT Rate	2
Package FIT Rate	31

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 200 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55 °C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ISO6760L and ISO6760LN in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT state undetermined	35%
OUT not in timing or voltage specification	30%
OUT stuck to default state	25%
OUT stuck high	5%
OUT stuck low	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ISO6760L and ISO6760LN (16-DW package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (seeTable 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1. Note that when pin short to ground case is discussed, only same side ground shorts are considered.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 16-DW (wide-body SOIC) Package

Figure 4-1 shows the ISO6760L and ISO6760LN pin diagram for the 16-DW package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ISO6760L and ISO6760LN data sheet.

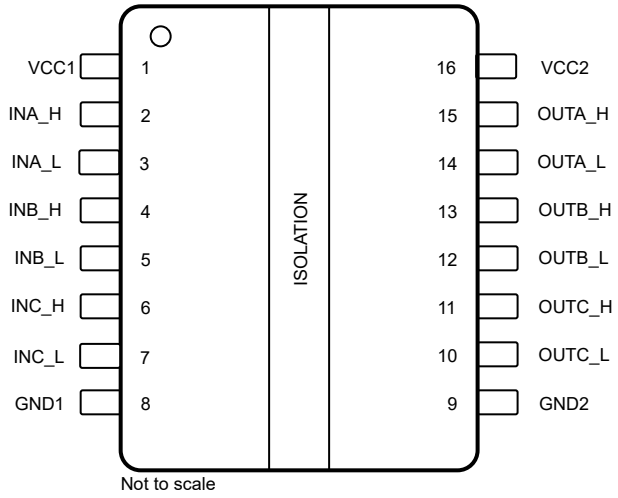

Figure 4-1. Pin Diagram

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	No power to the device on side-1. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage may be plausible.	A
INA_H	2	Input signal shorted to ground, so output (OUTA_H) stuck to low. Communication from INA_H to OUTA_H corrupted.	B
INA_L	3	Input signal shorted to ground, so output (OUTA_L) stuck to low. Communication from INA_L to OUTA_L corrupted.	B
INB_H	4	Input signal shorted to ground, so output (OUTB_H) stuck to low. Communication from INB_H to OUTB_H corrupted.	B
INB_L	5	Input signal shorted to ground, so output (OUTB_L) stuck to low. Communication from INB_L to OUTB_L corrupted.	B
INC_H	6	Input signal shorted to ground, so output (OUTC_H) stuck to low. Communication from INC_H to OUTC_H corrupted.	B
INC_L	7	Input signal shorted to ground, so output (OUTC_L) stuck to low. Communication from INC_L to OUTC_L corrupted.	B
GND1	8	Device continues to function as expected. Normal operation.	D
GND2	9	Device continues to function as expected. Normal operation.	D
OUTC_L	10	OUTC_L stuck low. Data communication from INC_L to OUTC_L lost. Device damage possible if INC_L is driven high for extended period of time.	A
OUTC_H	11	OUTC_H stuck low. Data communication from INC_H to OUTC_H lost. Device damage possible if INC_H is driven high for extended period of time.	A
OUTB_L	12	OUTB_L stuck low. Data communication from INB_L to OUTB_L lost. Device damage possible if INB_L is driven high for extended period of time.	A
OUTB_H	13	OUTB_H stuck low. Data communication from INB_H to OUTB_H lost. Device damage possible if INB_H is driven high for extended period of time.	A
OUTA_L	14	OUTA_L stuck low. Data communication from INA_L to OUTA_L lost. Device damage possible if INA_L is driven high for extended period of time.	A
OUTA_H	15	OUTA_H stuck low. Data communication from INA_H to OUTA_H lost. Device damage possible if INA_H is driven high for extended period of time.	A
V_{CC2}	16	No power to the device on side-2. OUTA/OUTB/OUTC pins state undetermined.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	Operation undetermined. Either device is unpowered and OUTA/OUTB/OUTC=default logic state. Device can power up if any IN is driven to logic high. If IN has current sourcing capability to provide regular operating current of device, ESD diode conducts that current and device damage plausible.	A
INA_H	2	No communication to INA channel possible. OUTA stuck to default state (Low)	B
INA_L	3	No communication to INA channel possible. OUTA stuck to default state (Low)	B
INB_H	4	No communication to INB channel possible. OUTB stuck to default state (Low).	B
INB_L	5	No communication to INB channel possible. OUTC stuck to default state (Low).	B
INC_H	6	No communication to INC channel possible. OUTC stuck to default state (Low).	B
INC_L	7	No communication to INC channel possible. OUTC stuck to default state (Low).	B
GND1	8	No current return ground path on side1. Device unpowered on side1.	B
GND2	9	No current return ground path on side2. Device unpowered on side2.	B
OUTC_L	10	State of OUTC_L undetermined. Data communication from INC_L to OUTC_L lost.	B
OUTC_H	11	State of OUTC_H undetermined. Data communication from INC_H to OUTC_H lost.	B
OUTB_L	12	State of OUTB_L undetermined. Data communication from INB_L to OUTB_L lost.	B
OUTB_H	13	State of OUTB_H undetermined. Data communication from INB_H to OUTB_H lost.	B
OUTA_L	14	State of OUTA_L undetermined. Data communication from INA_L to OUTA_L lost.	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUTA_H	15	State of OUTA_H undetermined. Data communication from INA_H to OUTA_H lost.	B
V_{CC2}	16	Device unpowered on side-2 and state of OUTA/OUTB/OUTC undetermined.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	INA_H	No power to the device on side-1. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage may be plausible.	A
INA_H	2	INA_L	Channel Pairing INA inputs shorted together, so outputs (OUTA) stay to low. Communication from INA to OUTA corrupted.	B
INA_L	3	INB_H	Communication corrupted for either INA_L or INB_H channel.	B
INB_H	4	INB_L	Channel Pairing INB inputs shorted together, so outputs (OUTB) stay low. Communication from INB to OUTB corrupted.	B
INB_L	5	INC_H	Communication corrupted for either INB_L or INC_H channel.	B
INC_H	6	INC_L	Channel Pairing INC inputs shorted together, so outputs (OUTC) stay low. Communication from INC to OUTC corrupted.	A
INC_L	7	GND1	INC_L shorted to ground, so OUTC_L stuck to low.	B
GND1	8	INC_L	Already considered in above row.	B
GND2	9	OUTC_L	OUTC_L stuck low. Data communication from INC_L to OUTC_L lost. Device damage possible if INC_L is set to cause OUTC_L to high for extended period of time.	A
OUTC_L	10	OUTC_H	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTC_H	11	OUTB_L	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTB_L	12	OUTB_H	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTB_H	13	OUTA_L	CCommunication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTA_L	14	OUTA_H	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTA_H	15	V_{CC2}	OUTA_H stuck to high. Device damage possible if INA_H is set to cause OUTA_H to low for extended period of time.	A
V_{CC2}	16	OUTA_H	Already considered in above row.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	No effect. Normal operation.	D
INA_H	2	INA_H pin stuck high. Communication corrupted. OUTA_H state high and OUTA_L state low.	B
INA_L	3	INA_L pin stuck high. Communication corrupted. OUTA_L state high and OUTA_H state low.	B
INB_H	4	INB_H pin stuck high. Communication corrupted. OUTB_H state high and OUTB_L state low.	B
INB_L	5	INB_L pin stuck high. Communication corrupted. OUTB_L state high and OUTB_H state low.	B
INC_H	6	INC_H pin stuck high. Communication corrupted. OUTC_H state high and OUTC_L state low.	B
INC_L	7	INB_L pin stuck high. Communication corrupted. OUTB_L state high and OUTB_H state low.	B
GND1	8	VCC1 shorted to GND1. Potential device damage.	A

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Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND2	9	VCC2 shorted to GND2. Potential device damage.	A
OUTC_L	10	OUTC_L stuck high. Communication disrupted. If INC_L is set to cause OUTC_L to low, OUTC_L being stuck high creates a short and can damage the device.	A
OUTC_H	11	OUTC_H stuck high. Communication disrupted. If INC_H is set to cause OUTC_H to low, OUTC_H being stuck high creates a short and can damage the device.	A
OUTB_L	12	OUTB_L stuck high. Communication disrupted. If INB_L is set to cause OUTB_L to low, OUTB_L being stuck high creates a short and can damage the device.	A
OUTB_H	13	OUTB_H stuck high. Communication disrupted. If INB_H is set to cause OUTB_H to low, OUTB_H being stuck high creates a short and can damage the device.	A
OUTA_L	14	OUTA_L stuck high. Communication disrupted. If INA_L is set to cause OUTA_L to low, OUTA_L being stuck high creates a short and can damage the device.	A
OUTA_H	15	OUTA_H stuck high. Communication disrupted. If INA_H is set to cause OUTA_H to low, OUTA_H being stuck high creates a short and can damage the device.	A
V_{CC2}	16	Device continues to function as expected. Normal operation.	D

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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