Functional Safety Information

LM5141-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LM5141-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

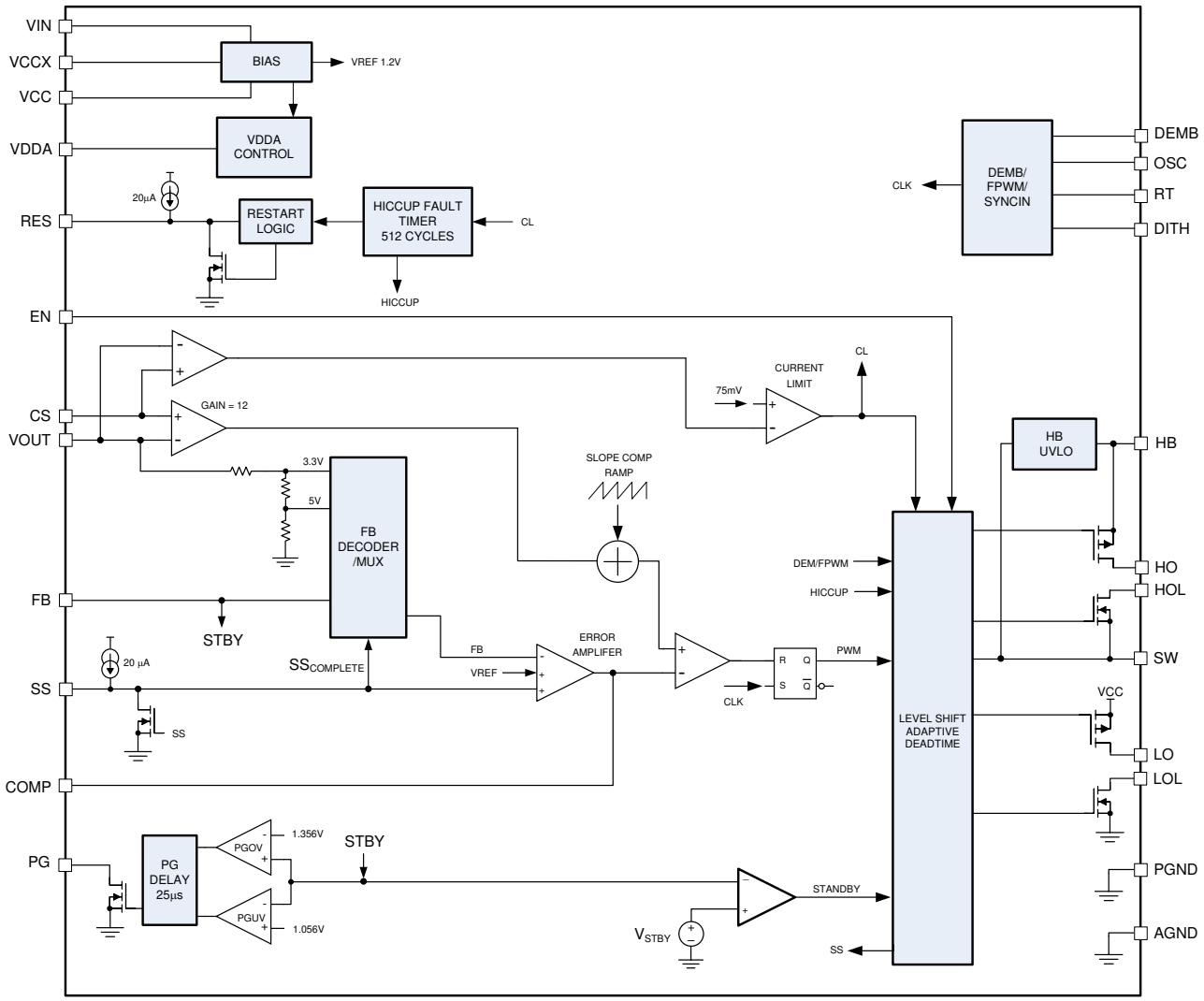

Figure 1-1. Functional Block Diagram

LM5141-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM5141-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	15
Die FIT Rate	4
Package FIT Rate	11

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 750 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed > 50V supply	32 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM5141-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	60%
Output not in specification – voltage or timing	25%
Gate driver stuck on	5%
PG false trip or fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM5141-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuit to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LM5141-Q1 pin diagram. For a detailed description of the device pins, please refer to the *Pin Configuration and Functions* section in the LM5141-Q1 data sheet.

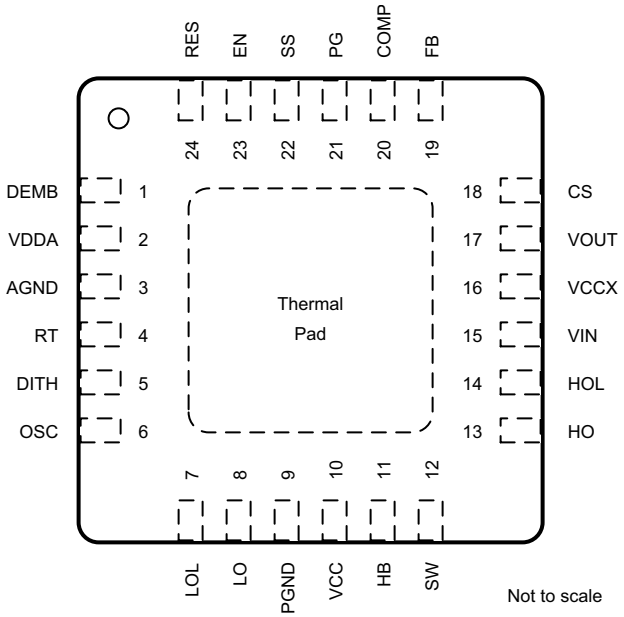

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit as per LM5141-Q1 data sheet is used
- PG is pulled up to VOUT

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DEMB	1	V_{OUT} = expected, DEMB mode only, and no synchronization is available.	C
		If DEMB = VDDA, V_{OUT} = 0 V. Loaded VCC output	B
VDDA	2	V_{OUT} = 0 V. No switching. Loaded VCC output	B
AGND	3	AGND is GND. V_{OUT} = expected	D
RT	4	Normal operation. V_{OUT} = expected. F_{SW} defaults to 2.2 MHz or 440 kHz, depending on OSC.	C
DITH	5	Dither disabled. V_{OUT} = expected	C
OSC	6	If OSC = GND, then F_{SW} = 440 kHz. V_{OUT} = expected	C
		If OSC = VDDA, then V_{OUT} = 0 V. Loaded VCC output	
LOL	7	V_{OUT} = 0 V. The VCC regulator is loaded to current limit.	B
LO	8	V_{OUT} = 0 V. The VCC regulator is loaded to current limit.	B
PGND	9	PGND is GND. V_{OUT} = expected	D
VCC	10	V_{OUT} = 0 V. The VCC regulator is loaded to current limit.	B
HB	11	V_{OUT} = 0 V. The VCC regulator is loaded to current limit.	B
SW	12	V_{OUT} = 0 V. Excessive current from VIN	B
HO	13	V_{OUT} = 0 V. High-side MOSFET cannot be turned on.	B
HOL	14	V_{OUT} = 0 V. High-side MOSFET cannot be turned on.	B
VIN	15	V_{OUT} = 0 V	B
VCCX	16	V_{OUT} = expected. The internal VCC regulator provides bias voltage.	C
VOUT	17	V_{OUT} = 0 V. Current limit reached and hiccup mode occurs.	B
CS	18	V_{OUT} = 0 V	B
FB	19	If FB = VDDA, then V_{OUT} = 0 V.	D
		If FB = GND, then V_{OUT} = 5 V.	B
COMP	20	V_{OUT} = 0 V	B
PG	21	V_{PG} = 0 V. V_{OUT} = expected	C
SS	22	V_{OUT} = 0 V	C
EN	23	V_{OUT} = 0 V. The LM5141-Q1 is disabled and enters shutdown.	C
RES	24	V_{OUT} = expected. The LM5141-Q1 cannot exit hiccup mode.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DEMB	1	Diode emulation/FPWM mode undefined. V_{OUT} = expected, erratic switching	C
VDDA	2	V_{OUT} = 0 V. Poor noise immunity	C
AGND	3	V_{OUT} = 0 V	B
RT	4	Normal operation. Frequency modulation feature is disabled. V_{OUT} = expected	C
DITH	5	V_{OUT} = expected	C
OSC	6	F_{SW} 440 kHz or 2.2 MHz. V_{OUT} = expected	C
LOL	7	V_{OUT} = 0 V. No discharge path for low-side MOSFET gate	B
LO	8	V_{OUT} = expected. Lower efficiency	C
PGND	9	V_{OUT} = 0 V. Uncontrolled behavior because of floating ground	B
VCC	10	V_{OUT} = 0 V	B
HB	11	V_{OUT} = 0 V. High-side gate drive floating	B
SW	12	V_{OUT} = VIN. High-side FET control floating	B
HO	13	V_{OUT} = 0 V. Will not regulate	B
HOL	14	V_{OUT} = VIN. Will not regulate. Excessive current from VIN	B
VIN	15	V_{OUT} = 0 V	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCX	16	V_{OUT} = expected	D
VOUT	17	V_{OUT} = oscillation. Will not regulate	B
CS	18	V_{OUT} = oscillation. No overcurrent or current sense information for current mode control.	B
FB	19	V_{OUT} will not regulate. The controller will be configured for adjustable output.	B
COMP	20	V_{OUT} = oscillation. Will not regulate	B
PG	21	V_{OUT} = expected. No PG information	C
SS	22	V_{OUT} = expected	D
EN	23	V_{OUT} = 0 V	B
RES	24	V_{OUT} = expected. Will exit hiccup mode quickly because low parasitic capacitor value.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effect(s)	Failure Effect Class
DEMB	1	VDDA	V_{OUT} = regulation, normal operation, and FPWM mode is enabled.	C
VDDA	2	AGND	V_{OUT} = 0 V	B
AGND	3	RT	V_{OUT} = regulation. Frequency modulation is disabled.	C
RT	4	DITH	V_{OUT} = regulation. Frequency modulation is disabled.	C
DITH	5	OSC	V_{OUT} = regulation. F_{SW} = 440 kHz	C
OSC	6	LOL	V_{OUT} = unregulated	B
LOL	7	LO	V_{OUT} = expected	C
LO	8	PGND	V_{OUT} = 0 V	B
PGND	9	VCC	V_{OUT} = 0 V	B
VCC	10	HB	V_{OUT} = 0 V	B
HB	11	SW	V_{OUT} = 0 V. The VCC regulator is in current limit.	B
SW	12	HO	V_{OUT} = 0 V	B
HO	13	HOL	V_{OUT} = expected	B
HOL	14	VIN	V_{OUT} = 0 V	A
VIN	15	VCCX	If V_{VIN} > 6.5 V, then V_{OUT} = 0 V. Exceeds the VCCX absolute maximum ratings	A
VCCX	16	VOUT	V_{OUT} = expected	D
			If V_{OUT} is > 6.5 V, then it exceeds the VCCX absolute maximum rating.	A
VOUT	17	CS	V_{OUT} cannot regulate, current limit is disabled, and there is no current sense information.	B
CS	18	FB	If FB = VDDA, then V_{OUT} = 3.3 V.	B
			If FB = GND, then V_{OUT} = 0 V. Excessive current from VIN	B
FB	19	COMP	If FB = VDDA, then V_{OUT} = VIN.	A
			If FB = GND, then V_{OUT} = 0 V.	B
COMP	20	PG	V_{OUT} = 0 V	B
PG	21	SS	V_{OUT} = 0 V	B
SS	22	EN	If V_{EN} > 6.5 V, then it will exceed the absolute maximum rating of the SS pin. V_{OUT} = 0 V	A
EN	23	RES	If V_{EN} > 6.5 V, then it will exceed the absolute maximum rating of the SS pin. V_{OUT} = 0 V	A
RES	24	DEMB	If DEMB = GND, V_{OUT} = regulation, then it will not restart if current limit is reached.	B
			If DEMB = VDDA, then V_{OUT} = regulation. No hiccup mode	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DEMB	1	If DEMB = GND, then V_{OUT} = 0 V. Excessive current for VIN	B
		If DEMB = VDDA and V_{VIN} < 6.5 V, then V_{OUT} = expected and there is erratic switching.	B
		If V_{VIN} > 6.5 V and exceeds the maximum rating of the DEMP pin, the device is damaged.	A
VDDA	2	If V_{VIN} > 6.5 V, V_{OUT} = 0 V, and exceeds the maximum rating of the VDDA pin, the device is damaged.	A
		If V_{VIN} < 6.5 V, then V_{OUT} = expected.	D
AGND	3	High VIN current. V_{OUT} = 0 V	B
RT	4	If V_{VIN} < 6.5 V, then V_{OUT} = 0 V.	B
		If V_{VIN} > 6.5 V and exceeds the maximum ratings, then the device is damaged.	A
DITH	5	If V_{VIN} > 6.5 V, the device is damaged.	A
		If V_{VIN} < 6.5 V, $_{OUT}$ = expected. No spread spectrum	C
OSC	6	If OSC = GND and high VIN current, then V_{OUT} = 0 V.	B
		If OSC = VDDA, VIN > 6.5 V, the device is damaged, and V_{OUT} = 0 V.	A
		If OSC = VDDA, VIN < 6.5 V, V_{OUT} = expected, and there is erratic switching.	C
LOL	7	If V_{VIN} < 6.5 V, V_{OUT} = 0 V and there is excessive current from VIN.	B
		If V_{VIN} > 6.5 V, exceeds the maximum ratings for the LO pin and the device is damaged.	A
LO	8	If V_{VIN} < 6.5 V, V_{OUT} = 0 V and there is excessive current from VIN.	B
		If V_{VIN} > 6.5 V, exceeds the maximum ratings for the LOL pin, the device is damaged	A
PGND	9	V_{OUT} = 0 V. Excessive current from VIN	B
VCC	10	If V_{VIN} < 6.5 V, then V_{OUT} = expected.	D
		If V_{VIN} > 6.5 V, exceeds the maximum ratings and the device is damaged.	A
HB	11	If V_{VIN} < 6.5 V, then V_{OUT} = expected and there is erratic switching.	B
		If V_{VIN} > 6.5 V, exceeds the maximum rating the device is damaged and V_{OUT} = VIN.	A
SW	12	V_{OUT} = VIN. Excessive current from VIN	A
HO	13	If V_{VIN} < 6.5 V, V_{OUT} drops lower than VIN, no switching, and excessive current from VIN.	B
		If V_{VIN} > 6.5 V, exceeds maximum ratings of the HO pin, the device is damaged, and V_{OUT} = VIN.	A
HOL	14	If V_{VIN} < 6.5 V, V_{OUT} drops lower than VIN, no switching, and excessive current from VIN.	B
		If V_{VIN} > 6.5 V, exceeds maximum ratings of the HO pin, the device is damaged, and V_{OUT} = VIN.	
VIN	15	N/A	B
VCCX	16	For VCCX = VOUT, V_{IN} < 6.5 V and V_{OUT} = VIN.	B
		If V_{VIN} > 6.5 V, it exceeds the VCCX pin maximum rated voltage and the LM5141-Q1 is damaged.	A
VOUT	17	If V_{VIN} < 15.5 V, VOUT = VIN.	B
		If V_{VIN} > 15.5 V and exceeds the maximum rating, the LM5141-Q1 is damaged.	A
CS		V_{VIN} < 6.5 V. V_{OUT} = VIN	B
		If V_{VIN} > 15.5 V and exceeds the maximum rating, the LM5141-Q1 is damaged.	A
FB	19	If V_{VIN} < 6.5 V, FB = VDDA, then V_{OUT} = expected.	B
		If V_{VIN} < 6.5 V, FB = GND, then V_{OUT} = 0 V. Excessive current from VIN	B
		If V_{VIN} > 6.5 V and exceeds the maximum ratings, the LM5141-Q1 is damaged.	A
COMP	20	If V_{VIN} > 5 V and < 6.5 V, V_{OUT} = 0 V	B
		If V_{VIN} > 6.5 V and exceeds the maximum ratings, the LM5141-Q1 is damaged.	A
PG	21	If V_{VIN} < 6.5 V, V_{OUT} = expected and PG forced high.	B
		If V_{VIN} > 6.5 V and exceeds the maximum ratings, the LM5141-Q1 is damaged.	A
SS	22	If V_{VIN} < 6.5 V, then V_{OUT} = expected.	D
		If V_{VIN} > 6.5 V and exceeds the maximum ratings, the LM5141-Q1 is damaged.	A
EN	23	V_{OUT} = expected	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RES	24	If V_{VIN} < 6.5 V, V_{OUT} = expected. No hiccup mode	C
		If V_{VIN} > 6.5 V and exceeds the maximum ratings, the LM5141-Q1 is damaged.	A

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