Functional Safety Information

TLV766-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TLV766-Q1 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the adjustable output device functional block diagram for reference.

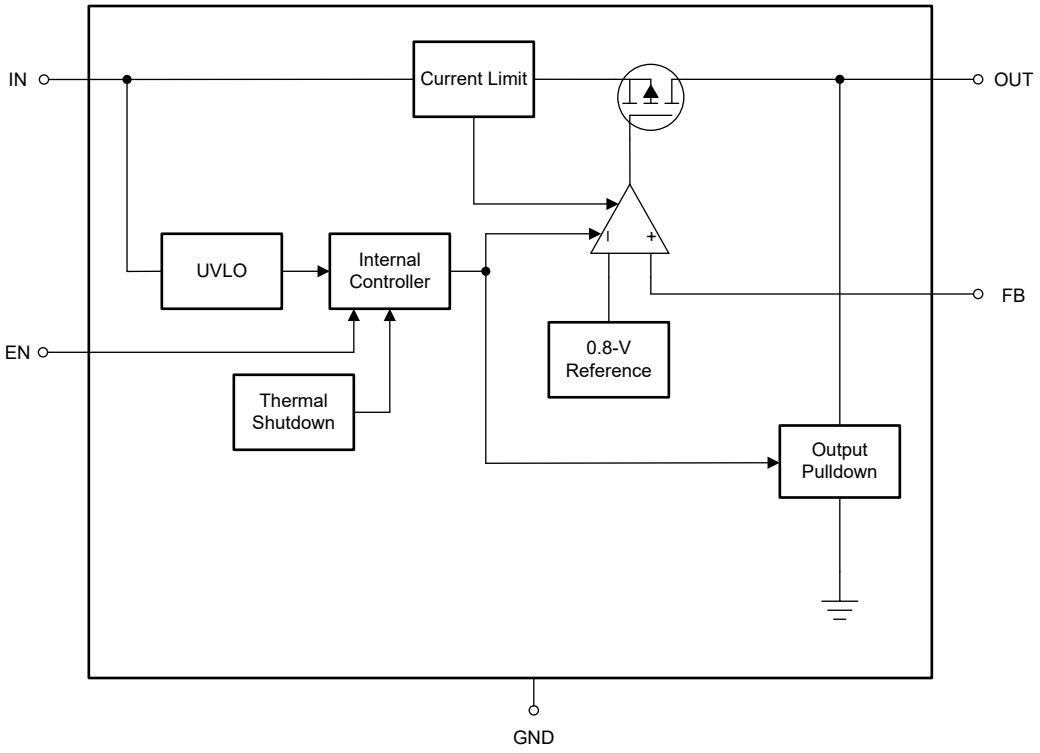

Figure 1-1. TLV766-Q1 Adjustable Output Functional Block Diagram

Figure 1-2 shows the fixed output device functional block diagram for reference.

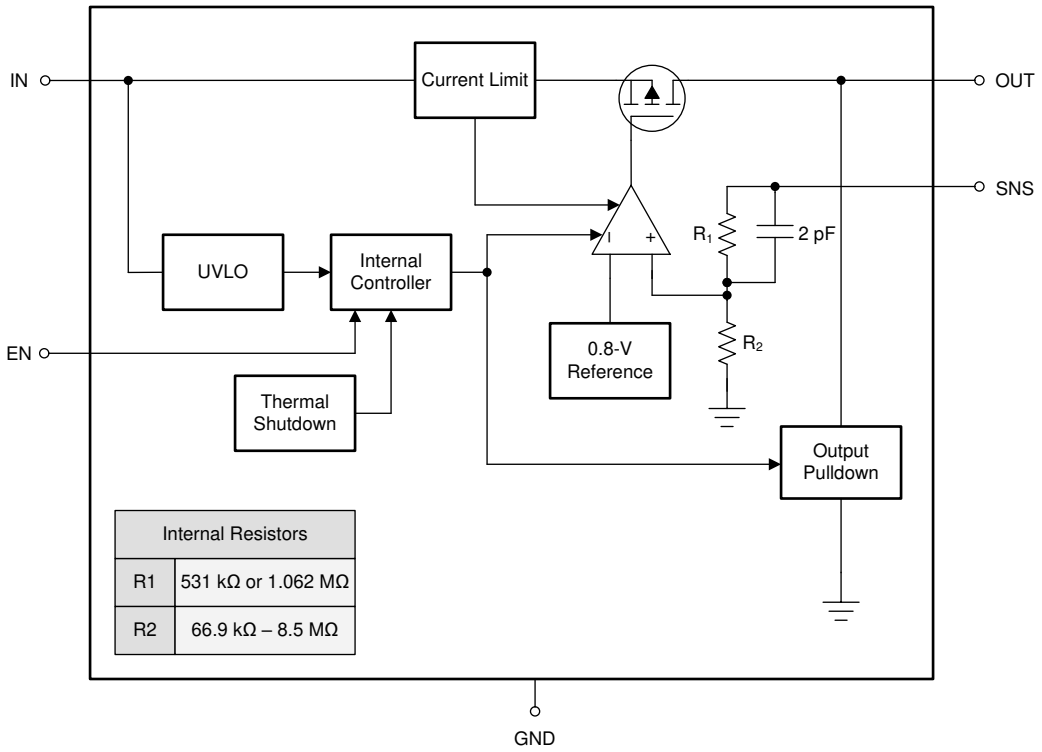

Figure 1-2. TLV766-Q1 Fixed Output Functional Block Diagram

The TLV766-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TLV766-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10
Die FIT rate	6
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLV766-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT high (following VIN)	60
VOUT not in specification - voltage or timing	10
VOUT low (no output)	20
Short circuit any two pins	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLV766-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TLV766-Q1 adjustable output pin diagram, and Figure 4-2 shows the TLV766-Q1 fixed output pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLV766-Q1 data sheet.

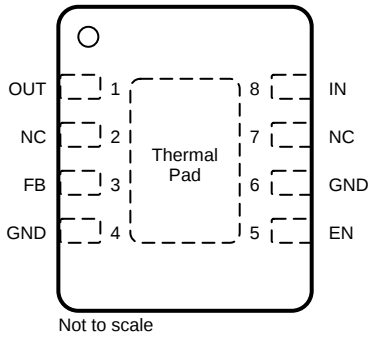

Figure 4-1. Adjustable Output Pin Diagram

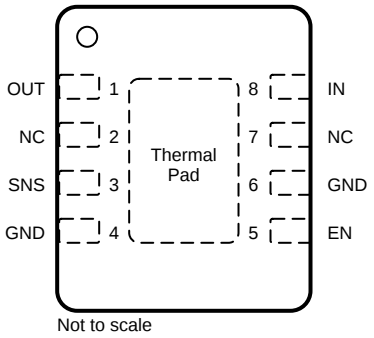

Figure 4-2. Fixed Output Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible. The device operates at current limit and can cycle in and out of thermal shutdown.	B
NC	2	No effect. Normal operation.	D
FB/SNS	3	(Fixed output.) Regulation is not possible. The device operates at current limit and can cycle in and out of thermal shutdown. (Adjustable output.) The device operates as a switch because the gate of the pass transistor is driven fully on.	B/B
GND	4	No effect. Normal operation.	D
EN	5	The device is disabled, resulting in no output voltage.	B
GND	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
IN	8	No power to the device, resulting in no output voltage.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
NC	2	No effect. Normal operation.	D
FB/SNS	3	(Fixed output.) The output voltage is incorrect. (Adjustable output.) The error amplifier input is not connected. The output voltage is indeterminate.	B/B
GND	4	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
EN	5	The enable circuit is in an unknown state. The device is either enabled or disabled.	B
GND	6	A very small possibility exists that device turns on even if EN is held low.	B
NC	7	No effect. Normal operation.	D
IN	8	No power is supplied to the device, resulting in no output voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC (pin 2)	No effect. Normal operation.	D
NC	2	FB/SNS (pin 3)	No effect. Normal operation.	D
FB/SNS	3	GND (pin 4)	(Fixed output.) Regulation is not possible. The device operates at current limit and can cycle in and out of thermal shutdown. (Adjustable output.) The device operates as a switch because the gate of the pass transistor is driven fully on.	B/B
EN	5	GND (pin 6)	The device is disabled, resulting in no output voltage.	B
GND	6	NC (pin 7)	No effect. Normal operation.	D
NC	7	IN (pin 8)	No effect. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	(Fixed output.) Regulation is not possible because VOUT = VIN, but no damage occurs because OUT and SNS can handle up to VIN + 0.3 V (max). (Adjustable output.) If FB is tied to OUT, damage is possible on FB. See the *Absolute Maximum Ratings* table in the product data sheet. If the device is configured with a resistive feedback network, no damage occurs.	B/A
NC	2	No effect. Normal operation.	D
FB/SNS	3	(Fixed output.) Regulation is not possible because VOUT = VIN. (Adjustable output.) If VIN is greater than 3 V, the rating for FB (3 V max) is violated and can damage the device. If VIN is less than 3 V and if there is any loading on the device, the output is approximately 0 V.	A/B
GND	4	No output voltage. System performance depends on upstream current limiting.	B
EN	5	The device is always enabled when the input is powered.	B
GND	6	No output voltage. System performance depends on upstream current limiting.	B
NC	7	No effect. Normal operation.	D
IN	8	No effect. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2022) to Revision A (March 2023)	Page
• Added *Failure Effect Class* value to GND row of *Pin FMA for Device Pins Open-Circuited* table	5

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265