Functional Safety Information

TPSM63606
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPSM63606 (B3QFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

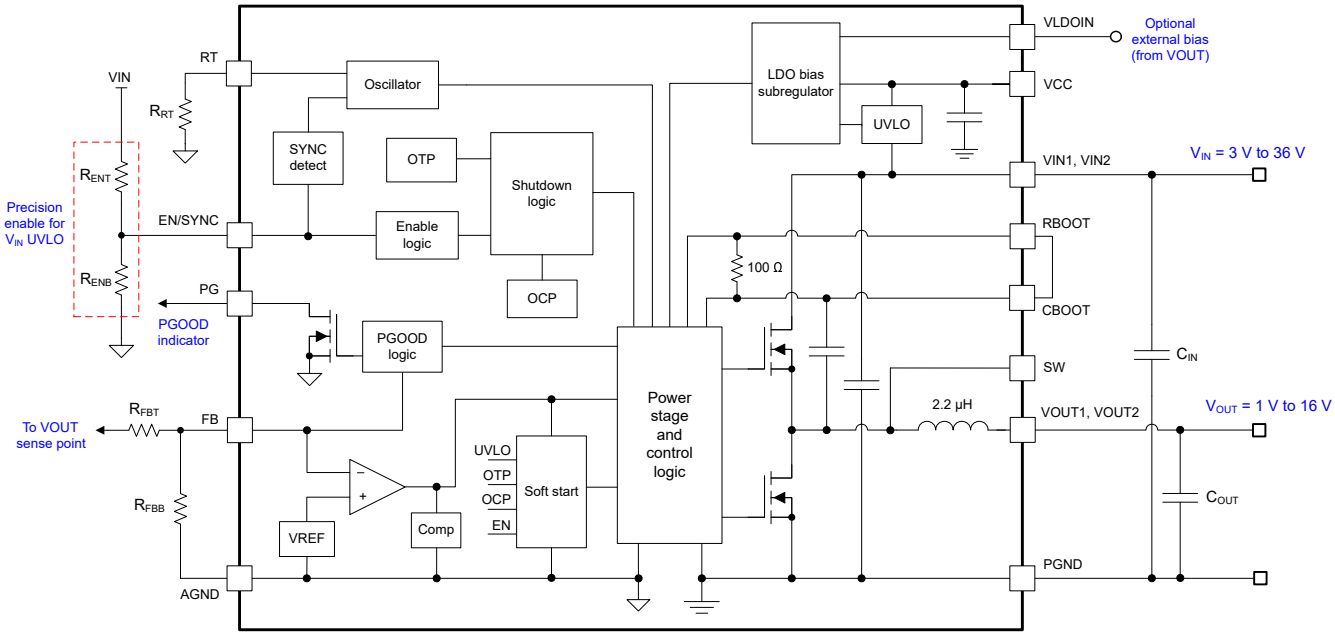

Figure 1-1. Functional Block Diagram

TPSM63606 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TPSM63606 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	22
Die FIT Rate	4
Package FIT Rate	8
Passives FIT Rate	10

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 700 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed signal less than 50 V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPSM63606 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution
No output voltage	60%
Output not in specification – voltage or timing	25%
Gate driver stuck on	5%
Power Good – false trip or fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPSM63606. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPSM63606 pin diagram. For a detailed description of the device pins, please refer to the *Pin Configuration and Functions* section in the TPSM63606 data sheet.

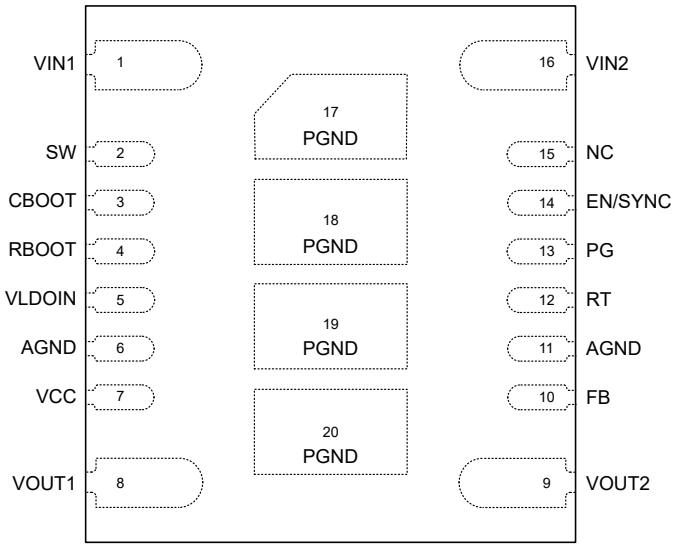

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the TPSM63606 data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN1, VIN2	1, 16	V_{OUT} = 0 V. Possible damage to customer input supply, PCB can occur unless customer provides protection, or both. Reverse current from the VOUT pin to VIN pin, due to discharge of output capacitors, can damage the regulator.	B
SW	2	Shorting the SW pin to ground will result in large currents through the device and subsequent damage. No output voltage will be produced.	A
CBOOT	3	Driver supply to high-side MOSFET will be lost. Output voltage will not be regulated. Possible damage to the internal regulator and CBOOT charging circuit	B
RBOOT	4	Loss of output voltage	A
VLDOIN	5	Normal operation, IC powers from VIN, causing decreased efficiency.	C
AGND	6, 11	No effect	D
VCC	7	Internal circuits will be disabled. No output voltage will be generated. Possible increase in input current	B
VOUT1, VOUT2	8, 9	Loss of output voltage	B
FB	10	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage level. Possible damage to customer load, output stage components can occur, or both.	B
RT	12	Loss of output voltage	B
PG	13	This is a valid connection for the PG output. PG functionality will be lost. Damage to external components connected to PG input can occur.	D
EN/SYNC	14	This is a valid connection for the EN input. Enable functionality will be lost; the device will remain off with no output voltage generated. Damage to external components connected to EN input can occur.	B
NC	15	No effect	D
PGND	17, 18, 19, 20	This is the recommended connection for PGND.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN1	1	V_{OUT} normal. Current loop will be affected, potentially affecting noise/jitter/EMI/ reliability.	C
SW	2	Normal operation	D
CBOOT	3	Normal operation	D
RBOOT	4	Normal operation	D
VLDOIN	5	Normal operation, IC powers from VIN, causing decreased efficiency.	C
AGND	6, 11	Load regulation degraded	C
VCC	7	Normal operation	D
VOUT1	8	V_{OUT} normal. Current loop will be affected, potentially affecting noise/jitter/EMI/ reliability.	C
VOUT2	9	V_{OUT} normal. Current loop will be affected, potentially affecting noise/jitter/EMI/ reliability.	C
FB	10	V_{OUT} >> than programmed output voltage.	B
RT	12	Loss of output voltage	B
PG	13	This is a valid connection for the PG output. PG functionality will be lost.	D
EN/SYNC	14	Loss of enable functionality. Erratic operation; probable loss of regulation	B
NC	15	Valid connection	D
VIN2	16	V_{OUT} normal. Current loop will be affected, potentially affecting noise/jitter/EMI/ reliability.	C
PGND	17, 18, 19, 20	Load regulation degraded, thermal impedance impacted. Loss of operation if all four pins are open.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VIN1	1	SW	Damage to low-side FET	A
SW	2	CBOOT	Loss of high-side gate drive supply	B
CBOOT	3	RBOOT	Valid connection	D
RBOOT	4	VLDOIN	Possible damage to internal circuits	A
VLDOIN	5	AGND	Valid connection. Possible decrease in efficiency when VLDOIN is intended to be tied to VOUT or external bias supply	D
AGND	6	VCC	Internal circuits will be disabled. No output voltage will be generated.	B
VCC	7	VOUT1	VCC ESD clamp damaged if V_{OUT} > 5 V.	A
VOUT1	8	VOUT2	Valid connection	D
VOUT2	9	FB	V_{OUT} = 1 V	B
FB	10	AGND	V_{OUT} close to V_{IN}	B
AGND	11	RT	Loss of output voltage	B
RT	12	PG	Possible damage to internal circuits	A
PG	13	EN/SYNC	Possible damage to internal PG circuit if $V_{EN/SYNC}$ > 16 V	A
EN/SYNC	14	NC	No effect	C
NC	15	VIN2	No effect	
VIN2	16	VIN1	Valid connection	D
PGND	17, 18, 19, 20	Any	Other pin is shorted to ground, see Table 4-5.	–

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (VIN1 and/or VIN2)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN1, VIN2	1, 16	No effect (normal operation)	D
SW	2	Damage to low-side FET	A
CBOOT	3	V_{OUT} = 0 V. CBOOT ESD clamp will run current to destruction.	A
RBOOT	4	V_{OUT} = 0 V. RBOOT ESD clamp will run current to destruction.	A
VLDOIN	5	If VIN exceeds 16 V, damage will occur. If below, normal operation	A
AGND	6, 11	V_{OUT} = 0 V. Damage to other pins referred to GND	A
VCC	7	If VIN exceeds 5.5 V, damage will occur.	A
VOUT1, VOUT2	8, 9	Damage to low-side FET. The output voltage will rise to nearly the level of VIN. Customer load will be damaged. Possible damage to device	A
FB	10	If VIN exceeds 16 V, damage will occur. V_{OUT} = 0 V	A
RT	12	V_{OUT} = 0 V	B
PG	13	V_{OUT} = 0 V. PGOOD ESD clamp will run current to destruction.	A
EN/SYNC	14	Normal operation; enable functionality will be lost, the device will remain on.	D
NC	15	No effect	D
PGND	17, 18, 19, 20	V_{OUT} = 0 V. Damage to low-side circuitry if V_{PGND} >> V_{AGND}	B

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