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1 Overview

This document contains information for the ADS130B02-Q1 (TSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

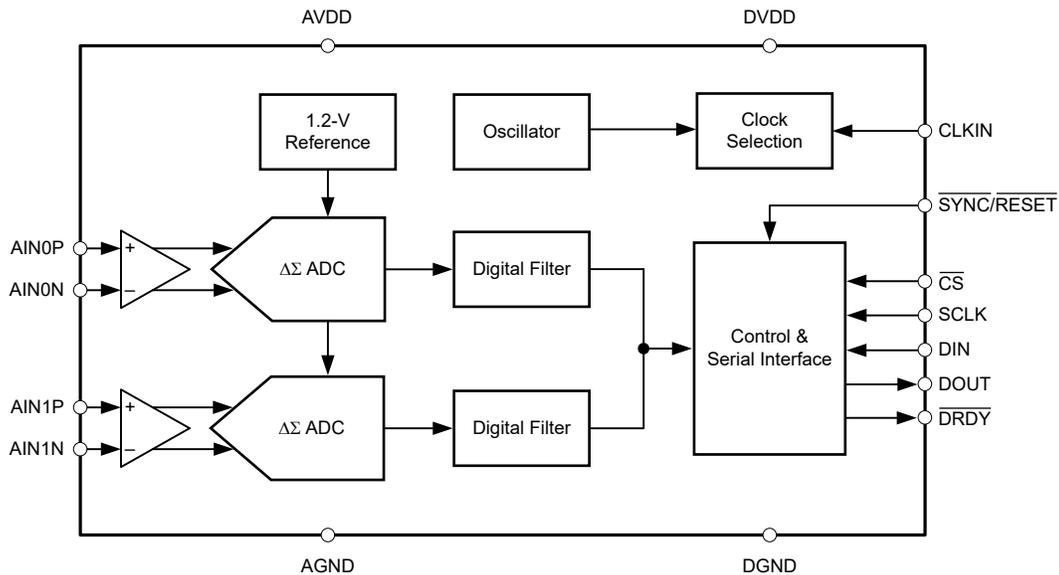


Figure 1-1. Functional Block Diagram

The ADS130B02-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the ADS130B02-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	13
Die FIT rate	2
Package FIT rate	11

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 15.2 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ADS130B02-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Incorrect conversion result of individual ADC ⁽¹⁾ . (For example, ADC output code at positive or negative full scale, at 0 V, undetermined or otherwise incorrect.)	25%
SPI communication error	15%
Register bit error leading to incorrect device configuration. (Device behavior depends on which user or internal register bit is affected.)	15%
Gain error of individual ADC out of specification ⁽¹⁾	10%
Offset error of individual ADC out of specification ⁽¹⁾	5%
Noise of conversion result of individual ADC out of specification ⁽¹⁾	5%
INL of individual ADC out of specification ⁽¹⁾	5%
Gain error, INL, or noise of conversion results of both ADCs out of specification resulting from common circuitry. (Common circuitry includes internal supplies, voltage reference, bias current generator, and clock.)	5%
Oscillator fault leading to incorrect data rate. (For example, oscillator frequency too high or low, oscillator output stuck-at.)	5%
ADC output code bit stuck-at	5%
Device behavior undetermined	5%

(1) The failure mode percentage provided is for the sum of the two ADCs. For a single ADC divide the failure mode percentage by 2x.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ADS130B02-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the ADS130B02-Q1 pin diagram. For a detailed description of the device pins see the *Pin Configuration and Functions* section in the ADS130B02-Q1 data sheet.

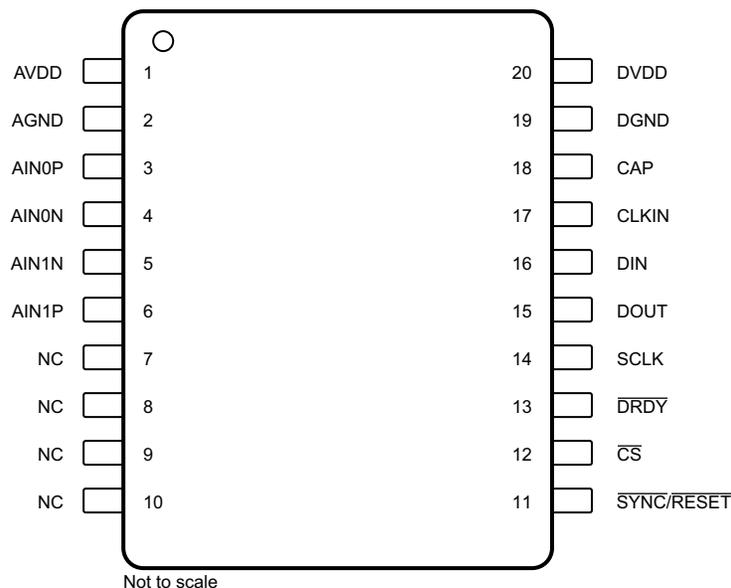


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- AVDD and DVDD use the same 3.3-V supply voltage.
- *Short circuit to supply* means short to AVDD = DVDD.
- *Short circuit to ground* means short to AGND = DGND.
- Differential RC filters on every ADC channel.
Series resistors are sized to limit the input currents into the analog inputs to <10 mA in all circumstances (for example, in case the device is unpowered and the input signal is applied).
- External pulldown resistor ($\geq 1 \text{ k}\Omega$) on CLKIN to DGND in case the device is configured for use with the internal oscillator.
- NC pins are left unconnected.
- The device is the only peripheral on the SPI bus.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AGND	2	No effect. Normal operation.	D
AIN0P	3	AIN0P stuck low. $V_{IN0} = V_{AIN0P} - V_{AIN0N} = AGND - V_{AIN0N}$. Conversion results of ADC0 incorrect.	B
AIN0N	4	AIN0N stuck low. $V_{IN0} = V_{AIN0P} - V_{AIN0N} = V_{AIN0P} - AGND$. Conversion results of ADC0 incorrect.	B
AIN1N	5	AIN1N stuck low. $V_{IN1} = V_{AIN1P} - V_{AIN1N} = V_{AIN1P} - AGND$. Conversion results of ADC1 incorrect.	B
AIN1P	6	AIN1P stuck low. $V_{IN1} = V_{AIN1P} - V_{AIN1N} = AGND - V_{AIN1N}$. Conversion results of ADC1 incorrect.	B
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
SYNC/RESET	11	SYNC/RESET stuck low. Device held in reset.	B
\overline{CS}	12	\overline{CS} stuck low. Normal operation when trying to communicate with the ADS130B02-Q1.	B
\overline{DRDY}	13	\overline{DRDY} stuck low. No data-ready indication through \overline{DRDY} pin to host possible. Increase in supply current when \overline{DRDY} tries to drive high in case bit DRDY_HiZ = 0b. Device damage plausible if \overline{DRDY} drives high for extended period of time.	A
SCLK	14	SCLK stuck low. No SPI communication with device possible.	B
DOUT	15	DOUT stuck low. No SPI communication back to host possible. Increase in supply current when DOUT tries to drive high. Device damage plausible if DOUT drives high for extended period of time.	A
DIN	16	DIN stuck low. No SPI communication with device possible.	B
CLKIN	17	Device configured for use with external clock: CLKIN stuck low. No clock provided to device. Device not functional, but SPI communication with device possible.	B
		Device configured for use with internal oscillator: CLKIN stuck low. No effect. Normal operation.	D
CAP	18	Device unpowered. Device not functional.	B
DGND	19	No effect. Normal operation.	D
DVDD	20	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	Device functionality undetermined. Device unpowered and not functional if all external analog pins are held low. Device may power up through internal ESD diodes to AVDD if voltages above the device power-on reset threshold are present on any of the analog pins.	B
AGND	2	Device functionality undetermined. Device may be unpowered or connect to ground internally through alternate pin ESD diode and power up.	B
AIN0P	3	State of AIN0P input undetermined. Conversion results of ADC0 undetermined.	B
AIN0N	4	State of AIN0N input undetermined. Conversion results of ADC0 undetermined.	B
AIN1N	5	State of AIN1N input undetermined. Conversion results of ADC1 undetermined.	B
AIN1P	6	State of AIN1P input undetermined. Conversion results of ADC1 undetermined.	B
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
$\overline{\text{SYNC/RESET}}$	11	State of $\overline{\text{SYNC/RESET}}$ input undetermined. Device functionality undetermined. Device may operate normally or be held in reset.	B
$\overline{\text{CS}}$	12	State of $\overline{\text{CS}}$ input undetermined. SPI communication corrupted.	B
$\overline{\text{DRDY}}$	13	State of $\overline{\text{DRDY}}$ output undetermined. No data-ready indication through $\overline{\text{DRDY}}$ pin to host possible.	B
SCLK	14	State of SCLK input undetermined. No SPI communication with device possible.	B
DOUT	15	State of DOUT output undetermined. No SPI communication back to host possible.	B
DIN	16	State of DIN input undetermined. No SPI communication with device possible.	B
CLKIN	17	Device configured for use with external clock. State of CLKIN input undetermined. No clock provided to device. Device not functional, but SPI communication with device possible.	B
		Device configured for use with internal oscillator. State of CLKIN input undetermined. No effect. Normal operation.	D
CAP	18	Internal digital LDO unstable. Device functionality undetermined.	B
DGND	19	Device functionality undetermined. Device may be unpowered or connect to ground internally through alternate pin ESD diode and power up.	B
DVDD	20	Device functionality undetermined. Device unpowered and not functional if all external digital pins are held low. Device may power up through internal ESD diodes to DVDD if voltages above the device power-on reset threshold are present on any of the digital pins.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	AGND	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AGND	2	AIN0P	AIN0P stuck low. $V_{IN0} = V_{AIN0P} - V_{AIN0N} = AGND - V_{AIN0N}$. Conversion results of ADC0 incorrect.	B
AIN0P	3	AIN0N	$V_{IN0} = V_{AIN0P} - V_{AIN0N} = 0$ V. Conversion result of ADC0 close to 0 V.	B
AIN0N	4	AIN1N	Conversion results of ADC0 and ADC1 undetermined.	B
AIN1N	5	AIN1P	$V_{IN1} = V_{AIN1P} - V_{AIN1N} = 0$ V. Conversion result of ADC1 close to 0 V.	B
AIN1P	6	NC	No effect. Normal operation.	D
NC	7	NC	No effect. Normal operation.	D
NC	8	NC	No effect. Normal operation.	D
NC	9	NC	No effect. Normal operation.	D
NC	10	SYNC/RESET	Not considered. Corner pin.	D
SYNC/RESET	11	CS	Device behavior dependent on drive strength of control signals driving CS and SYNC/RESET pins. In case SYNC/RESET control signal can overdrive CS control signal, CS stuck high or SPI communication corrupted. No SPI communication with device possible. In case CS control signal can overdrive SYNC/RESET control signal, the device synchronizes conversions every time CS transitions high. Conversion results are valid but data ready is indicated outside the expected time window. In case the SYNC/RESET pin is held low for longer than the reset time period, then device reset occurs.	B
CS	12	DRDY	SPI communication corrupted. No SPI communication with device possible. Increase in supply current possible when DRDY tries to drive low while CS is driven high and vice versa. Device damage plausible if this condition exists for extended period of time.	A
DRDY	13	SCLK	SPI communication corrupted. No SPI communication with device possible. Increase in supply current possible when DRDY tries to drive low while SCLK is driven high and vice versa. Device damage plausible if this condition exists for extended period of time.	A
SCLK	14	DOUT	SPI communication corrupted. No SPI communication with device possible. Increase in supply current possible when DOUT tries to drive low while SCLK is driven high and vice versa. Device damage plausible if this condition exists for extended period of time.	A
DOUT	15	DIN	SPI communication corrupted. No SPI communication with device possible. Increase in supply current possible when DOUT tries to drive low while DIN is driven high and vice versa. Device damage plausible if this condition exists for extended period of time.	A
DIN	16	CLKIN	Device configured for use with external clock: SPI communication corrupted. No SPI communication with device possible. CLKIN signal corrupted. Device behavior undetermined.	B
			Device configured for use with internal oscillator. No effect. Normal operation as long as DIN can drive the pull-down resistor between CLKIN and DGND.	D
CLKIN	17	CAP	Device configured for use with external clock. Device behavior undetermined. Device damage plausible when CLKIN pin drives digital core LDO output on CAP pin to >1.8 V.	A
			Device configured for use with internal oscillator. Digital core LDO output drives external pull-down resistor on CLKIN pin to 1.8 V. Increase in digital supply current. Otherwise normal operation.	D
CAP	18	DGND	Device unpowered. Device not functional.	B
DGND	19	DVDD	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DVDD	20	AVDD	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	No effect. Normal operation.	D
AGND	2	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AIN0P	3	AIN0P stuck high. $V_{IN0} = V_{AIN0P} - V_{AIN0N} = AVDD - V_{AIN0N}$. Conversion results of ADC0 incorrect.	B
AIN0N	4	AIN0N stuck high. $V_{IN0} = V_{AIN0P} - V_{AIN0N} = V_{AIN0P} - AVDD$. Conversion results of ADC0 incorrect.	B
AIN1N	5	AIN1N stuck high. $V_{IN1} = V_{AIN1P} - V_{AIN1N} = V_{AIN1P} - AVDD$. Conversion results of ADC1 incorrect.	B
AIN1P	6	AIN1P stuck high. $V_{IN1} = V_{AIN1P} - V_{AIN1N} = AVDD - V_{AIN1N}$. Conversion results of ADC1 incorrect.	B
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D
NC	9	No effect. Normal operation.	D
NC	10	No effect. Normal operation.	D
$\overline{\text{SYNC/RESET}}$	11	No effect. Normal operation. Device cannot be reset or synchronized using the $\overline{\text{SYNC/RESET}}$ pin any more.	B
$\overline{\text{CS}}$	12	$\overline{\text{CS}}$ stuck high. No SPI communication with device possible.	B
$\overline{\text{DRDY}}$	13	$\overline{\text{DRDY}}$ stuck high. No data-ready indication through $\overline{\text{DRDY}}$ pin to host possible. Increase in supply current when $\overline{\text{DRDY}}$ tries to drive low. Device damage plausible if $\overline{\text{DRDY}}$ drives low for extended period of time.	A
SCLK	14	SCLK stuck high. No SPI communication with device possible.	B
DOUT	15	DOUT stuck high. No SPI communication back to host possible. Increase in supply current when DOUT tries to drive low. Device damage plausible if DOUT drives low for extended period of time.	A
DIN	16	DIN stuck high. No SPI communication with device possible.	B
CLKIN	17	Device configured for use with external clock: CLKIN stuck high. No clock provided to device. Device not functional, but SPI communication with device possible.	B
		Device configured for use with internal oscillator: CLKIN stuck high. No effect. Normal operation.	D
CAP	18	Device may operate normally, but permanent device damage within short period of time is very plausible. Device not functional anymore in case of damage.	A
DGND	19	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DVDD	20	No effect. Normal operation.	D

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