

# LM5146 Functional Safety, FIT Rate, and Failure Mode Distribution



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## 1 Overview

This document contains information for LM5146 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

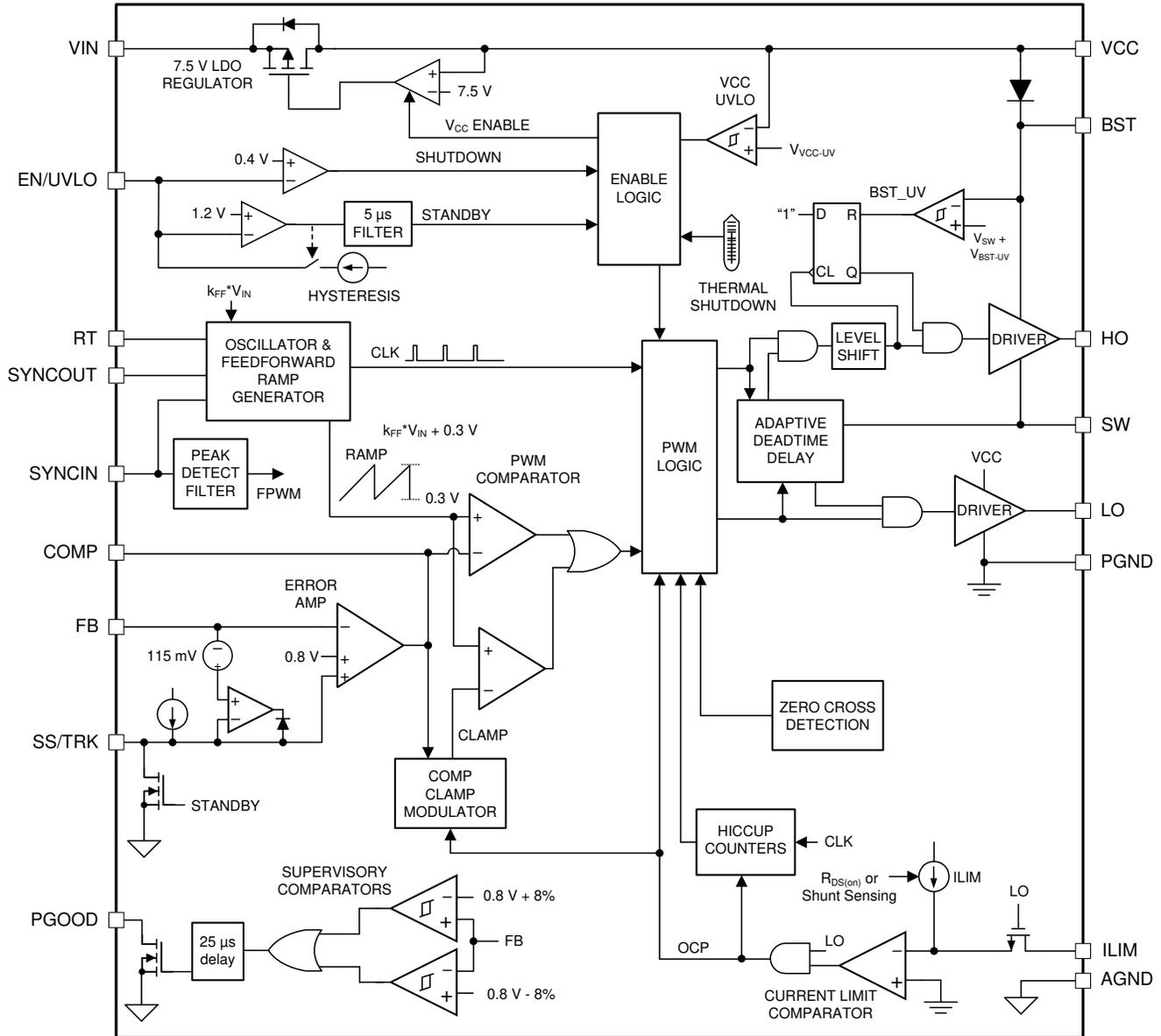


Figure 1-1. Functional Block Diagram

LM5146 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM5146 in [Table 2-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 2-1. Die Failure Modes and Distribution**

| Die Failure Modes  | Failure Mode Distribution (%) |
|--|-------------------------------|
| HO or LO gate driver stuck off                           | 20%                           |
| HO or LO output not in specification – voltage or timing | 45%                           |
| Ho or LO gate driver open – high Z                       | 10%                           |
| HO or LO gate driver stuck on                            | 20%                           |
| PGOOD false trip, fails to trip                          | 5%                            |

The FMD in excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

### 3 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM5146 based on two different industry-wide used reliability standards:

- [Table 3-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 3-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 3-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per 10 <sup>9</sup> Hours) |
|------------------------------|--|
| Total Component FIT Rate     | 30                                       |
| Die FIT Rate                 | 6  |
| Package FIT Rate             | 24                                       |

The failure rate and mission profile information in [Table 3-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 750 mW
- Climate type: World-wide Table 8
- Package factor ( $\lambda_3$ ): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 3-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category  | Reference FIT Rate | Reference Virtual T <sub>J</sub> |
|-------|---|--------------------|----------------------------------|
| 5     | CMOS/BICMOS ASICs Analog & Mixed HV >50V supply | 30 FIT             | 75°C                             |

The Reference FIT Rate and Reference Virtual T<sub>J</sub> (junction temperature) in [Table 3-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM5146. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

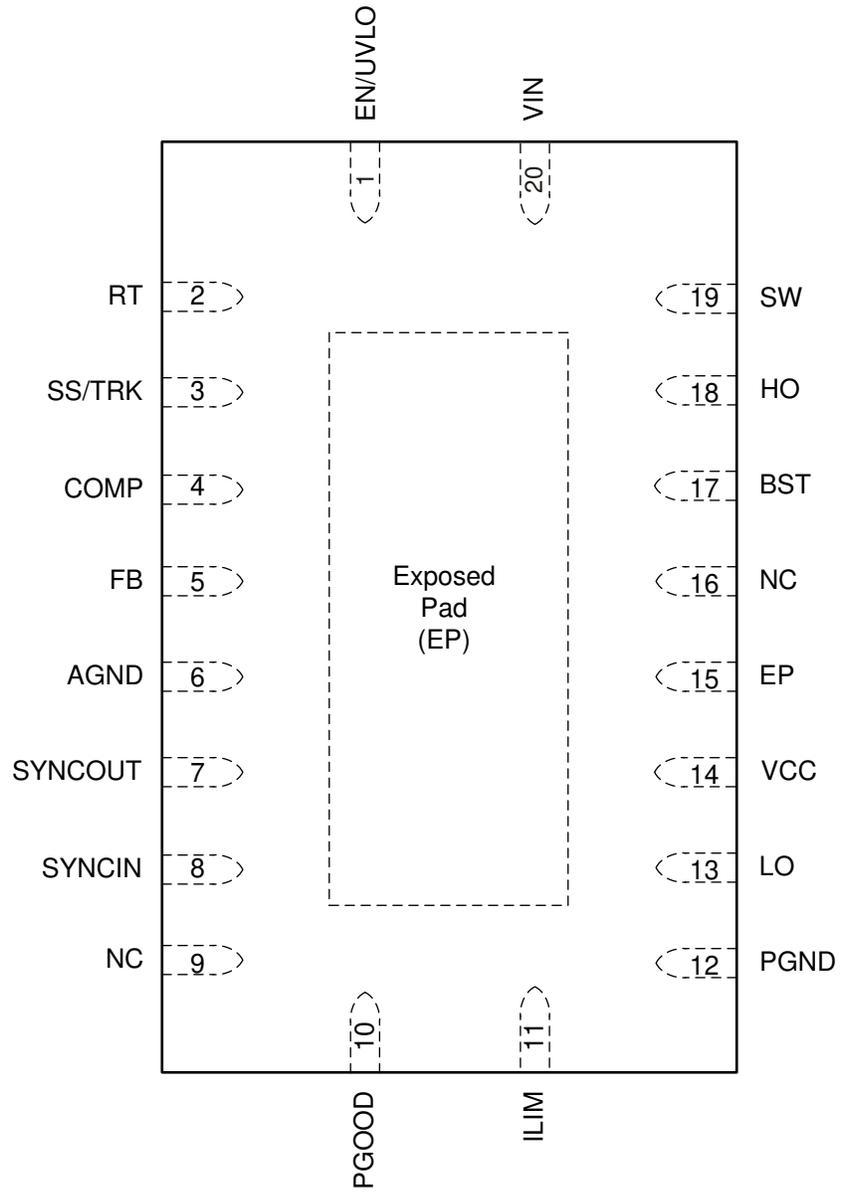
- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin short-circuited to 12 V (see [Table 4-3](#))
- Pin open-circuited (see [Table 4-5](#))
- Pin short-circuited to an adjacent pin (see [Table 4-6](#))

[Table 4-2](#) through [Table 4-6](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects   |
|-------|---|
| A     | Potential device damage that affects functionality          |
| B     | No device damage, but loss of functionality                 |
| C     | No device damage, but performance degradation               |
| D     | No device damage, no impact to functionality or performance |

[Figure 4-1](#) shows the LM5146 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM5146 data sheet.



**Figure 4-1. Pin Diagram**

**Table 4-2. Pin FMA for Short to GND**

| Pin Name | Pin No. | Description of Potential Failure Effect(s)               | Failure Effect Class |
|----------|---------|--|----------------------|
| EN/UVLO  | 1       | VOUT = 0 V   | B                    |
| RT       | 2       | VOUT = 0 V   | B                    |
| SS/TRK   | 3       | VOUT = 0 V   | B                    |
| COMP     | 4       | VOUT = 0 V   | B                    |
| FB       | 5       | VOUT is limited by when the part enters into hiccup mode | B                    |
| AGND     | 6       | Normal operation   | D                    |
| SYNCOUT  | 7       | VOUT = 0 V   | B                    |
| SYNCIN   | 8       | Normal operation with DCM at light loads                 | B                    |
| NC9      | 9       | Normal operation   | D                    |
| PGOOD    | 10      | Normal operation   | C                    |
| ILIM     | 11      | Normal operation   | B                    |
| PGND     | 12      | Normal operation   | D                    |
| LO       | 13      | VOUT = 0 V   | B                    |
| VCC      | 14      | VOUT = 0 V   | B                    |
| EP       | 15      | Normal operation   | D                    |
| NC16     | 16      | Normal operation   | D                    |
| BST      | 17      | VOUT = 0 V   | B                    |
| HO       | 18      | VOUT = 0 V   | B                    |
| SW       | 19      | VOUT = 0 V   | A                    |
| VIN      | 20      | VOUT = 0 V   | B                    |

**Table 4-3. Pin FMA for Short to VIN  $\geq$  12 V**

| Pin Name | Pin No. | Description of Potential Failure Effect(s)   | Failure Effect Class |
|----------|---------|--|----------------------|
| EN/UVLO  | 1       | ESD protection runs full current and RT pin destroyed (VOUT = 0 V)                                 | C                    |
| RT       | 2       | ESD protection runs full current and SS pin destroyed (VOUT = 0 V)                                 | A                    |
| SS/TRK   | 3       | ESD protection runs full current and COMP destroyed (VOUT = 0 V)                                   | A                    |
| COMP     | 4       | ESD protection runs full current and COMP pin destroyed (VOUT = 0 V)                               | A                    |
| FB       | 5       | ESD protection runs full current and FB pin destroyed (VOUT = 0 V)                                 | A                    |
| AGND     | 6       | VOUT = 0 V   | D                    |
| SYNCOUT  | 7       | ESD protection runs full current and SYNCOUT pin destroyed (VOUT = 0 V)                            | A                    |
| SYNCIN   | 8       | ESD protection runs full current and SYNCIN pin destroyed, but the part continues to work normally | A                    |
| NC9      | 9       | Normal operation   | D                    |
| PGOOD    | 10      | ESD protection runs full current and PGOOD pin destroyed, but VOUT might not be affected           | A                    |
| ILIM     | 11      | Buck operation is not affected   | C                    |
| PGND     | 12      | VOUT = 0 V   | B                    |
| LO       | 13      | VOUT = 0 V   | B                    |
| VCC      | 14      | ESD protection runs full current and VCC pin destroyed (VOUT = 0 V)                                | A                    |
| EP       | 15      | Normal operation   | D                    |
| NC16     | 16      | Normal operation   | D                    |
| BST      | 17      | ESD protection runs full current and BST pin destroyed (VOUT = 0 V)                                | A                    |
| HO       | 18      | VOUT = VIN   | A                    |
| SW       | 19      | VOUT = VIN   | B                    |
| VIN      | 20      | Normal operation   | D                    |

**Table 4-4. Pin FMA for Short to VOUT**

| Pin Name | Pin Number | Description of Potential Failure Effect(s) | Failure Class |
|----------|------------|--|---------------|
| EN/UVLO  | 1          | VOUT = 0 V                                 | B             |
| RT       | 2          | VOUT = 0 V                                 | A             |
| SS/TRK   | 3          | VOUT = 0 V                                 | A             |
| COMP     | 4          | VOUT = 0 V                                 | A             |
| FB       | 5          | VOUT = VREF                                | A             |
| AGND     | 6          | VOUT = 0 V                                 | B             |
| SYNCOUT  | 7          | Normal operation                           | A             |
| SYNCIN   | 8          | Normal operation. FPWM enabled             | A             |
| NC9      | 9          | Normal operation                           | D             |
| PGOOD    | 10         | Normal operation                           | A             |
| ILIM     | 11         | Normal operation                           | C             |
| PGND     | 12         | VOUT = 0 V                                 | B             |
| LO       | 13         | VOUT = 0 V                                 | B             |
| VCC      | 14         | VOUT = 0 V                                 | A             |
| EP       | 15         | Normal operation                           | D             |
| NC16     | 16         | Normal operation                           | D             |
| BST      | 17         | VOUT = 0 V                                 | B             |
| HO       | 18         | VOUT = 0 V                                 | B             |
| SW       | 19         | VOUT = 0 V                                 | B             |
| VIN      | 20         | VOUT = VIN                                 | B             |

**Table 4-5. Pin FMA Open-Circuited**

| Pin Name | Pin Number | Description of Potential Failure Effect(s)                   | Failure Class |
|----------|------------|--|---------------|
| EN/UVLO  | 1          | VOUT = 0 V   | B             |
| RT       | 2          | VOUT = 0 V   | B             |
| SS/TRK   | 3          | Normal operation   | C             |
| COMP     | 4          | Regulated to required voltage. SW freq is all over the place | B             |
| FB       | 5          | VOUT = 0 V   | B             |
| AGND     | 6          | VOUT = 0 V   | B             |
| SYNCOUT  | 7          | Normal operation   | C             |
| SYNCIN   | 8          | Normal operation. DCM mode                                   | C             |
| NC9      | 9          | Normal operation   | D             |
| PGOOD    | 10         | Normal operation   | C             |
| ILIM     | 11         | Normal operation   | C             |
| PGND     | 12         | VOUT = 0 V   | B             |
| LO       | 13         | Normal operation. DCM mode enabled at light loads            | B             |
| VCC      | 14         | VOUT = 0 V   | B             |
| EP       | 15         | Normal operation   | D             |
| NC16     | 16         | Normal operation   | D             |
| BST      | 17         | VOUT = 0 V   | B             |
| HO       | 18         | VOUT = 0 V   | B             |
| SW       | 19         | VOUT = 0 V   | B             |
| VIN      | 20         | VOUT = 0 V   | B             |

**Table 4-6. Pin FMA for Short-Circuited to Adjacent Pin**

| Pin Name | Pin Number | Description of Potential Failure Effect(s)   | Failure Class | Neighbor |
|----------|------------|--|---------------|----------|
| EN/UVLO  | 1          | Normal operation   | C             | VIN      |
| RT       | 2          | VOUT = 0 V   | B             | SS/TRK   |
| SS/TRK   | 3          | VOUT = 0 V   | B             | COMP     |
| COMP     | 4          | VOUT is not regulated to required voltage and is controlled by the ON time it makes when COMP is 0.8 V and the switching frequency set by RT pin | B             | FB       |
| FB       | 5          | VOUT is limited by when the part enters into hiccup mode   | B             | AGND     |
| AGND     | 6          | VOUT = 0 V   | B             | SYNCOUT  |
| SYNCOUT  | 7          | Normal operation   | C             | SYNCIN   |
| SYNCIN   | 8          | Normal operation   | D             | NC9      |
| NC9      | 9          | Normal operation   | D             |          |
| PGOOD    | 10         | Normal operation   | A             | ILIM     |
| ILIM     | 11         | Normal operation   | D             |          |
| PGND     | 12         | VOUT = 0 V   | A             | LO       |
| LO       | 13         | VOUT = 0 V   | B             | VCC      |
| VCC      | 14         | Normal operation   | D             | EP       |
| EP       | 15         | Normal operation   | D             | NC16     |
| NC16     | 16         | Normal operation   | D             | BST      |
| BST      | 17         | VOUT = 0 V   | B             | HO       |
| HO       | 18         | VOUT = 0 V   | B             | SW       |
| SW       | 19         | Normal operation   | D             |          |
| VIN      | 20         | Normal operation   | D             |          |

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