Functional Safety Information

TCAN11623-Q1 and TCAN11625-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

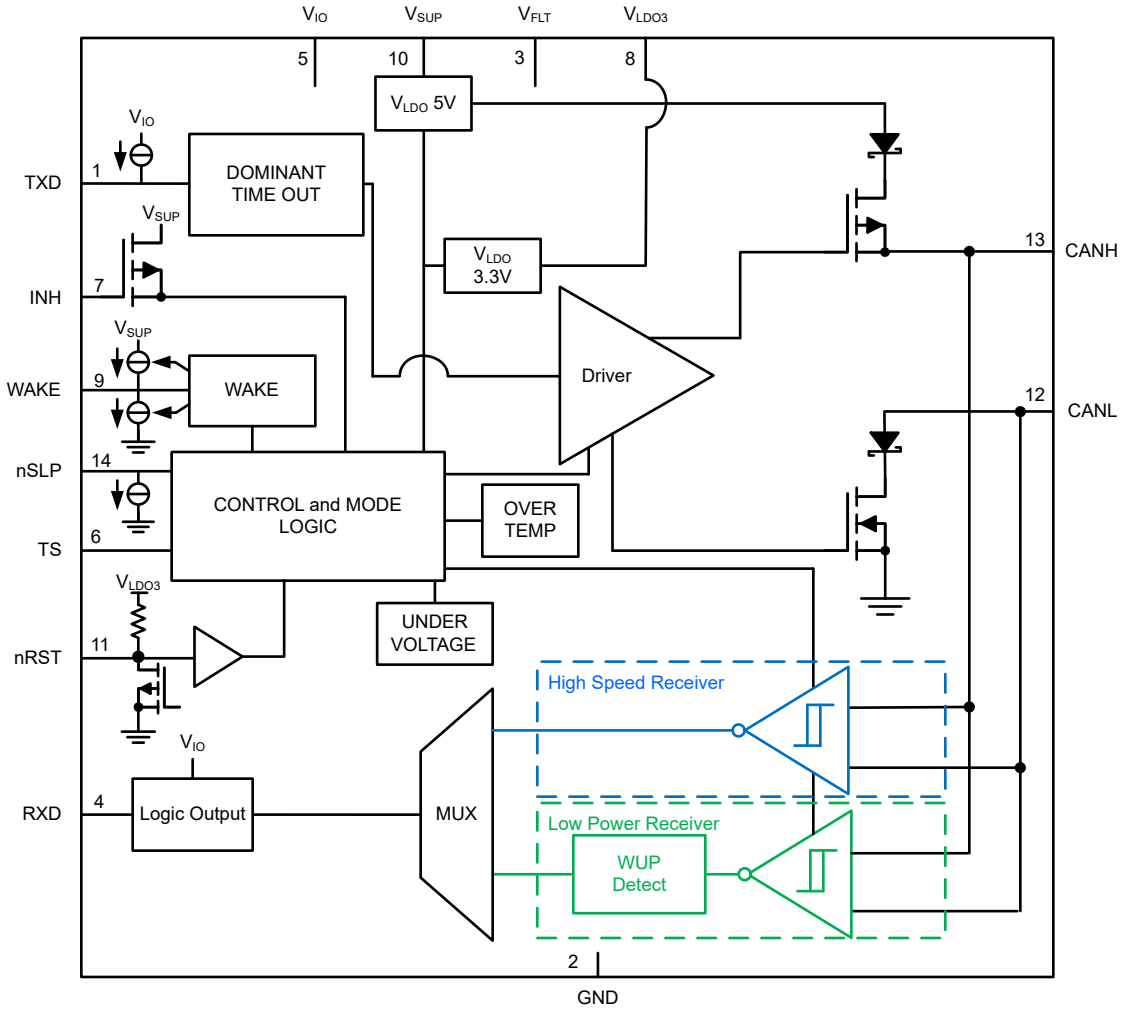
Trademarks

1 Overview

This document contains information for TCAN11623-Q1 and TCAN11625-Q1 (DTM package) to aid in a functional safety system design. Information provided are:

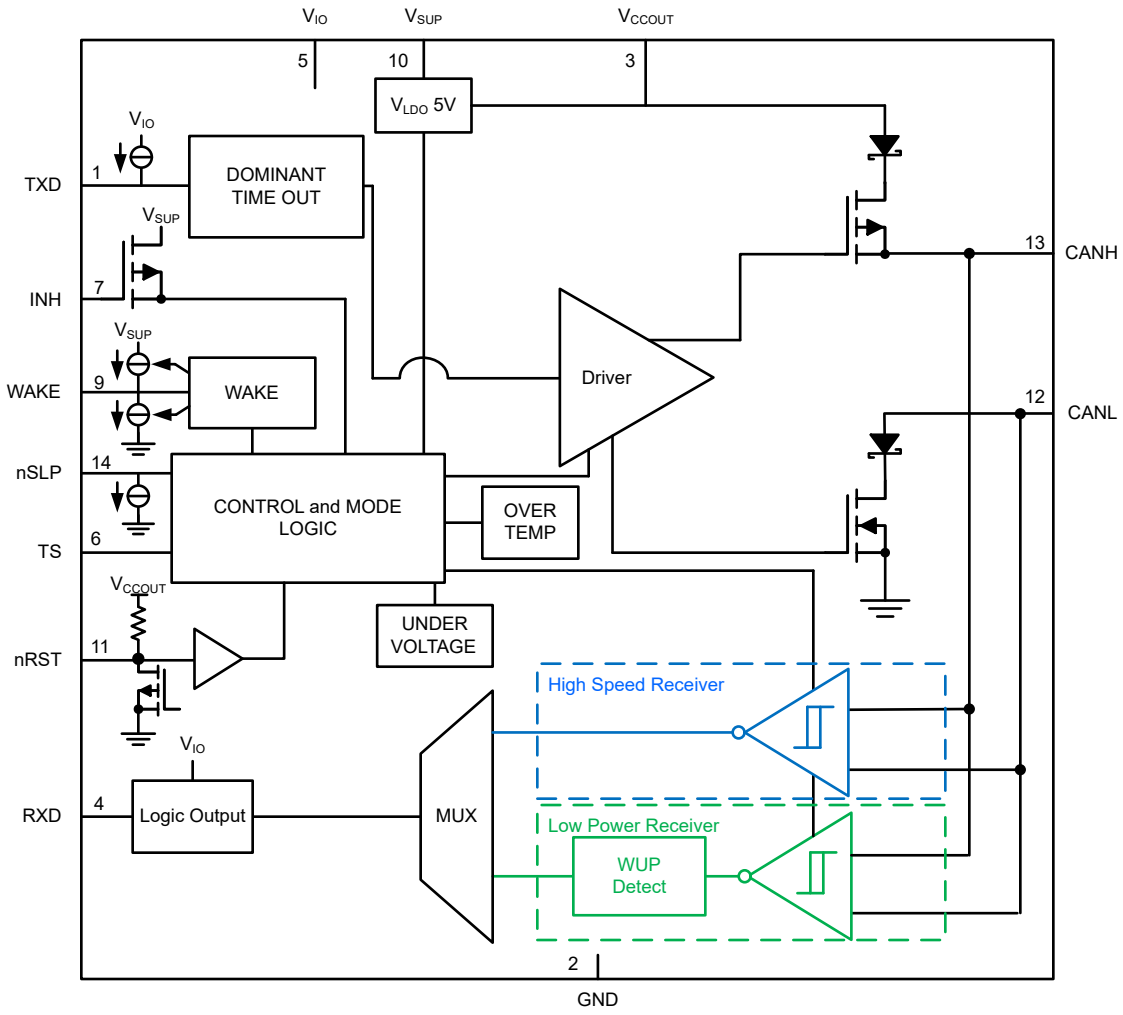
- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 and Figure 1-2 shows the device functional block diagram for reference.



A. WUP = Wake-up pattern

Figure 1-1. Functional Block Diagram (TCAN11623-Q1)



A. WUP = Wake-up pattern

Figure 1-2. Functional Block Diagram (TCAN11625-Q1)

The TCAN11623-Q1 and TCAN11625-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 TCAN11623-Q1 DMT Package

This section provides Functional Safety Failure In Time (FIT) rates for DMT package of TCAN11623-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	29
Die FIT Rate	21
Package FIT Rate	8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1940 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 TCAN11625-Q1 DMT Package

This section provides Functional Safety Failure In Time (FIT) rates for the DTM package of TCAN11625-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	36
Die FIT Rate	28
Package FIT Rate	8

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 2210 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCAN11623-Q1 and TCAN11625-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
CAN transceiver transmitter fail	21
CAN transceiver receiver fail	8
Power rail fail	23
Input/output fail	29
Digital core fail	16
Voltage monitor fail	3

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TCAN11623-Q1 and TCAN11625-Q1 (DMT package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-8.)
- Pin open-circuited (seeTable 4-3 and Table 4-9)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-10)
- Pin short-circuited to V_{SUP} supply (see Table 4-5 and Table 4-11)
- Pin short-circuited to V_{CCOUT} supply (see Table 4-12)
- Pin short-circuited to V_{LDO3} supply (see Table 4-6)
- Pin short-circuited to V_{IO} supply (see Table 4-7 and Table 4-13)

Table 4-2 through Table 4-11 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All conditions are within recommended operating conditions
- VSUP = see recommended conditions in device datasheet
- VIO = 1.7 to 5.5 V

4.1 TCAN11623-Q1 DMT Package

Figure 4-1 shows the TCAN11623-Q1 pin diagram for the DMT package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCAN11623-Q1 data sheet.

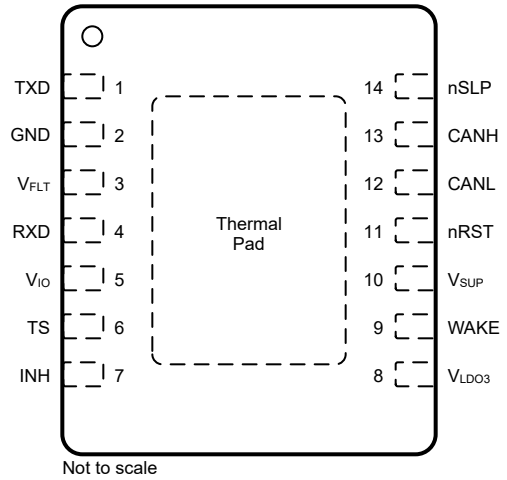


Figure 4-1. Pin Diagram (TCAN11623-Q1 DMT) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Device will enter dominant timeout mode. Unable to transmit data from processor to CAN bus	B
GND	2	None	D
V_{FLT}	3	Internal power rail held to ground, which results in unpowered device and high I_{SUP} current. No communication with device or CAN bus possible	B
RXD	4	Transceiver output biased dominant. Unable to send data from CAN bus to processor	B
V_{IO}	5	Digital pins unpowered, high I_{IO} current. No communication between device and processor possible	B
TS	6	Transceiver status output held at ground. Unable to signal ready transceiver to processor	B
INH	7	INH will not function, excessive V_{SUP} current and not able to perform power enable function	B
V_{LDO3}	8	Shorting LDO output to ground could cause device to enter thermal shutdown due to short circuit current.	B
WAKE	9	Will not be able to transition to high, which will not allow device to recognize a local wake up function	B
V_{SUP}	10	Device unpowered, high I_{SUP} current	B
nRST	11	Device held in reset. No communication with device or CAN bus possible	B
CANL	12	$V_{O(REC)}$ spec violated. Degraded EMC performance	C
CANH	13	Device cannot drive dominant to the bus, no communication possible	B
nSLP	14	Part held in sleep mode. Part will not wake up, resulting in CAN bus communication failure	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Unable to trtansmit data from processor to CAN bus	B
GND	2	Device is unpowered	B
V_{FLT}	3	Degraded EMC performance due to no capacitance	C
RXD	4	Unable to send data from CAN bus to processor	B
V_{IO}	5	Digital pins unpowered. No communication between device and processor possible	B
TS	6	Transceiver status output held at ground. Unable to signal ready transceiver to processor	B
INH	7	INH will not be able to perform system power enable functrion	B
V_{LDO3}	8	Open circuit on LDO could cause devices relying on this 3.3 V supply to go unpowered	B
WAKE	9	Will not be able to transition, which will not allow device to recognize a local wake up function	B
V_{SUP}	10	Device is unpowered	B
nRST	11	Processor will be unable to reset the device.	B
CANL	12	Device cannot drive dominant to the bus, unable to communicate	B
CANH	13	Device cannot drive dominant to the bus, unable to communicate	B
nSLP	14	Processor will be unable to put the device into low-power sleep mode	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	GND	Device will enter dominant time out mode. Unable to transmit data from processor to CAN bus	B
GND	2	V_{FLT}	Internal power rail held to ground, which results in unpowered device and high I_{SUP} current. No communication with device or CAN bus possible.	B
V_{FLT}	3	RXD	RXD output biased recessive, unable to communication bus data to processor	B
RXD	4	V_{IO}	RXD output biased recessive, unable to communication bus data to processor	B
V_{IO}	5	TS	Transceiver status output held at V_{IO}. Unable to signal ready transceiver to processor	B
TS	6	INH	Absolute maximum violation, pin may be damaged. Unable to communicate from transceiver status to processor	A
V_{LDO3}	8	WAKE	Device will wake itself when transitioned to sleep mode, as supply is powered down.	B
WAKE	9	V_{SUP}	Absolute maximum violation, WAKE pin may be damaged	A
V_{SUP}	10	nRST	Absolute maximum violation, nRST pin may be damaged	A
nRST	11	CANL	Device would be reset every time bus is dominant. No communication possible	B
CANL	12	CANH	Bus biased recessive, no communication possible. I_{OS} current may be reached on CANH/CANL	B
CANH	13	nSLP	Device could be put to sleep when bus is recessive. No communication possible	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{SUP} supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Absolute maximum violation, pin may be damaged. Unable to communicate from processor to CAN bus	A
GND	2	Device unpowered, high I_{SUP} current, may damage device	A
V_{FLT}	3	Absolute maximum violation, device may be damaged.	A
RXD	4	Absolute maximum violation, pin may be damaged. Unable to communicate from CAN bus to processor	A
V_{IO}	5	Absolute maximum violation, pin may be damaged.	A
TS	6	Absolute maximum violation, pin may be damaged.	A
INH	7	INH will be biased on and will not be able to turn off	B
V_{LDO3}	8	Absolute maximum violation, device may be damaged.	A
WAKE	9	Processor will be unable to toggle wake pin. No local wake possible.	B
V_{SUP}	10	None	D
nRST	11	Absolute maximum violation, pin may be damaged.	A
CANL	12	RXD biased recessive, no communication from CAN bus to processor possible. I_{OS} current may be reached	B
CANH	13	$V_{O(REC)}$ spec violated. May degrade EMC performance	C
nSLP	14	Absolute maximum violation, pin may be damaged.	A

Table 4-6. Pin FMA for Device Pins Short-Circuited to V_{LDO3} supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD will be held high, no communication from processor to CAN bus possible	B
GND	2	Device unpowered, high V_{LDO3} current, may enter thermal shutdown	B
V_{FLTR}	3	Excessive current from internal rail, may enter thermal shutdown	B
RXD	4	RXD will be held high, no communication from CAN bus to processor possible	B
V_{IO}	5	Potential for high V_{CCOUT} current, may enter thermal shutdown	B
TS	6	Held high, unable to signal transceiver state to processor	B
INH	7	Absolute maximum violation, device may be damaged	A
V_{LDO3}	8	None	D
WAKE	9	Processor will be unable to toggle wake pin. No local wake possible	B
V_{SUP}	10	Absolute maximum violation, device may be damaged	A
nRST	11	Held high, unable to reset processor	B
CANL	12	RXD biased recessive, no communication from CAN bus to processor possible. I_{OS} current may be reached	B
CANH	13	$V_{O(REC)}$ spec violated. May degrade EMC performance	C
nSLP	14	Held high, unable to put device to sleep	B

Table 4-7. Pin FMA for Device Pins Short-Circuited to V_{IO} supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD will be held high, no communication from processor to CAN bus possible	B
GND	2	Device unpowered, communication not possible	B
V_{FLTR}	3	Excessive current from internal rail, may enter thermal shutdown	B
RXD	4	RXD will be held high, no communication from CAN bus to processor possible	B
V_{IO}	5	None	D
TS	6	Held high, unable to signal transceiver state to processor	B
INH	7	Absolute maximum violation, device may be damaged	A
V_{LDO3}	8	Excessive current from V_{LDO3}, may enter thermal shutdown	B
WAKE	9	Processor will be unable to toggle wake pin. No local wake possible	B
V_{SUP}	10	Absolute maximum violation, device may be damaged	A
nRST	11	Held high, unable to reset processor	B
CANL	12	RXD biased recessive, no communication from CAN bus to processor possible. I_{OS} current may be reached	B
CANH	13	$V_{O(REC)}$ spec violated. May degrade EMC performance	C
nSLP	14	Held high, unable to put device to sleep	B

4.2 TCAN11625-Q1 DMT Package

Figure 4-2 shows the TCAN11625-Q1 pin diagram for the DMT package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCAN11625-Q1 data sheet.

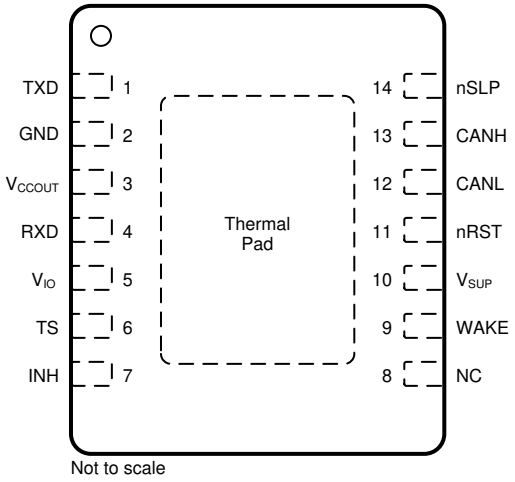


Figure 4-2. Pin Diagram (TCAN11625-Q1 DMT Package)

Table 4-8. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Device will enter dominant timeout mode. Unable to transmit data from processor to CAN bus	B
GND	2	None	D
V_{CCOUT}	3	Internal power rail held to ground, which results in unpowered device and high I_{SUP} current. No communication with device or CAN bus possible	B
RXD	4	Transceiver output biased dominant. Unable to send data from CAN bus to processor	B
V_{IO}	5	Digital pins unpowered, high I_{IO} current. No communication between device and processor possible	B
TS	6	Transceiver status output held at ground. Unable to signal ready transceiver to processor	B
INH	7	INH will not function, excessive V_{SUP} current and not able to perform power enable function	B
NC	8	This pin should be left floating or pulled to ground	D
WAKE	9	Will not be able to transition to high, which will not allow device to recognize a local wake up function	B
V_{SUP}	10	Device unpowered, high I_{SUP} current	B
nRST	11	Device held in reset. No communication with device or CAN bus possible	B
CANL	12	$V_{O(REC)}$ spec violated. Degraded EMC performance	C
CANH	13	Device cannot drive dominant to the bus, no communication possible	B
nSLP	14	Part held in sleep mode. Part will not wake up, resulting in CAN bus communication failure	B

Table 4-9. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Unable to trtansmit data from processor to CAN bus	B
GND	2	Device is unpowered	B
V_{CCOUT}	3	Degraded EMC performance due to no capacitance	C
RXD	4	Unable to send data from CAN bus to processor	B
V_{IO}	5	Digital pins unpowered. No communication between device and processor possible	B
TS	6	Transceiver status output held at ground. Unable to signal ready transceiver to processor	B
INH	7	INH will not be able to perform system power enable functrion	B
NC	8	This pin should be left floating or connected to ground	D
WAKE	9	Will not be able to transition, which will not allow device to recognize a local wake up function	B
V_{SUP}	10	Device is unpowered	B
nRST	11	Processor will be unable to reset the device.	B
CANL	12	Device cannot drive dominant to the bus, unable to communicate	B
CANH	13	Device cannot drive dominant to the bus, unable to communicate	B
nSLP	14	Processor will be unable to put the device into low-power sleep mode	B

Table 4-10. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	GND	Device will enter dominant time out mode. Unable to transmit data from processor to CAN bus	B
GND	2	V_{CCOUT}	Internal power rail held to ground, which results in unpowered device and high I_{SUP} current. No communication with device or CAN bus possible.	B
V_{CCOUT}	3	RXD	RXD output biased recessive, unable to communication bus data to processor	B
RXD	4	V_{IO}	RXD output biased recessive, unable to communication bus data to processor	B
V_{IO}	5	TS	Transceiver status output held at V_{IO}. Unable to signal ready transceiver to processor	B
TS	6	INH	Absolute maximum violation, pin may be damaged. Unable to communicate from transceiver status to processor	A
NC	8	WAKE	Absolute maximum violation on the NC pin, possible damage or unexpected behavior of device	A
WAKE	9	V_{SUP}	Absolute maximum violation, WAKE pin may be damaged	A
V_{SUP}	10	nRST	Absolute maximum violation, nRST pin may be damaged	A
nRST	11	CANL	Device would be reset every time bus is dominant. No communication possible	B
CANL	12	CANH	Bus biased recessive, no communication possible. I_{OS} current may be reached on CANH/CANL	B
CANH	13	nSLP	Device could be put to sleep when bus is recessive. No communication possible	B

Table 4-11. Pin FMA for Device Pins Short-Circuited to V_{SUP} supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Absolute maximum violation, pin may be damaged. Unable to communicate from processor to CAN bus	A
GND	2	Device unpowered, high I_{SUP} current, may damage device	A
V_{CCOUT}	3	Absolute maximum violation, device may be damaged	A
RXD	4	Absolute maximum violation, pin may be damaged. Unable to communicate from CAN bus to processor	A
V_{IO}	5	Absolute maximum violation, pin may be damaged	A
TS	6	Absolute maximum violation, pin may be damaged	A
INH	7	INH will be biased on and will not be able to turn off	B
NC	8	Absolute maximum violation on the NC pin, possible damage or unexpected behavior of device	A
WAKE	9	Processor will be unable to toggle wake pin. No local wake possible	B
V_{SUP}	10	None	D
nRST	11	Absolute maximum violation, pin may be damaged	A
CANL	12	RXD biased recessive, no communication from CAN bus to processor possible. I_{OS} current may be reached	B
CANH	13	$V_{O(REC)}$ spec violated. May degrade EMC performance	C
nSLP	14	Absolute maximum violation, pin may be damaged	A

Table 4-12. Pin FMA for Device Pins Short-Circuited to V_{CCOUT} supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD will be held high, no communication from processor to CAN bus possible	B
GND	2	Device unpowered, high V_{CCOUT} current, may enter thermal shutdown	B
V_{CCOUT}	3	None	D
RXD	4	RXD will be held high, no communication from CAN bus to processor possible	B
V_{IO}	5	Potential for high V_{CCOUT} current, may enter thermal shutdown	B
TS	6	Held high, unable to signal transceiver state to processor	B
INH	7	Absolute maximum violation, device may be damaged	A
NC	8	Pin not held at ground or floating, possible unexpected behavior of device	B
WAKE	9	Processor will be unable to toggle wake pin. No local wake possible	B
V_{SUP}	10	Absolute maximum violation, device may be damaged	A
nRST	11	Held high, unable to reset processor	B
CANL	12	RXD biased recessive, no communication from CAN bus to processor possible. I_{OS} current may be reached	B
CANH	13	$V_{O(REC)}$ spec violated. May degrade EMC performance	C
nSLP	14	Held high, unable to put device to sleep	B

Table 4-13. Pin FMA for Device Pins Short-Circuited to V_{IO} supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD will be held high, no communication from processor to CAN bus possible	B
GND	2	Device unpowered, communication not possible	B
V_{CCOUT}	3	Potential for high V_{CCOUT} current, may enter thermal shutdown	B
RXD	4	RXD will be held high, no communication from CAN bus to processor possible	B
V_{IO}	5	None	D
TS	6	Held high, unable to signal transceiver state to processor	B
INH	7	Absolute maximum violation, device may be damaged	A
NC	8	Pin not held at ground or floating, possible unexpected behavior of device	B
WAKE	9	Processor will be unable to toggle wake pin. No local wake possible	B
V_{SUP}	10	Absolute maximum violation, device may be damaged	A
nRST	11	Held high, unable to reset processor	B
CANL	12	RXD biased recessive, no communication from CAN bus to processor possible. I_{OS} current may be reached	B
CANH	13	$V_{O(REC)}$ spec violated. May degrade EMC performance	C
nSLP	14	Held high, unable to put device to sleep	B

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