*Functional Safety Information*

# *ISO6720/ISO6720-Q1 Functional Safety FIT Rate, FMD and Pin FMA*

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# 1 Overview

This document contains information for ISO6720/ISO6720-Q1 and ISO6720F/ISO6720F-Q1 (8-D and 8-DWV package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the functional block diagram of one channel of ISO6720/ISO6720-Q1 and ISO6720F/ISO6720F-Q1 for reference.

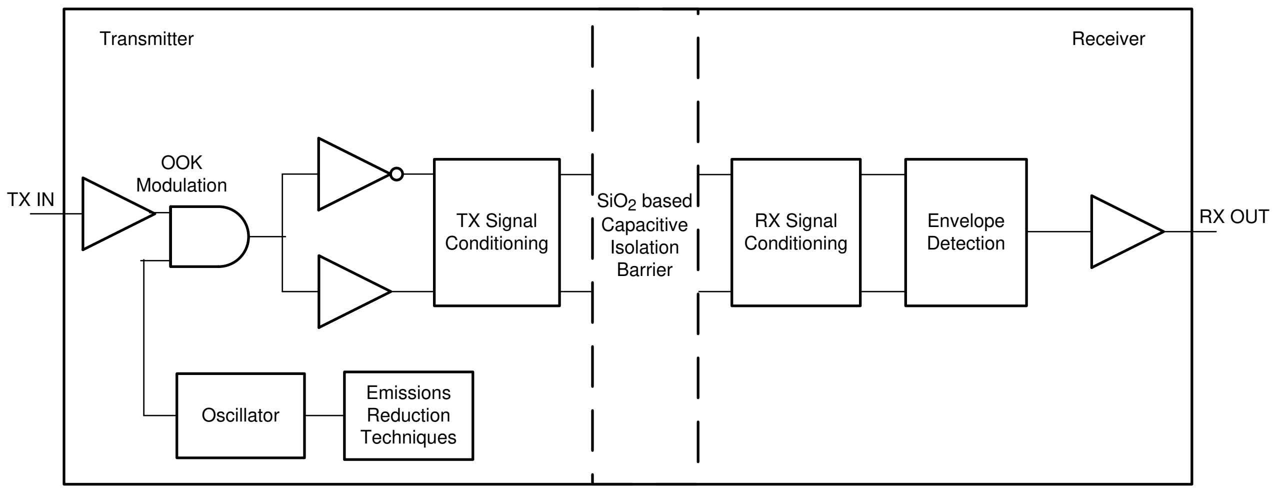


**Figure 1-1. Functional Block Diagram**

ISO6720/ISO6720-Q1 and ISO6720F/ISO6720F-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

# 2 Functional Safety Failure In Time (FIT) Rates

## 2.1 8-D (narrow body SOIC) Package

This section provides Functional Safety Failure In Time (FIT) rates for 8-D package of ISO6720/ISO6720-Q1 and ISO6720F/ISO6720F-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 10 |
| Die FIT Rate | 3 |
| Package FIT Rate | 7 |

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog / mixed | 25 FIT | 55 °C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

## 2.2 8-SOIC (wide-body SOIC) Package

This section provides Functional Safety Failure In Time (FIT) rates for the 8-DWV package of ISO6720/ISO6720-Q1 and ISO6720F/ISO6720F-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 16 |
| Die FIT Rate | 2 |
| Package FIT Rate | 14 |

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog / mixed | 25 FIT | 55°C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ISO6720/ISO6720-Q1 and ISO6720F/ISO6720F-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| OUT state undetermined | 35% |
| OUT not in timing or voltage specification | 30% |
| OUT stuck to default state | 25% |
| OUT stuck high | 5% |
| OUT stuck low | 5% |

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ISO6720/ISO6720-Q1 and ISO6720F/ ISO6720F-Q1 (8-D and 8-DWV package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1. Note that when pin short to ground case is discussed, only same side ground shorts are considered.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

## 4.1 8-D (narrow-body SOIC) and 8-DWV (wide-body SOIC) Package

Figure 4-1 shows the ISO6720/ISO6720-Q1 and ISO6720F/ISO6720F-Q1 pin diagram for the 8-D and 8-DWV packages. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ISO6720/ISO6720-Q1 data sheet.

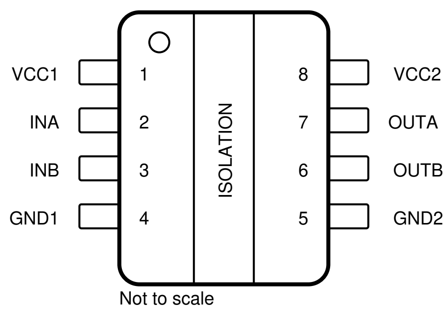


**Figure 4-1. Pin Diagram (8-D and 8-DWV) Package**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $V_{CC1}$ | 1 | No power to the device on side-1. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage may be plausible. | A |
| INA | 2 | Input signal shorted to ground, so output (OUTA) stuck to low. Communication from INA to OUTA corrupted. | B |
| INB | 3 | Input signal shorted to ground, so output (OUTB) stuck to low. Communication from INB to OUTB corrupted. | B |
| GND1 | 4 | Device continues to function as expected. Normal operation. | D |
| GND2 | 5 | Device continues to function as expected. Normal operation. | D |
| OUTB | 6 | OUTB stuck low. Data communication from INB to OUTB lost. Device damage possible if INB is driven high for extended period of time. | A |
| OUTA | 7 | OUTA stuck low. Data communication from INA to OUTA lost. Device damage possible if INA is driven high for extended period of time. | A |
| $V_{CC2}$ | 8 | No power to the device on side-2. OUTA/OUTB pins state undetermined. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $V_{CC1}$ | 1 | Operation undetermined. Either device is unpowered and OUTA/OUTB=default logic state or through internal ESD diode on any IN pin, device can power up if any IN is driven to logic high. If IN pin has current sourcing capability to provide regular operating current of device, ESD diode conducts that current and device damage possible. | A |
| INA | 2 | No communication to INA channel possible. OUTA stuck to default state (High for ISO6720/ ISO6720-Q1 and Low for ISO6720F/ISO6720F-Q1). | B |
| INB | 3 | No communication to INB channel possible. OUTB stuck to default state (High for ISO6720/ ISO6720-Q1 and Low for ISO6720F/ISO6720F-Q1). | B |
| GND1 | 4 | Device unpowered on side1. OUTA/OUTB go to default state (High for ISO6720/ISO6720-Q1 and Low for ISO6720F/ISO6720F-Q1). | B |
| GND2 | 5 | Device unpowered on side-2. OUTA/OUTB state undetermined. | B |
| OUTB | 6 | State of OUTB undetermined. Data communication from INB to OUTB lost. | B |
| OUTA | 7 | State of OUTA undetermined. Data communication from INA to OUTA lost. | B |
| $V_{CC2}$ | 8 | Device unpowered on side-2 and state of OUTA/OUTB undetermined. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| $V_{CC1}$ | 1 | INA | INA stuck high. External bit-stream for communication to INA pin corrupted. OUTA stuck high. | B |
| INA | 2 | INB | Communication corrupted for either INA or INB channel. | B |
| INB | 3 | GND1 | Input signal shorted to ground, so output (OUTB) stuck to low. Communication from INB to OUTB corrupted. | B |
| GND1 | 4 | INB | Already considered in above row. | B |
| GND2 | 5 | OUTB | OUTB pin stuck low. Communication corrupted. If IN pin is driven high for extended duration, OUTB pin stuck low creates a short between supply and ground with possible device damage. | A |
| OUTB | 6 | OUTA | Communication corrupted for either OUTA or OUTB channel. Device damage possible if INA and INB try to drive opposite logic state for extended duration creating a short between supply and ground on side-2. | A |
| OUTA | 7 | $V_{CC2}$ | OUTA stuck high. Data communication from INA to OUTA lost. Device damage possible if INA is driven low for extended period of time. | A |
| $V_{CC2}$ | 8 | OUTA | Already considered in above row. | A |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $V_{CC1}$ | 1 | No effect. Normal operation. | D |
| INA | 2 | INA pin stuck high. Communication corrupted. OUTA stuck high. | B |
| INB | 3 | INB pin stuck high. Communication corrupted. OUTB stuck high. | B |
| GND1 | 4 | Device side-1 unpowered. Observe that the absolute maximum ratings for INA/INB pins of the device are met, otherwise device damage may be plausible. | A |
| GND2 | 5 | Device side-2 unpowered. OUTA/OUTB state undetermined. | B |
| OUTB | 6 | OUTB stuck high. Communication disrupted. If INB is low for extended duration, OUTB being stuck high creates a short and can damage the device. | A |
| OUTA | 7 | OUTA stuck high. Communication disrupted. If INA is low for extended duration, OUTA being stuck high creates a short and can damage the device. | A |
| $V_{CC2}$ | 8 | No effect. Normal operation. | D |

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| Month Year | * | Initial Release |