Functional Safety Information

TPS3702

Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS3702 (DDC package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

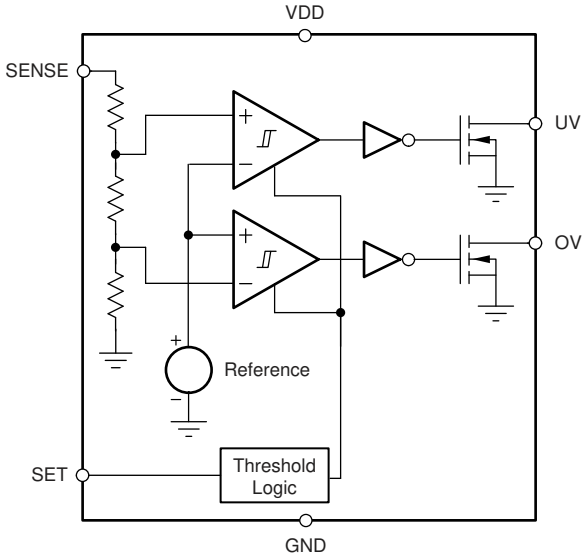

Figure 1-1. Functional Block Diagram

TPS3702 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS3702 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	4
Die FIT Rate	2
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 6 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS3702 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
UV or OV output HiZ	30%
UV or OV output stuck low	30%
UV or OV output operating outside of specification	40%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS3702. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDD (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS3702 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS3702 data sheet.

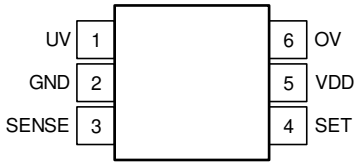

Figure 4-1. DDC Package SOT-6 Top View

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Unless otherwise specified, it is assumed that the voltages applied to all the pins are within the Recommended Operating Range specified in the TPS3702 data sheet.
- Note that the SET and the SENSE pin have lower maximum operating range than VDD and UV/OV.
- For shorts to VDD, this document assumes the SET and SENSE pin maximum is not exceeded.
- Refer to *Typical Application Circuit* diagram in the datasheet for test layout.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
UV	1	No damage to device, undervoltage output pin nonfunctional, increase in system current.	B
GND	2	No effect.	D
SENSE	3	No damage to device, Undervoltage output always active, Overvoltage output always inactive.	B
OV	4	No damage to device, Overvoltage output pin nonfunctional, increase in system current.	B
VDD	5	No damage to device, but device is unpowered. Device is nonfunctional.	B
SET	6	No damage to device, wide thresholds selected.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
UV	1	No damage to device, undervoltage output pin nonfunctional.	B
GND	2	No damage to device, but device is unpowered. Device is nonfunctional.	B
SENSE	3	No damage to device. Due to internal resistor ladder for setting trip points open SENSE pin behaves as though GND potential - Undervoltage output always active, Overvoltage output always inactive.	B
OV	4	No damage to device, overvoltage output pin nonfunctional.	B
VDD	5	No damage to device, but device is unpowered. Device is nonfunctional.	B
SET	6	No damage to device. Due to internal pull up on SET pin it behaves as if connected to VDD - narrow thresholds selected.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
UV	1	GND	No damage to device, undervoltage output pin nonfunctional, increase in system current.	B
GND	2	SENSE	No damage to device, Undervoltage output always active, Overvoltage output always inactive.	B
SENSE	3	SET	Since SET VIH = 750mV and all SENSE thresholds >1V, SENSE = SET means always narrow threshold tolerances selected.	B
OV	4	UV	No damage to device, but device is nonfunctional with both outputs tied together, can't distinguish OV from UV.	B
VDD	5	OV	No damage to device, overvoltage output pin nonfunctional.	B
SET	6	VDD	No damage to device, narrow thresholds selected.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
UV	1	No damage to device, undervoltage output pin nonfunctional.	B
GND	2	No damage to device, but device is unpowered. Device is nonfunctional.	B
SENSE	3	No damage to device, Undervoltage output always inactive, Overvoltage output always active.	B
OV	4	No damage to device, overvoltage output pin nonfunctional.	B
VDD	5	No effect.	D
SET	6	No damage to device, narrow thresholds selected.	B

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