Functional Safety Information

LMR34215-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for LMR34215-Q1 (VQFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

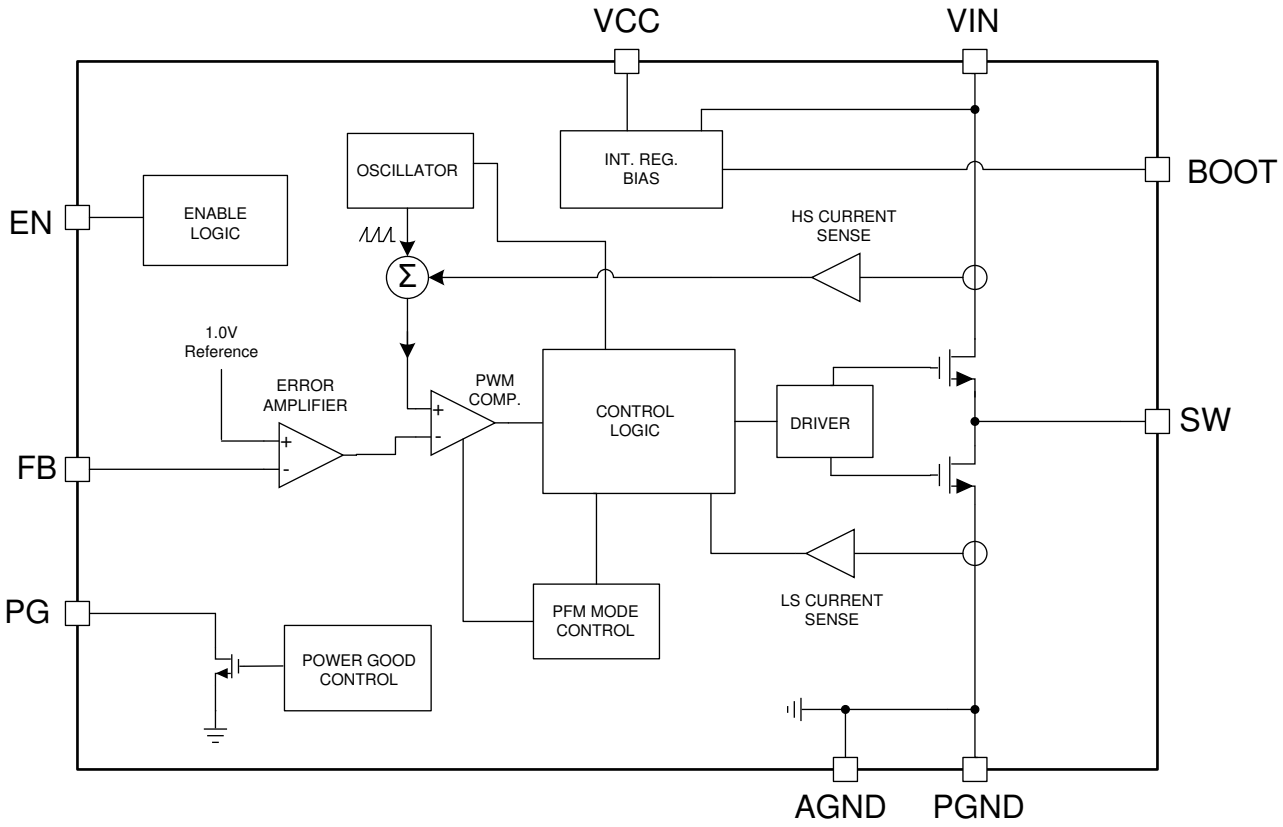

Figure 1-1. Functional Block Diagram

LMR34215-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LMR34215-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	13
Die FIT Rate	9
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR34215-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	35%
SW output not in specification – voltage or timing	45%
SW driver FET stuck on	10%
PG false trip or fails to trip	5%
Short circuit any two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LMR34215-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LMR34215-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMR34215-Q1 data sheet.

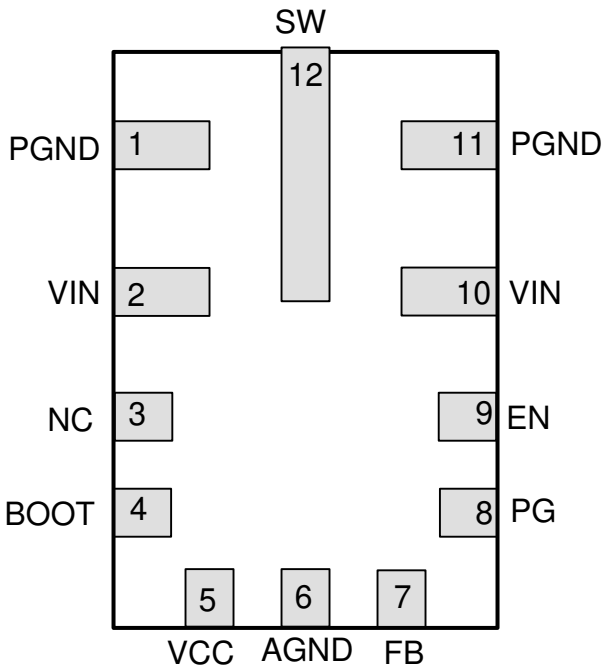

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the LMR36015-Q1 data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1,11	This is the ground pin, no effect.	D
VIN	2,10	No output voltage will be generated. Possible damage to customer input supply, PCB can occur unless customer provides protection, or both. Reverse current from the SW pin to VIN pin, due to discharge of output capacitors, can damage regulator.	B
N/C	3	No connection when it is NOT used for SW to BOOT connection	D
		When used for SW to BOOT connection, as recommended, the effect is the same as for pin SW (12).	A
BOOT	4	Driver supply to high side MOSFET will be lost. Output voltage will not be regulated. Possible damage to internal regulator and Cboot charging circuit.	A
VCC	5	Internal circuits will be disabled. No output voltage will be generated. Possible increase in input current and possible damage to internal LDO.	A
AGND	6	This is the ground pin, no effect.	D
FB	7	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage level. Possible damage to customer load, output stage components can occur, or both.	D
PG	8	This is a valid connection for the PG output. PG functionality will be lost. Damage to customer components connected to PG input can occur.	D
EN	9	This is a valid connection for the EN input. Enable functionality will be lost; the device will remain off with no output voltage generated. Damage to customer components connected to EN input can occur.	B
SW	12	Shorting the SW pin to ground will result in large currents through the device and subsequent damage. No output voltage will be produced.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1,11	Erratic operation; probable loss of regulation. Possible output voltage increase and damage to customer load	B
VIN	2,11	Loss of output voltage	B
N/C	3	No connection when it is NOT used for SW to BOOT connection.	D
		When used for SW to BOOT connection, as recommended, the effect is the same as for pin BOOT (4).	B
BOOT	4	Driver supply to high side MOSFET will be lost. Output voltage will not be regulated. Low or no output voltage; erratic switching behavior	B
VCC	5	Internal LDO may oscillate. VCC voltage will not be stable. Internal circuits will not function correctly. Output voltage may not be regulated.	B
AGND	6	Erratic operation; probable loss of regulation. Possible output voltage increase and damage to customer load	B
FB	7	Device will not regulate. Output voltage can rise or fall. Damage to customer load, output stage components is probable, or both.	B
PG	8	This is a valid connection for the PG output. PG functionality will be lost.	B
EN	9	Loss of enable functionality. Erratic operation; probable loss of regulation	B
SW	12	Loss of output voltage	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	VIN	No output voltage will be generated. Possible damage to customer input supply, PCB can occur unless customer provides protection, or both. Reverse current from the SW pin to VIN pin, due to discharge of output capacitors, can damage the regulator.	B
VIN	2	N/C	No connection when NOT used for SW to BOOT connection.	D
			When used for SW to BOOT connection, as recommended, the output voltage will rise to the level of VIN. Customer load will be damaged.	B
N/C	3	BOOT	No connection, when NOT used for SW to BOOT connection.	D
			When used for SW to BOOT connection, as recommended, large currents will flow through internal circuits. Possible damage to internal regulator and CBOOT charging circuits. No output voltage will be produced.	A
BOOT	4	VCC	Damage to VCC regulator, other internal circuits, or both. Output voltage can be affected.	A
VCC	5	AGND	Internal circuits will be disabled. No output voltage will be generated. Possible increase in input current and possible damage to internal LDO	A
AGND	6	FB	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage level. Possible damage to customer load, output stage components can occur, or both.	B
FB	7	PG	Erratic operation; probable loss of regulation. Possible output voltage increase and damage to customer load	B
PG	8	EN	Erratic operation; probable loss of regulation. Possible damage to customer circuits connected to these pins	B
EN	9	VIN	This is a valid connection for the EN input. Enable functionality will be lost; the device will remain on. Damage to customer components connected to EN input can occur.	D
VIN	10	PGND	No output voltage will be generated. Possible damage to customer input supply, PCB can occur unless customer provides protection, or both. Reverse current from SW pin to VIN pin, due to discharge of output capacitors, can damage the regulator.	B
PGND	11	SW	Shorting the SW pin to ground will result in large currents through the device and subsequent damage. No output voltage will be produced.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1,11	VOUT = 0 V. Damage to low-side circuitry if PGND >> AGND	A
VIN	2,10	Normal operation	D
N/C	3	Normal operation when NOT used for SW to BOOT connection	D
		Damage to LS FET when used for SW to BOOT connection as recommended.	A
BOOT	4	VOUT = 0 V. CBOOT ESD clamp will run current to destruction.	A
VCC	5	If VIN exceeds 5.5 V, damage will occur.	A
AGND	6	VOUT = 0 V. Damage to other pins referred to GND.	A
FB	7	If VIN exceeds 16 V, damage will occur. VOUT = 0 V.	A
PG	8	PGOOD ESD clamp will run current to destruction	A
EN	9	Normal operation	D
SW	12	Damage to LS FET	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265