Application Brief

Optimizing String Inverter Systems Using Logic and Translation

Functional Block Diagram

For the purpose of this report, a simplified string inverter block diagram is used to illustrate the logic and translation use cases, see Figure 1. Each red block has an associated use-case document. Links are provided in Table 1 and Table 2. For a more complete block diagram, see the interactive online end equipment reference diagram for string inverters.

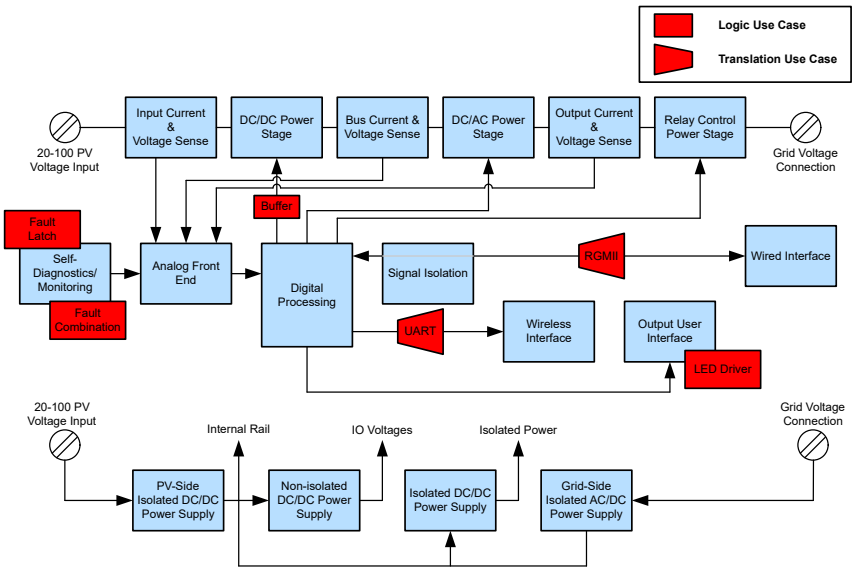

Figure 1. Simplified Block Diagram for String Inverters

Logic and Translation Use Cases

Each use case is linked to a separate short document that provides additional details including a block diagram, design tips, and part recommendations. The nearest block and use-case identifiers are listed to match up exactly to the use cases shown in the provided *simplified block diagram*.

Table 1. Logic Use Cases

Nearest Block	Use-Case Identifier	Use Case
Self-Diagnostics/Monitoring	Fault Latch	*Catch a Digital Pulse* *Multiple Fault Monitoring*
	Fault Combination	*Use Fewer Inputs to Monitor Error Signals*
Digital Processing	Buffer	*Redrive Digital Signals*
Output User Interface	LED Driver	*Drive Indicator LEDs*

Table 2. Translation Use Cases

Nearest Block	Use-Case Identifier	Use Case
Wireless Interface	UART	*Translate Voltages for UART*
Wired Interface	RGMII	*Translate Voltages for RGMII*

Multiple Fault Monitoring

It is common to see string inverters utilizing multiple sensors that could indicate fault conditions. Each fault signal can be individually monitored utilizing individual pins of a system controller; however, another approach is to utilize a combination of digital latches and a shift register to reduce the number of system controller pins required to monitor for issues. This has the added advantage that the controller can only occasionally poll for errors and will not miss anything due to the added latches.

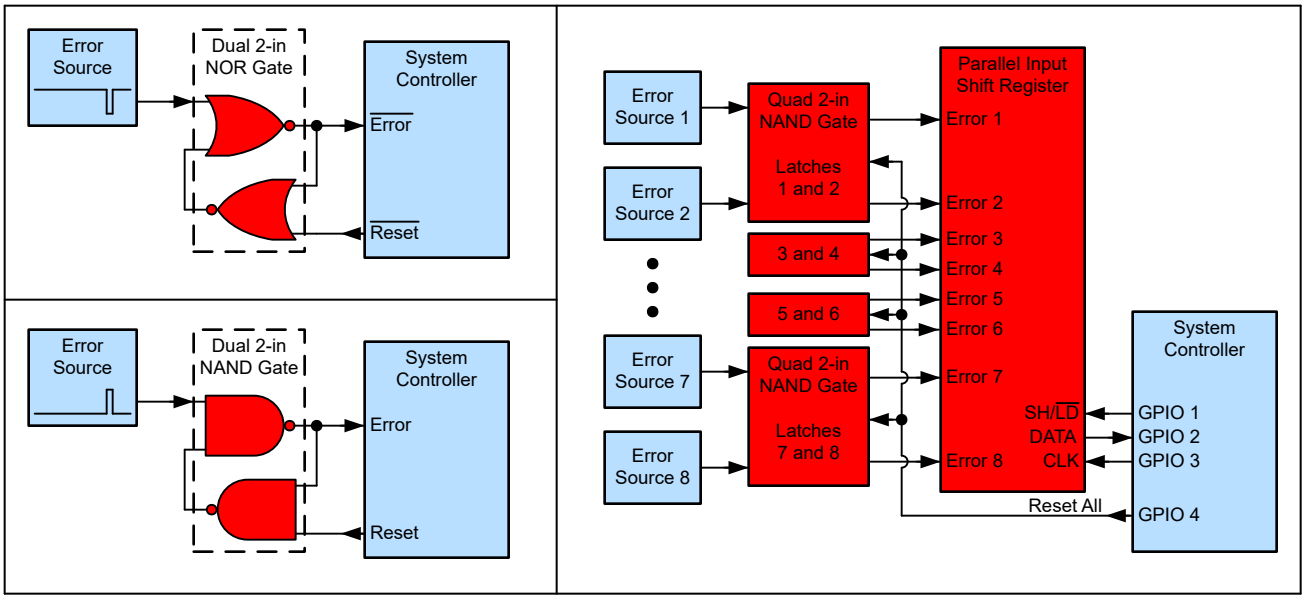

Figure 2. [Left top] Single Negative Pulse Latch, [Left bottom] Single Positive Pulse Latch, [Right] Monitoring Multiple Latches Using Parallel-Input Shift Register to Reduce Controller Pin Count

See more about similar use cases in the *Logic Minute* videos *Design an Alarm / Tamper Circuit with an S-R Latch* and *Increase the Number of Inputs on a Microcontroller*.

- Dedicated logic latches catch even extremely short events that could otherwise be missed by the controller
- Positive and negative latches can be combined as needed depending on the output of the sensor
- Eight or more sensors can be monitored by utilizing only 4 GPIO pins
- Ensure that all input signals are digital; use comparators or Schmitt-trigger buffers to convert analog signals
- [FAQ] How does a slow or floating input affect a CMOS device?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

Table 3. Recommended Parts

Part Number	Automotive Qualified	Operating Voltage Range	Features
SN74AUP2G00		0.8 V to 3.6 V	AUP family logic devices are extremely low power; I_{CC} < 0.9 µA One latch per device (2 × 2-input gates) ('00) NAND-based positive pulse detectors ('02) NOR-based negative pulse detectors
SN74AUP2G02			

Table 3. Recommended Parts (continued)

Part Number	Automotive Qualified	Operating Voltage Range	Features
SN74HCS00-Q1	✓	2 V to 6 V	HCS family logic has integrated Schmitt-trigger inputs allowing for slow input signals
SN74HCS00			Up to two latches per device (4 × 2-input gates)
SN74HCS02-Q1	✓		Low power consumption - I_{CC} < 2 µA
SN74HCS02			('00) NAND-based positive pulse detectors
SN74HCS165-Q1	✓		('02) NOR-based negative pulse detectors
SN74HCS165			('165) Parallel-input shift registers increase the number of inputs; can be daisy-chained for 16+ inputs from only 4 GPIO pins

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265