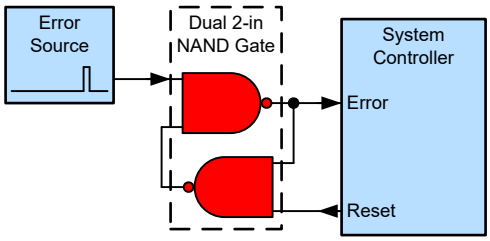
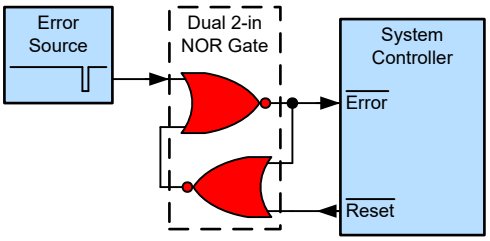
Product Overview

Catch a Digital Pulse

An error condition or other digital input might only occur for a very short time while the processor is busy with other tasks or asleep for power savings. In order to ensure that an error state is correctly identified, a dedicated latch circuit can be used to catch even very brief pulses while using very little power.



Single Positive Pulse Latch



Single Negative Pulse Latch

See more about similar use cases in the *Logic Minute* video *Design an Alarm / Tamper Circuit with an S-R Latch*.

Design Considerations

- Ensure that the error signal is digital; analog signals should be converted using a comparator
- Reset latches on system startup; latch circuits do not have a default value
- *[FAQ] What is the default output of a latched device? (Flip-Flop, latch, register)*
- *[FAQ] How does a slow or floating input affect a CMOS device?*
- Ask a question on our *Engineer-to-Engineer forum*

Recommended Parts

Part Number	AEC-Q100	V_{CC} Range	Features
SN74AUP2G02		0.8 V – 3.6 V	Extremely low power – I_{CC} < 0.9 µA One latch per device (2 × 2-input gates)
SN74AUP2G00			
SN74HCS02-Q1	✓	2 V – 6 V	Schmitt-trigger input architecture Low power – I_{CC} < 2 µA Up to two latches per device (4 × 2-input gates)
SN74HCS02			
SN74HCS00-Q1	✓		
SN74HCS00			

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265