Application Note

Top Questions About Auto Bi-Direction LSF Family Translators

Jack Guan

ABSTRACT

The LSF Type translators utilize passive switches to level shift voltages, allowing the device to support both open drain and push pull interface signals. Board designers have the freedom to adjust the device behavior with external components to satisfy specific system needs. As a result, designing with the LSF Family requires additional attention due to specific biasing requirements, external RC component guidelines, and other design considerations.

This application note takes a deeper look into some of the most commonly asked questions regarding this device and serves as an extension to the existing app note regarding the operation of the LSF family devices. Please see Voltage Translation with the LSF Family for an introduction to how the LSF Family devices operate in example applications.

Table of Contents

1 How Does the LSF000x Differentiate From the LSF010x During Setup? 2
2 How is the Internal Body Diode of the LSF NMOS Configured? 3
3 Are Pullup Resistors Required for Push-Pull Applications with the LSF? 4
4 How is Power Consumption Calculated for LSF Devices? 7
5 Can I use LDO as a Power Supply? 8
6 What if my I/Os Operate Lower Than V_{REFA}? 9
7 Summary 10
8 References 11

Trademarks

1 How Does the LSF000x Differentiate From the LSF010x During Setup?

Both variants of the LSF devices share similar architecture, but the LSF000x design requirements are less stringent than the LSF010x. The LSF000x only uses one power supply to directly bias the gates of the channel FETs to perform translation, removing the requirement to operate with two power supplies. Since LSF000x can operate with a single power supply, the device eliminates the need for V_{REFB} to be shorted to EN, as well as the external 200kΩ bias resistor. The key consideration with the LSF000x is that VBIAS must be referenced to the lower voltage of $V_{EXT,A}$ and $V_{EXT,B}$. Figure 1-1 depicts setup differences:

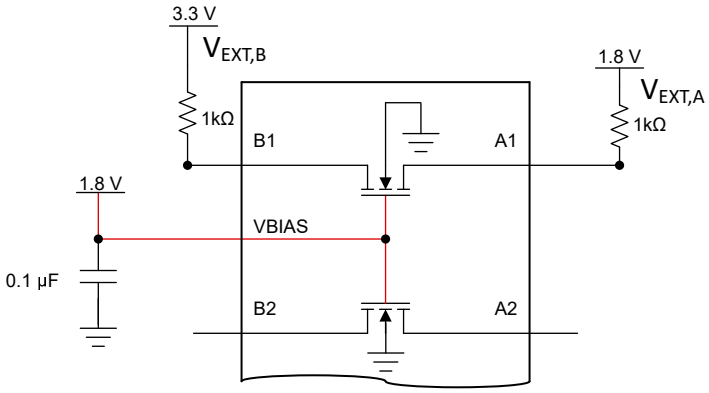

Figure 1-1. LSF000x Setup

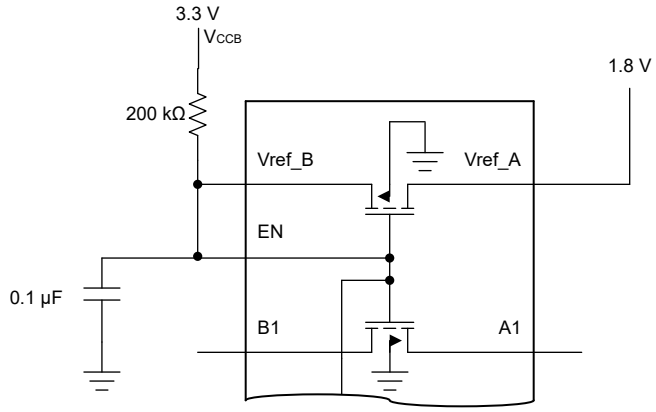

Figure 1-2. LSF010x Setup

2 How is the Internal Body Diode of the LSF NMOS Configured?

Unlike traditional FETs with a singular body diode (Figure 1-1), the LSF family translators utilize an N- channel MOSFET with two intrinsic body diodes as seen in Figure 1-2 (one connected in a body to source and one from the body to drain manner). This configuration minimizes leakage current flow from the source to the drain during level shifting operation (when the device is in cutoff mode) and when the device is disabled.

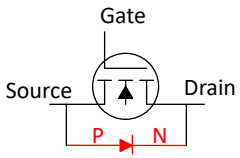

Figure 2-1. 3 Terminal NMOS

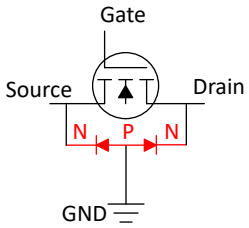

Figure 2-2. 4 Terminal NMOS

Additionally, by utilizing this structure for the internal channel FETs, both the source and the drain become interchangeable, allowing for bi-directional communication.

3 Are Pullup Resistors Required for Push-Pull Applications with the LSF?

Pullups are needed when used with open-drain interfaces to drive the bus to a logic high state since open-drain drivers are only capable of pulling the bus low. But when LSF is being used with push-pull drivers, this requirement becomes ambiguous.

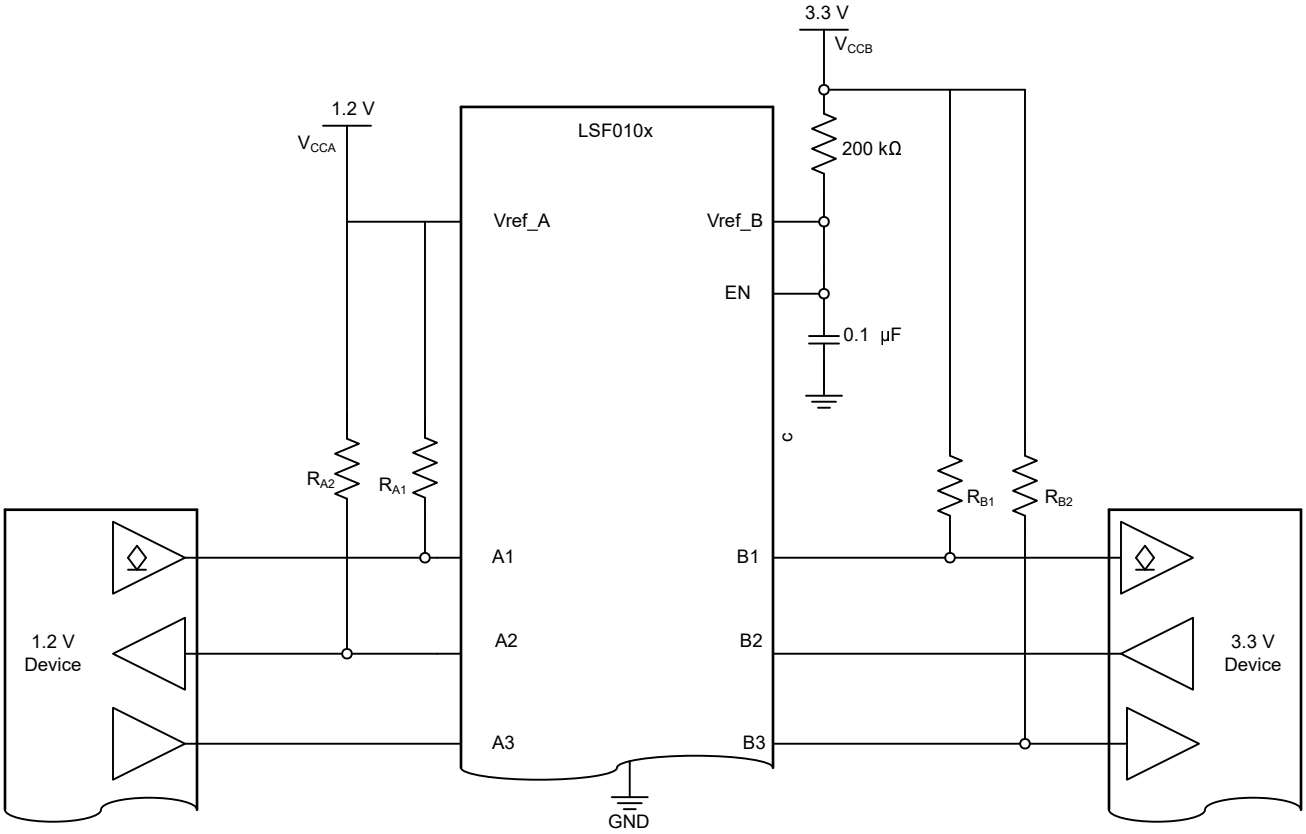

Figure 3-1. Example Schematic of LSF Used in Both Push-Pull and Open Drain Configurations

Table 3-1. Pullup Resistors Requirement with Push-Pull Drivers

	Up Translation (1.2V) → (3.3V)		Down Translation (3.3V) → (1.2V)	
Input/ Output (I/O)	A3 (I)	B3 (O)	B2 (I)	A2 (O)
Pullups Needed?	No	Recommended	No	Recommended if excessive leakage on output side, or translating to another voltage not V_{REFA}

Take an example of a down translation use case (A2/ B2 in above schematic) where pullup resistors are recommended on the output (A-side) if excessive leakage current is observed. This happens when the receiver is attempting to draw more current then the internal FET can provide during a logic high state. When this occurs, the voltage on the output side drops due to the internal FET turning on (transition to the linear region) as the source and gate voltage gap become wider (V_{GS}> V_{TH}). This in turn pulls the bus low and result in a false logic low signal for the device back upstream. To resolve this, external pullups are used to offset the leakage so that the FET can remain in the cutoff state (V_{GS}<V_{TH}) during a transmitted logic high signal. In the below Down Translation simulations, a leakage current at the output is imitated and the VOH levels are measured and compared to VOH levels if pullups were used in place.

Simulation #1: Effect of excessive leakage current on receiver side during down translation.

In Figure 3-2, we use a current source at the output side (IG1) to simulate a leakage path on the receiver side. The step function of the current at IG1 increases linearly and the voltage at the output is measured.

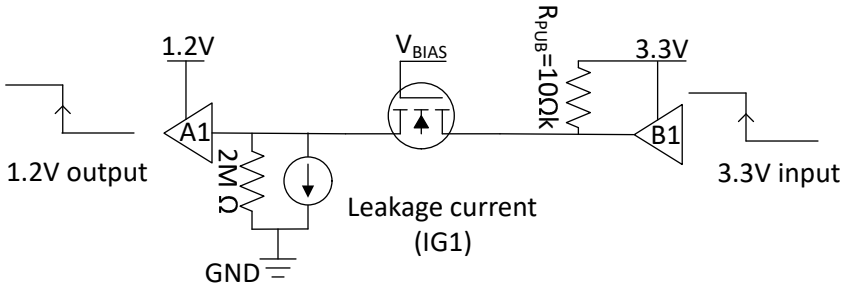

Figure 3-2. Simulation Setup With Excessive Leakage on Receiver Side

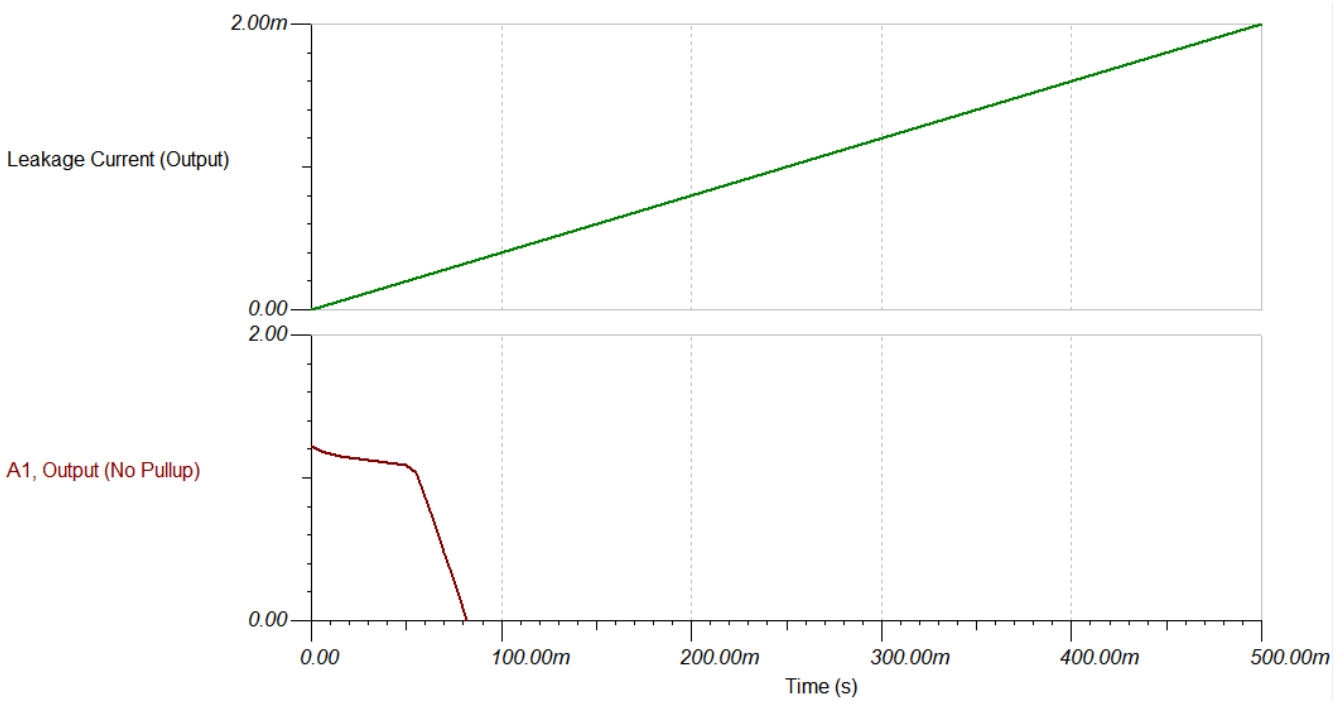

Figure 3-3. Simulation Result With Excessive Leakage on Receiver Side

As output leakage current (IG1) increased, the observed output voltage begins to sag further until the output voltage drifts below the threshold voltage. By now, the difference at the output and the gate voltage becomes large enough that the low side (A-side) becomes the source, thus the FET transitioning back into linear region. Once the FET is operating in the linear region, the pullup on B-side (input side) begins to source current into the A side, where the downward slope can be modeled as V_G- V_{TH}/ R_{PUB}. Note here that the data shown in the simulation is only to demonstrate the behavior of the device in this environment. Real life behavior of the device is dependent on multiple factors (process, variation, temperature, and others) so there is no guarantee for the voltage sag to be this small across the leakage current parameters.

Simulation #2: Benefit of having a pullup resistor (2.2kΩ) on receiver side with excessive leakage current on receiver side:

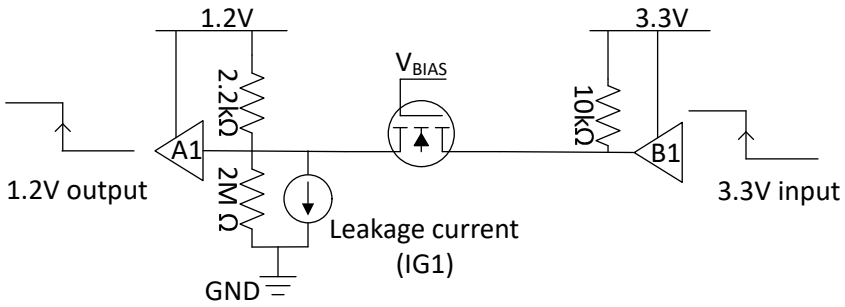

Figure 3-4. Simulation Setup With Excessive Leakage and Pullup Resistor on Receiver Side

Simulation #2: Output level on low-side with external uullup on A-side (2.2kΩ)

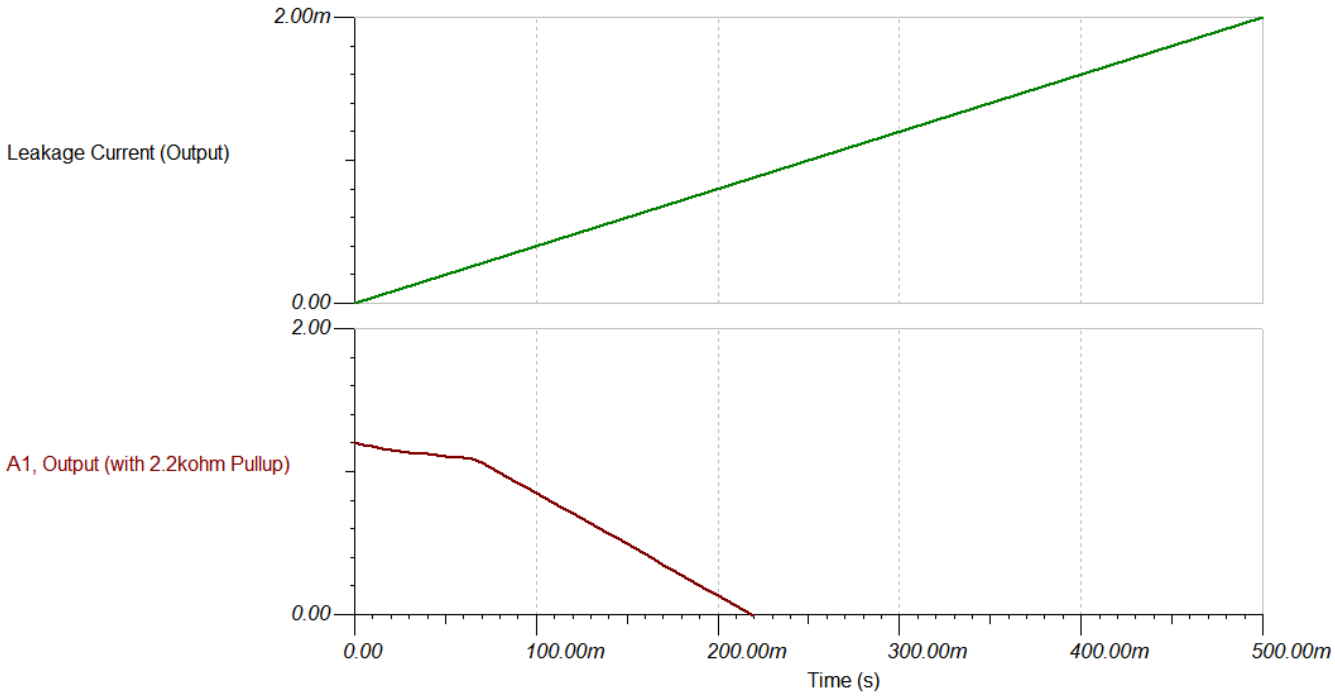

Figure 3-5. Simulation #2 Results

Table 3-2. Simulation Results

Simulated Leakage Current on Output (uA), IG1	Output Voltage (V), A1-No External Pullup	Output Voltage (V), A1 with External Pullup
10	1.19	1.2
100	1.13	1.14
200	1.09	1.11
250	1.01	1.09
275	0.53	1.07
300	0.28	1.03

Note: Values are taken from simulation only to demonstrate the behavior of leakage current and effect on output voltage with and without pullup resistor used on output.

In the 2nd schematic/ simulation, an external pullup resistor on A side (R_{PUA}) can be used to help regulate the voltage by sourcing the current which the device on A-side is capable of sinking/ sourcing.

4 How is Power Consumption Calculated for LSF Devices?

The LSF Family translators use passive components to perform level translation therefore these devices do not consume much power on their own. Instead there are other areas where power is dissipated. One of which, is the small current that flows through the internal biasing FET of the device. During normal operation (LSF010x, LSF0204), there is a leakage current from V_{REB} to V_{REFA} as depicted in the Figure 4-1. This current can be calculated as $I_{CC} = (V_{REFB}-V_{REFA}-V_{TH})/ 200k\Omega$, where R_{BIAS} is recommended to be a value of 200kΩ to minimize the leakage current from flowing back into VCCA.

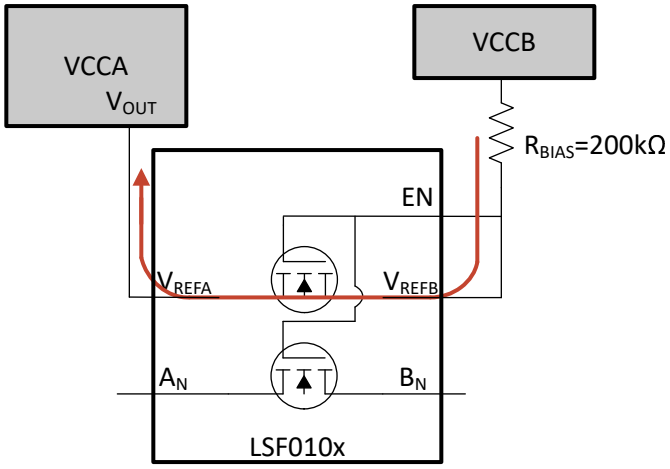

Figure 4-1. Leakage Current from Higher to Lower Power Supplies

The second leakage current sinks into the driver side whenever an input low signal is being propagated through the device. During a logic LOW, the FET is turned on due to voltage difference between the source (driver) and the gate of the FET due to $V_{GS} > V_{TH}$. The FET operates similar to a small resistor, directly connecting the input to the output. During this time, there is current flow from R_{B1} on B side, through the FET, combining with the current flowing through pullup R_{A1} and sunk into the driver (A_N) side.

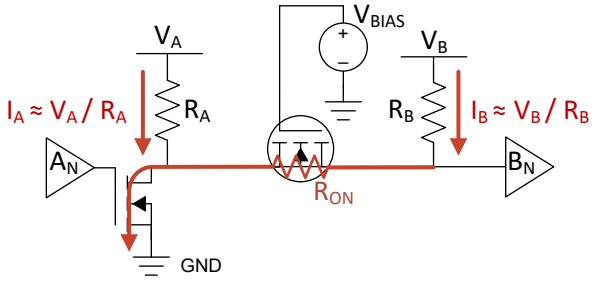

Figure 4-2. Leakage Current Into Driver Side During an Input Logic Low

The worst case is when all channels of the LSF device internal FET is on, where power dissipation, $P_D = N \times I_{CH}^2 \times R_{ON}$ where I_{CH} is I_B, the current flowing through the FET or V_B/R_B, and N is the number of channels actively switching. R_{ON} values can be used through data sheet values.

When a logic HIGH is being propagated, the FET transitions into cutoff mode, where the input and output are separated from one another, meaning negligible amount of current sinks back into the driver side (A_N). The calculation of this leakage current is insignificant and can be disregarded during power consumption calculation.

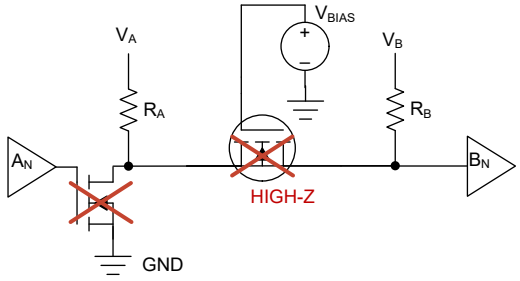

Figure 4-3. Leakage Current During an Input Logic High

5 Can I use LDO as a Power Supply?

During normal operation, there exists a leakage current that flows into the high-power supply (typ. referenced as V_{REFB}) and out the lower power supply (typ. referenced as V_{REFA}). The current flowing through the device is limited by the 200kΩ bias resistor to limit the current flowing through the internal FET and protect the lower supply from being overexposed to the otherwise high current, which can be presented by V_{REFB}-V_{REFA}-V_{TH}/ 200k.

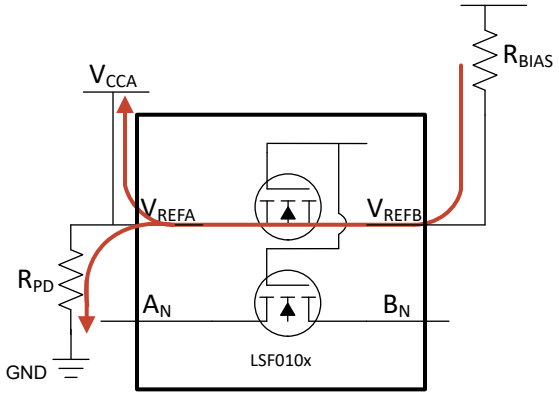

Figure 5-1. Using LDO Power Supply with LSF

Not all power supplies are capable of sinking in this back current, which is especially for the case when using low dropout regulator (LDO) as a power supply. If the LDO cannot sink this current, the LDO causes the power supply to float up above the expected levels of where it was at previously. For cases where the I/Os are also pulled up to LDO, their voltage levels also rise and can potentially damage both the signaling devices and the power supply. To accommodate for this current that cannot be accepted by the lower power supply, we recommend to add a relatively weak pulldown resistor at this node to create a path for the current to sink into instead.

6 What if my I/Os Operate Lower Than V_{REFA}?

To maintain proper functionality of the internal FET of the LSF, the voltage biased at V_{REFA} node needs to be the lowest voltage seen at the I/Os on A and B side. However, there can be cases where one of the I/Os operate lower than V_{CCA} and that voltage rail is also unavailable. One example of this is when the input voltage at the I/O channels have a $V_{OH,min}$ that is substantially lower than V_{CCA} for worst case conditions. To maintain that the FET operates in the proper state, V_{REFA} needs to be biased to similar voltages as $V_{OH,min}$ to achieve signal integrity. One method of resolving this is to create a voltage divider network with the V_{CCA} rail to maintain proper voltage at the V_{REFA} node. For single supply operation with only V_{REFB} rail, please refer to device data sheet.

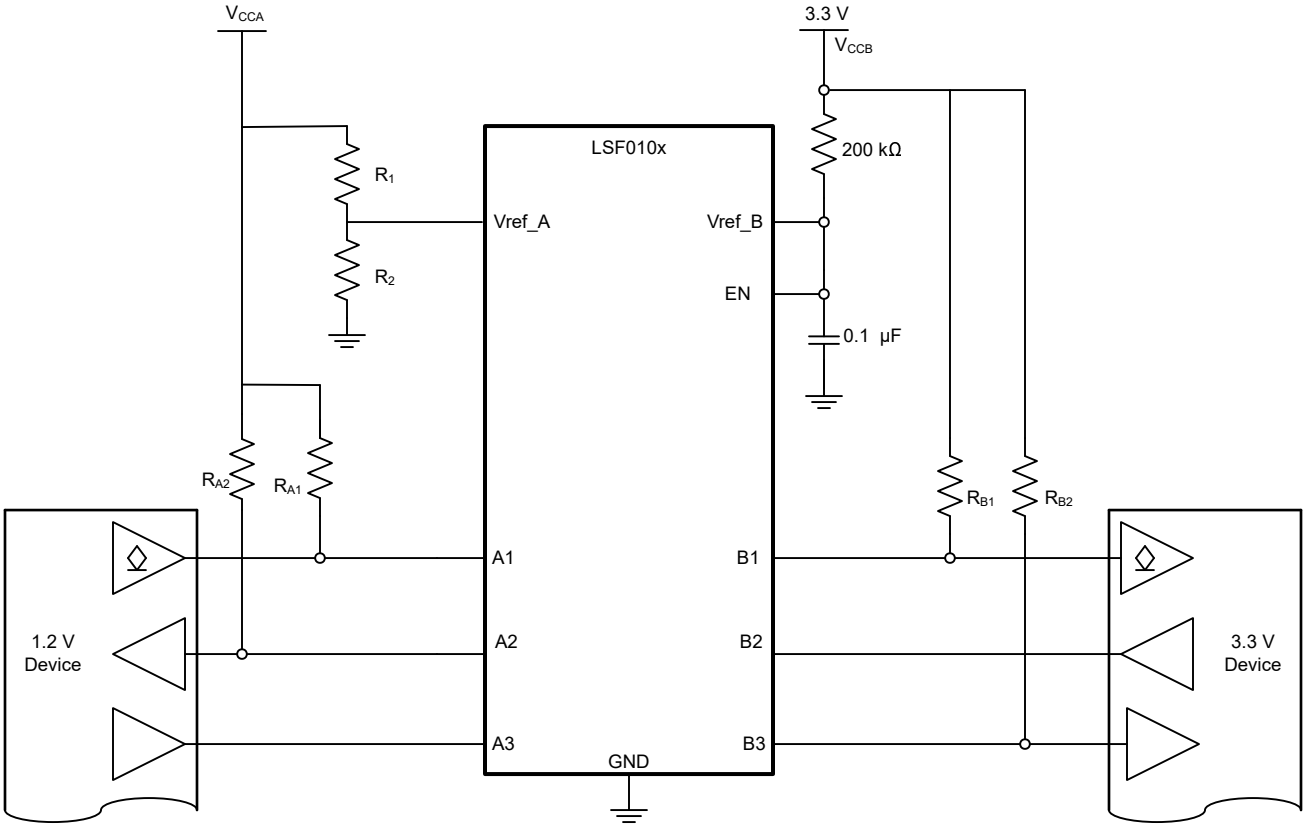

Figure 6-1. Voltage Divider Network on V_{REFA}

Use 1MΩ for R_1 to reduce leakage current.

Assume the below variables:

- V_x= Desired voltage for V_{REFA} rail
- V_{CCA}= Voltage at A-side power supply
- V_{TH}= 0.8V (typ. threshold value)
- R_{BIAS} = 200kΩ (external)
- R_1= External pullup on A-side power supply
- R_2= External pulldown on A-side power supply
- V_{REFB} = B-side power supply

Then the below equation can be used to solve for R_2 given known V_x:

$$R_2 = \frac{V_x \times R_1 \times R_{BIAS}}{R_{BIAS}(V_A - V_x) + R_1(V_{REFB} - (V_x + V_{TH})} \quad (1)$$

Take an example where V_{REFA} desired voltage is 1.4V but only a 1.8V power supply is available. In this case, we use R_1= 1MΩ to reduce leakage and V_x to be 1.4V since it is the voltage required. Then the pulldown, R_2 can be calculated through:

$$R_2 = \frac{1.4V \times 1M\Omega \times 200k\Omega}{200k\Omega(1.8V - 1.4V) + 1M\Omega(3.3V - (1.4V + 0.7V)} \quad (2)$$

$$R_2 = 237k\Omega \quad (3)$$

7 Summary

The LSF family translators can be used in a wide range of level shifting applications including open drain and push- pull interfaces due to the unique architecture compared to other translators. This app note compiles the most commonly asked questions regarding the LSF family to help designers fully use the LSF family benefits and tailor performance towards system requirements.

8 References

- Texas Instruments, *Voltage-Level Translation With the LSF Family*, application note
- Texas Instruments, *Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators*, application note
- Texas Instruments, *Factors Affecting VOL for TXS and LSF Auto-bidirectional Translation Devices*, application note
- Texas Instruments, LSF0108 Channel Auto-Bidirectional Multi-Voltage Level Translator for Open-Drain, data sheet
- Texas Instruments, LSF0204 Channel Auto-Bidirectional Multi-Voltage Level Translator for Open-Drain, data sheet
- Texas Instruments,LSF0102 Channel Auto-Bidirectional Multi-Voltage Level Translator for Open-Drain, data sheet
- Texas Instruments,LSF0002 Channel Auto-Bidirectional Multi-Voltage Level Translator for Open-Drain, data sheet
- Texas Instruments, LSF0101 Channel Auto-Bidirectional Multi-Voltage Level Translator for Open-Drain, data sheet

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265