Application Brief

Enabling AI Accelerators with Voltage Level Translation and Analog Multiplexing

Atul Patel, Jackson Jarboe

Introduction

Several of today's electronic end equipment applications are adding artificial intelligence (AI) capabilities to help bring new functionality and user experiences to end applications enabling users to harness the power of AI in their day to day work flows. To bring AI capabilities to their end application, electronic system designers need to leverage large language models (LLM) such as Generative Pre-trained Transformers (GPT) which requires high performance compute capabilities on both the cloud side as well as the client side of applications. Enabling AI capabilities on device or by leveraging cloud-based compute infrastructure requires client systems and cloud infrastructure designers to leverage the latest processor technologies.

GPT based AI implementations require system designers to not only use the latest high-performance processors and FPGAs (CPU based devices) but also use the latest high-performance GPU (Graphic Processing Units) that are better suited for AI given their ability to parallel process large amounts of data as well as higher memory bandwidths needed for high speed data transfer. Using the latest CPUs and GPUs to support AI functionality does present systems designer with multiple design challenges.

One of these design challenges is overcoming the control and low speed data I/O level mismatches that results from operating CPUs and GPUs at very low core voltages. Operating high performance CPUs and GPUs at low core voltages is often an absolute requirement for achieving target performance levels given the thermal and power limitations of a specific processor. Operating CPUs and GPUs at low core voltages limits the I/O voltage levels that these processors can support.

System designers often need a simple, efficient and scalable way to connect the numerous I/O and control buses of their GPU processors to peripheral devices and sub-systems. One design approach that enables system designers to maintain the CPU's or GPU's lower core voltage and still resolve I/O level mismatches is to use simple voltage level translator devices. Level translation devices provide system designers an easy and cost-effective solution for resolving their system's I/O level mismatch challenges without having to compromise on performance, power, or size. See Figure 1.

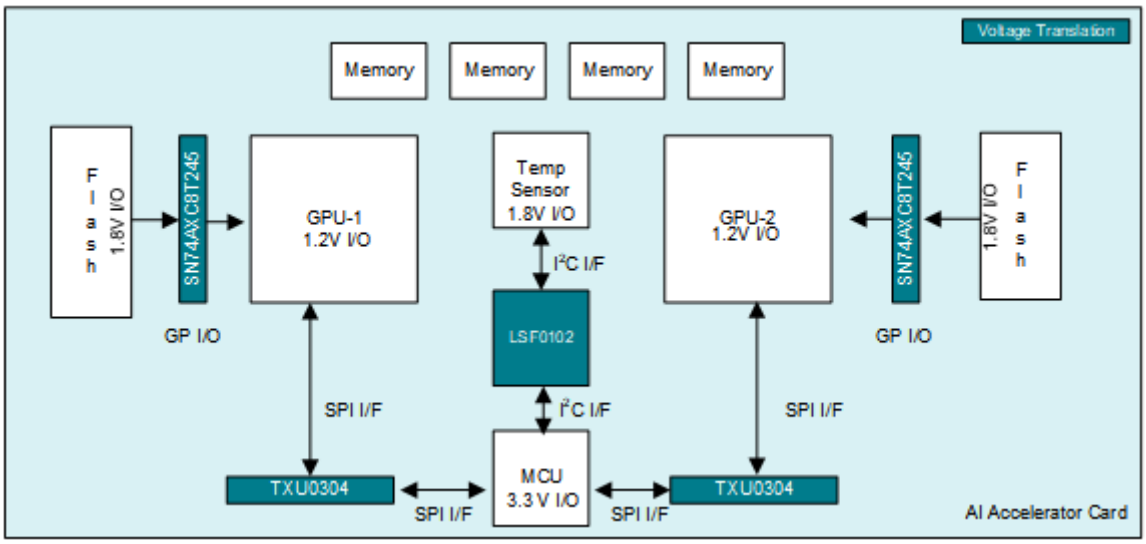

Figure 1. AI Accelerator Card Block Diagram

Voltage Level Translation

Integrated level shifting designs are available in a wide assortment of I/O types, bit widths, data rate ranges, current drive capabilities, and package options. Texas Instruments' portfolio of level shifter devices contains many different types of level translation functions that collectively is able to address almost any interface requirement likely needed for high performance compute use cases for AI applications. TI's level translation portfolio includes Auto Directional, Direction Controlled, and Fixed Direction level translators in Industrial, Automotive and Enhanced ratings. Table 1 shows common control interfaces found on high-performance CPU and GPU families and recommended level translation devices for each interface supporting voltage ranges from < 0.8V to 5.5V. For more information on all of TI's level translation devices, please visit TI's Level Translation Landing Page.

Table 1. Recommended Translator by Interface

	Translation Level	
Interface	**Up to 3.6V**	**Up to 5.5V**
FET Replacement	2N7001T	SN74LXC1T45/TXU0101
1 Bit GPIO/Clock Signal	SN74AXC1T45	SN74LXC1T45/TXU0101
2 Bit GPIO	SN74AXC2T245	SN74LXC2T45 / TXU0x02
2-Pin JTAG/UART	SN74AXC2T45	SN74LXC2T45 / TXU0x02
I2C/MDIO/SMBus	TXS0102 / LSF0102 / PCA9306	TXS0102 / LSF0102 / PCA9306
I^3C	TCA39306	TCA39306
4 Bit GPIO	SN74AXC4T245	TXB0104 / TXU0104
UART	SN74AXC4T245	TXB0104 / TXU0204
SPI	SN74AXC4T774 / TXB0104	TXB0104 / TXU0304
JTAG	SN74AXC4T774/ TXB0104	TXB0104 / TXU0204
I2S/PCM	SN74AXC4T774 / TXB0104	TXB0104 / TXU0204
Quad-SPI	TXB0106	TXB0106
SDIO/SD/MMC	TXS0206 / TWL1200	NA
8 Bit GPIO/RGMII	TXV0106/TXV0108	SN74LXC8T245

Analog Multiplexers

Analog multiplexers allow the selection and routing of multiple data lines to a single output, optimizing resource utilization and improving overall performance within the accelerator architecture. Switching is involved in many components including hardware accelerator baseboards, GPU cards, and Smart NICs to aid in processing large amounts of data in a small space.

Low voltage multiplexing is prevalent in AI accelerators for a variety of needs. TI offers devices for many applications including SPI interface, isolation and power sequencing for digital bus switching, GPIO expansion, clock signal muxing, and I2C/I3C protocol switching. Table 2 shows common control interfaces found in accelerators along with the recommended multiplexers for each interface supporting a wide range of supply voltages ranging from 1V to 5.5V. For more information, please visit TI's Analog Switches and Multiplexers page.

Table 2. Recommended Multiplexer by Interface

Interface		Configuration	Multiplexer Supply Voltage		
			1.8V	3.3V	5V
Quad-SPI		2:1	TS3A27518E	TS3A27518E	-
SPI		2:1	TMUX1575	SN74CB3Q3257	TMUX1574
I2C	GPIO Controlled	2:1	TMUX1574	TMUX121	TMUX1072
		3:1, 4:1	TMUX1309A	TS3A5017	SN74LV4052A
	I2C Controlled	4:1	TCA9546A	TCA9546A	TCA9546A
		8:1	TCA9548A	TCA9548A	TCA9548A
I3C Controlled		2:1	TMUX1574	TMUX136	TMUX1574
		3:1, 4:1	SN74CB3Q3253	TMUX131	-
USB		2:1	TMUXHS221F	TS3USB221A	TS5USBC412
GPIO		1:1, 1-bit	SN74LVC1G66	SN74CBTLV1G125	SN74CBT1G125
		1:1, 2-bit	SN74LVC2G66	SN74CBQ3306A	SN74CBTD3306C
		1:1, 4-bit	TMUX1511	SN74CBTLV3126	SN74CBT3126
		1:1, 8-bit	-	SN7CBTLV3245A	SN74CBT3245C

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265