Application Brief

Supporting Time and Skew Sensitive Interfaces with TI's TXV Level-Shifter Portfolio

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Introduction

Physical layer devices (PHYs) play an important part of the Ethernet network protocol as they bridge data communication from the external world by serializing and de-serializing data over many different types of translation media. PHYs are connected to an Ethernet media access controller (MAC), which is typically integrated in an FPGA or SoC. Interface design challenges often arise as large digital devices like SoCs, ASICs, and FPGAs move to lower core voltages. Integrated and standalone MACs are often not able to support a higher I/O voltage when operating at low voltages. System designers often need to resolve I/O level mismatch between the MAC and PHY while still maintaining the signal integrity of the interface. Additionally, Ethernet interfaces like Reduced Gigabit Media Independent Interface (RGMII) have strict timing requirements, which are even harder to meet at lower voltages.

This application brief provides over the timing requirements of RGMII and show how TI's high speed TXV family can meet RGMII timing requirements while overcoming I/O voltage mismatch.

RGMII Timing Requirements

RGMII is an interface used between the MAC and PHY and allows speeds of 10 Mbps, 100 Mbps and 1000 Mbps. Figure 1 shows the connection between the MAC and PHY. The timing requirements are more strict when operating at 1000 Mbps since data is processed in Dual Data Rate (DDR) signaling while the lower speeds use Single Data Rate (SDR). 1000 Mbps timing will be used throughout this app brief since satisfying those requirements also satisfies 10 Mbps and 100 Mbps timing requirements.

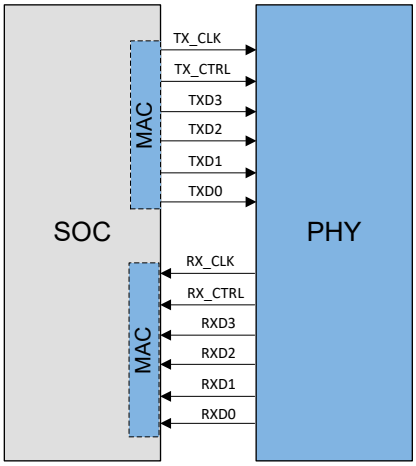

Figure 1. RGMII Interface Between MAC and PHY

Table 1, Figure 2 and Figure 3, show the timing requirements for both RGMII Version 1.3 and 2.0 standards. Version 1.3 states skew must be introduced between the clock and data lines, typically around 1.5 to 2.0 ns. In Version 2.0, skew can be generated by either the MAC or PHY and are given by T_{setupT} and T_{holdT}. RGMII Version 2.0 timing is highlighted in red.

Table 1. RGMII Version 1.3 and 2.0 Timing Specifications

Symbol	Parameter	Min	Typical	Max	Units
T_{skewT}	Data to Clock Output Skew (at Transmitter)	-500	0	500	ps
T_{skewR}	Data to Clock Input Skew (at Receiver)	1	1.8	2.6	ns
T_{setupT}	Data to Clock Output Setup	1.2	2.0		ns
T_{holdT}	Data to Clock Output Hold	1.2	2.0		ns
T_{setupR}	Data to Clock Input Hold	1.0	2.0		ns
T_{holdR}	Data to Clock Input Hold	1.0	2.0		ns
T_{cyc}	Clock Cycle Duration	7.2	8	8.8	ns
D_{cyc}	Duty Cycle for Gigabit	45	50	55	%
T_R/T_F	Rise/Fall Time (20-80%)			0.75	ns

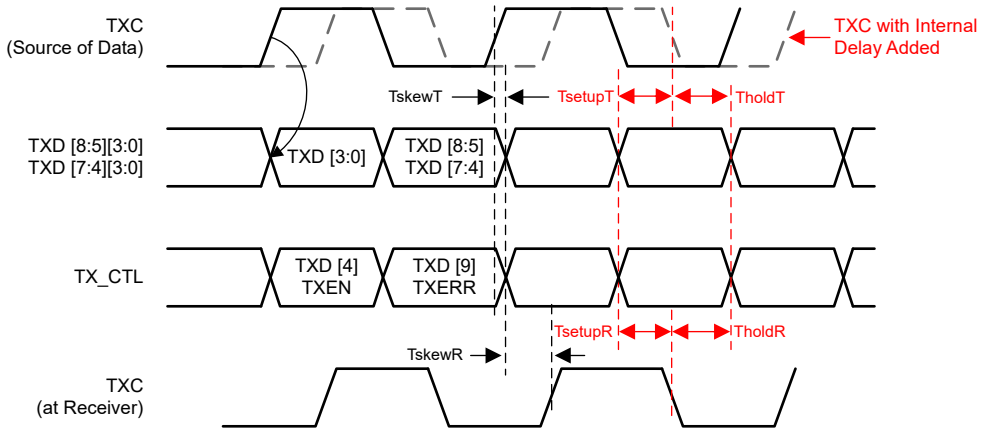

Figure 2. RGMII Version 1.3 and 2.0 Transmitter Timing Diagram

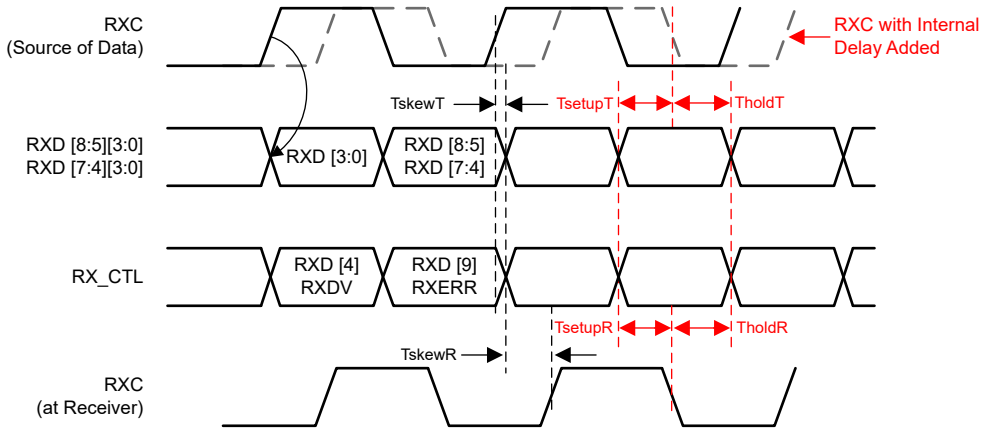

Figure 3. RGMII Version 1.3 and 2.0 Receiver Timing Diagram

TXV Output Skew Measurements

The output channel-to-channel skew, $T_{sk(o)}$, value found in the data sheet uses two types of skew measurements to capture the worst-case skew, output and inverting skew. An illustration for both can be found in Figure 4.

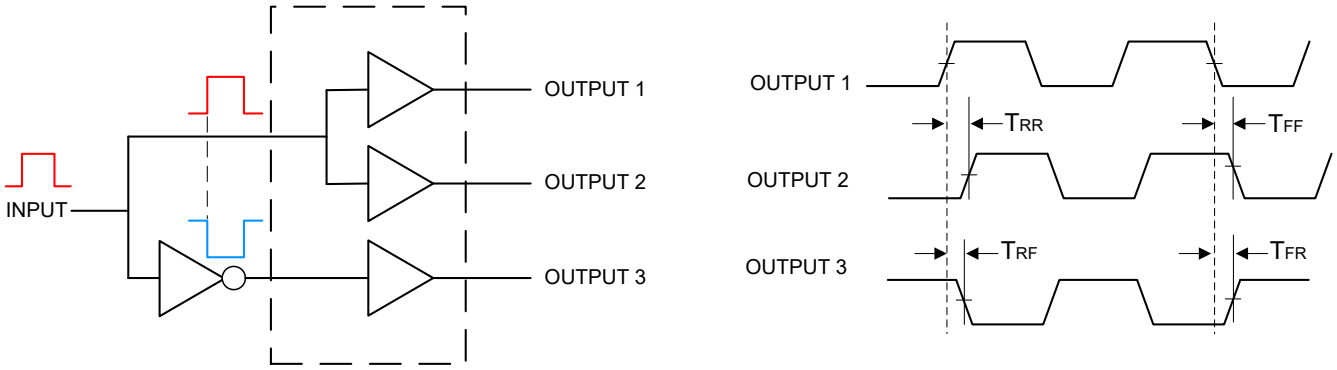

Figure 4. Output Skew (T_{RR}/T_{FF}) and Inverting Skew (T_{RF}/T_{FR}) Measurements

Output skew is the skew difference between any two outputs of the same device at identical transitions while driving identical specified loads. Output skew measurements are given by T_{RR} and T_{FF}. Inverting skew is the skew difference between two outputs of the same device with opposite input transitions while driving identical specified loads. Inverting skew measurements are given by T_{RF} and T_{FR}.

TXV Timing Benefit

Table 2 gives the timing difference between the TXV family and the RGMII standard. The comparison below shows the worst case timing of the TXV does not exceed the maximum timing parameters of the RGMII standard. This leaves timing margin to the MAC, PHY and PCB, and shows the TXV product family is suitable to interface with RGMII, even at 1000 Mbps.

Table 2. Comparison Between TXV0106/TXV0108 and RGMII Timing Specification

Symbol	Parameter	TXV Max [1] [2]	RGMII Max	Units
$T_{sk(o)}$	Output Channel-to-Channel Skew	± 317	± 500	ps
T_R/T_F	Rise/Fall Time (20-80%)	0.48	0.75	ns
D_{cyc}	Duty Cycle	± 4	± 5	%

Conclusion

Processors such as FPGA, SoC, and ASICs are moving to lower voltage I/Os benefiting customers by reducing power consumption. This can result in I/O voltage mismatch, however, many level-shifters are not capable in meeting strict timing requirements like rise/fall time, channel-to-channel skew and duty cycle distortion for skew sensitive interfaces. This application brief demonstrated how the TXV level-shifter family can bridge the I/O voltage gap while also delivering optimized AC performance and meeting strict timing requirements for low-skew interfaces like RGMII.

[1] V_{CCA} = 1.8 V, V_{CCB} = 3.3 V, C_{Load} = 5 pF, 250 Mbps for each data channel at 125°C
[2] Different voltage and loading conditions can also be found in the timing section on the TXV0106 and TXV0108 data sheet

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