Application Brief

Enabling Industrial and Automotive Ethernet RGMII Interfaces with Voltage Translation

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Ethernet has become the pervasive wired communication interface standard. Flexibility, cost, standardization, wide installed base, and many other factors has made Ethernet the go to communication standard for a spectrum of application use cases.

One of the key benefits of using Ethernet is the wide array of circuit options that exists for implementing the Physical (PHY) and Media Access Controller (MAC) layers of an Ethernet implementation. Several of today's Ethernet applications use integrated MAC and PHY devices which enable higher density application use case implementations where core processing of the data is relatively close to the integrated MAC/PHY device which can also be integrated into large switch ASSP (Application Specific Standard Product) devices.

However, for industrial and automotive use cases, many design engineers are having to separate the PHY and MAC layers as a result of physical location of data sources not being able to accommodate a larger integrated MAC/PHY device due to size, power, and signal routing constraints.

In addition, MAC functionality is often integrated into processors or FPGAs with interfaces provided for external PHY connectivity. For example, zonal architectures for networking in vehicles is becoming an enabling design approach for many of today's electric vehicle designs. Zone based designs rely on Ethernet as the underlying communication protocol. Zone based in-vehicle networks often have separate Ethernet MAC and Phy implementations that need to interoperate.

One of the main design challenges that design engineers face when using separate Ethernet MAC and PHY devices is having to resolve the I/O voltage mismatch that often arises between the MAC and PHY interfaces such as RGMII (Reduced Gigabit Media Independent Interface). It's common for MAC devices to be developed in smaller CMOS process technologies whether as standalone devices or integrated into large processors or FPGAs.

Devices developed in small CMOS process geometries often require lower core voltages such as 1.8 V or even lower. As a result of lower core voltages, the I/O voltages these devices can support is much lower than traditional I/O level such as 2.5 V and 3.3 V.

Also, Ethernet PHY devices are developed in mixed signal silicon processes that tend to operate at higher voltages in order to achieve the signal integrity performance needed for Ethernet serial data rates. System designers are turning to voltage level translation ICs to help resolve the I/O level mismatch between Ethernet MAC and PHY interfaces such as RGMII. TI's latest level translation devices TXV0106 and TXV0108 have been specifically developed to help system designers address voltage level mismatches for high performance use cases like Ethernet MAC to PHY interfaces such as RGMII. See Figure 1.

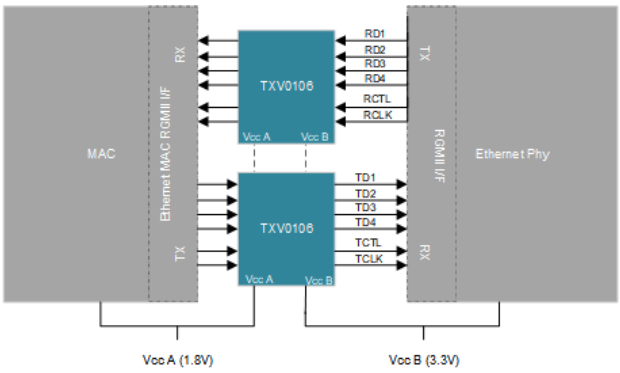

Figure 1. MAC to Ethernet Phy RGMII Interface

The TXV0106 and TXV0108 are one of the first translator devices to support RGMII interface signaling specifications with RGMII friendly pin outs enabling system designers to easily implement RGMII level translation as well as translation for other skew sensitive interfaces.

The TXV0106 is a fixed direction 6-bit level translator and buffer device supporting level translation between 1.8 V to 3.6 V. TXV0108 is a direction controlled 8-bit

level translator and buffer device supporting 1.8 V to 3.6 V translation with an industry standard footprint.

System designers can use the TXV0106 and TXV0108 for not only level translation use cases but also for cases where the RGMII interface may need to be buffered as a result of low I/O drive strength of the MAC or PHY devices. See level translation use case example in Figure 2. The TXV0106 and TXV0108 are available in both industrial and automotive grades. Another key concern for system designers for implementing RGMII level shifting is placing a device between the MAC and PHY. Interfaces such as RGMII tend to have stringent timing and skew requirements and placing a device between the MAC and PHY can make meeting the interface's timing requirements difficult.

The TXV0106 and TXV0108 help alleviate concerns of placing a device between the MAC and PHY by ensuring the devices meet RGMII I/O signaling specifications. General purpose level translation devices are usually not tested to specifically meet RGMII specifications so their suitability for these types of interfaces becomes much more difficult to determine without having to do lengthy testing for specific board level implementations.

Factors such as the layout of the RGMII interface signals, trace widths, and signal routing all play a role in ensuring the RGMII specifications are met. For more information on TXV0106-Q1 or the TXV0108-Q1 and using them to implement RGMII level translation please visit the TXV0106, TXV0106-Q1, TXV0108, or TXV0108-Q1 translation product pages on ti.com.

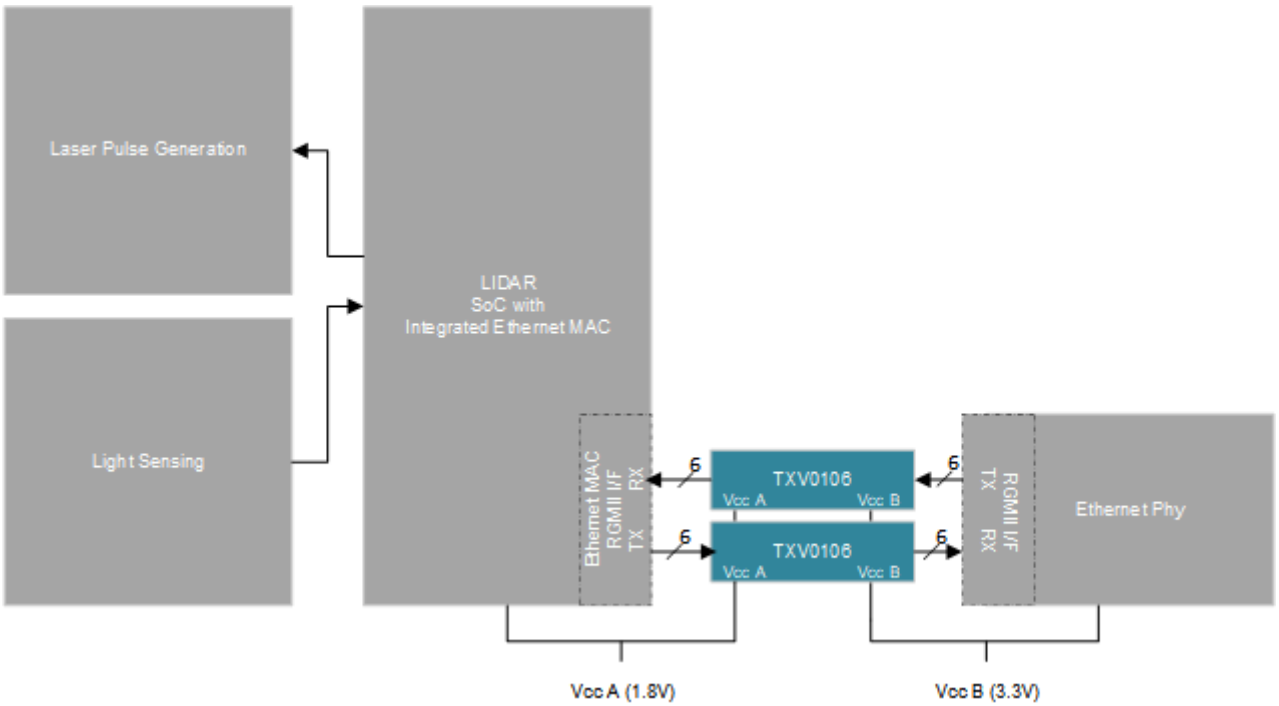

Figure 2. RGMII for LIDAR SoC Application

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