TWL1200 PCB Design Guidelines

Jason Battle *Standard Linear and Logic*

ABSTRACT

The Texas Instruments TWL1200 is a 19-bit voltage translator specifically designed to bridge the 1.8-V/2.6-V digital-switching compatibility gap between a 2.6-V baseband and the Wi-Link-6 (WL1271/3), and is optimized for SDIO, UART, and audio functions. When laying out a printed circuit board (PCB) for the TWL1200, careful consideration of design rules and guidelines must be employed to help preserve signal integrity and ensure optimal device performance.

This document presents several guidelines for designing the TWL1200 PCB and includes recommendations for device placement and proper layout.

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1 Overview

This document provides helpful guidelines that should be followed during TWL1200 layout creation. It is a complementary document and is not intended to replace the device data sheet. As a result, system designers should still reference all relevant device data sheets and application materials during system-level design to facilitate development of the highest quality end product.

The guidelines presented in this document are based on Texas Instruments' reference platforms and general design recommendations. Follow these rules to avoid unnecessary mistakes that can result in multiple PCB spins and delay time-to-market of the end product.

For questions or issues that arise during the layout process, contact your local Texas Instruments representative or field applications support.

2 Layout and Design Guidelines

2.1 Layer Stackup

The recommendations in this document refer to a four-layer PCB stackup with the TWL1200 and WL1271/3 devices implemented. Designing with a minimum of four layers is a great general-purpose rule of thumb for constructing a board with low electromagnetic interference (EMI). Additional layers may be incorporated into the PCB if needed, but they are not required to achieve an efficient design because all necessary routing for the TWL1200 and WL1271/3 can be accomplished in four layers. If complex designs warrant the need for more layers, the designer must always strive to preserve symmetry by using even numbered layer counts, as this helps prevent board warping during the fabrication process. For this TWL1200 PCB design, the chosen dielectric material is FR-4. Ideal board stackup from top to bottom is shown in Table 1.

Table 1. Four-Layer Stackup for TWL1200 PCB Design

	Subclass Name	Type	Thickness (mils)	Dielectric Constant	Loss Tangent	Shield	Width (mils)	Impedance (Ω)
1		Surface		1	0			
2	TOP (high speed)	Conductor	2.4	1	0		4	42.727
3		Dielectric	2	4.5	0.035			
4	GND	Plane	1.2	1	0	YES		
5		Dielectric	52	4.5	0.035			
6	VCC	Plane	1.2	1	0	YES		
7		Dielectric	2	4.5	0.035			
8	BOTTOM (low speed)	Conductor	2.4	1	0		4	42.727
9		Surface		1	0			

High-frequency signals exhibit sensitivity to impedance changes and discontinuities introduced by the use of vias. Placing this layer on the top helps reduce the need for vias and provides easy access for making direct interconnections. In addition, it is critical to keep all high-frequency traces at a characteristic impedance of 50 Ω or less to minimize transmission line effects. Due to clearance constraints that arise in dealing with ball grid array (BGA) and wafer chip scale packages (WCSP), a worst case trace width of 4 mils was assumed for this design. An impedance calculator or field solver may be used to help ensure that the desired trace impedance is achieved. Placing the ground layer directly underneath the high-frequency layer creates an ideal low-inductance path for return current flow, reducing potential for noise and signal reflection. The power layer is placed immediately underneath the ground layer to increase high-frequency bypass capacitance, which helps strengthen PCB immunity to power supply ripple. Adding the low-frequency signal routes on the bottom layer is the next logical step, as these signals can typically handle use of vias and other discontinues without suffering adverse effects on performance due to slower characteristic rise and fall times. If variations in this board stackup are necessary based on individual application requirements, system designers need to recalculate the characteristic trace impedance of all high-speed signal layers to ensure that they do not exceed 50 Ω in the new stackup.

2.2 Reference Planes

For medium- to high-frequency signals, best performance can be achieved by using a ground plane that is continuous across the entire PCB. Introducing discontinuities into the ground plane can increase EMI radiation due to larger inductance from potentially longer return current paths. Other unwanted effects can arise when splitting the ground layer into multiple planes. Traces on other layers that cross multiple split grounds can result in increased crosstalk due to coupling between these traces and incorrect reference planes. For example, routing audio signals, which are analog in nature, across a digital ground plane can strengthen the parasitic coupling between them, allowing noise to be injected into the digital ground plane. Another consequence is that controlled impedance traces become undefined when the ground plane is split under them. Signals routed on a continuous ground layer beneath controlled impedance traces have the same problematic effect as well. An example of continuous and split ground planes is shown in Figure 1.

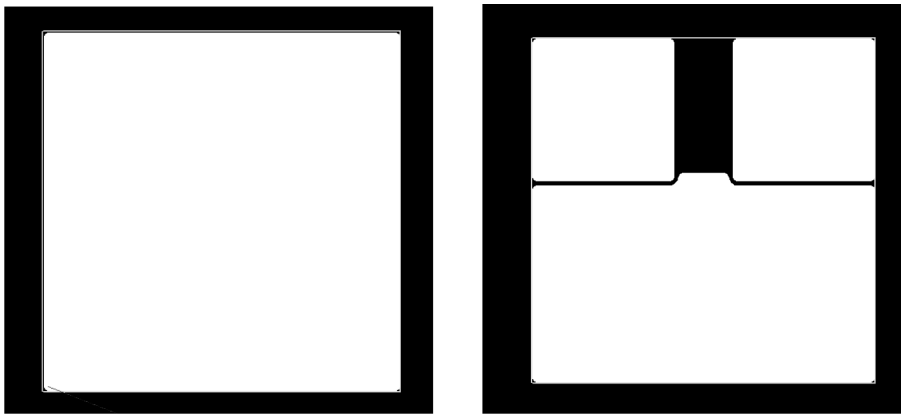

Figure 1. Continuous and Split Ground Planes

For four-layer boards, the best solution is to create a continuous dedicated plane for ground and to split the power supply layer as needed for different supply voltages. Larger PCB designs with spare layers may remove the need to split the power supply plane, because the extra layers allow for creation of dedicated power supply layers. If the ground plane needs to be split for some reason, such as to provide separate digital and analog ground references for a given system, the following rules should be taken into consideration to prevent potential design mistakes:

- Minimize loop areas by avoiding signal routes across plane splits.
- Connect local grounds to the common ground though a single point. Return current should not be forced to travel through multiple local grounds before reaching the common ground.
- Ensure that individual signal or power planes reference only their correct ground plane.
- Bypass capacitors should not be placed between any given signal or power plane and an unrelated ground plane.

With regard to the TWL1200, these reference plane guidelines are most critical for the SDIO, UART, and PCM audio lines. These traces carry medium- to high-frequency periodic signals that may exhibit increased sensitivity when routed across plane splits. Low-frequency, non-periodic signals, such as the enable and interrupt control signals routed on the bottom layer, exhibit higher tolerance to such discontinuities. Because the TWL1200 PCB design requires both 2.6-V and 1.8-V rails, it is best to keep the ground layer continuous and split the power plane into separate areas for the required voltages. This allows signal integrity to be maintained without having to add two additional layers to accommodate the extra voltage level.

2.3 Routing

2.3.1 Trace Width

Moving on to board routing, careful attention must be paid to trace characteristics such as width, length, and angle. Effective trace resistance is largely determined by its width and this, in turn, has a direct impact on its current carrying capability. Deviations in width across the length of a trace should be avoided because they cause impedance changes which contribute to the reflection of alternating current (ac) signals, causing problematic oscillations and ringing at the electrical source. This is also the reason why the angle of traces routed around corners becomes so important. 90° bends are seen as a large impedance change due to the increase in effective trace width. Better design practice is to use 45° angles for all trace bends in general-purpose designs. Higher speed signaling may even warrant the need for rounded trace bends to limit impedance changes as stringently as possible. Examples of each bend style are shown in Figure 2.

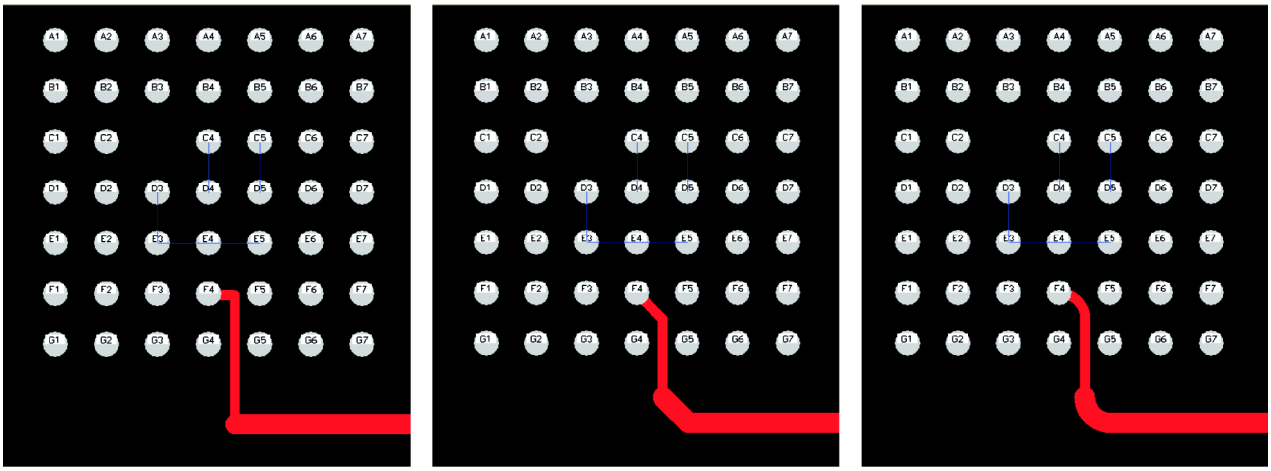

Figure 2. 90°, 45°, and Rounded Trace Bends

2.3.2 Trace Length

Trace length represents an equally important characteristic. As trace length increases, so does the effective capacitance and inductance. Instead of being seen as a lumped load, the trace starts to behave as a transmission line with distributed parallel capacitance and series inductance. An equivalent circuit for a trace with excessive length is shown in Figure 3.

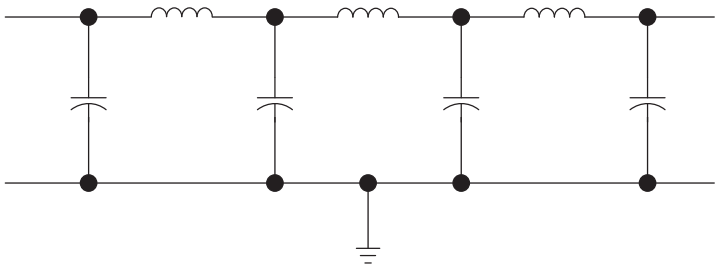

Figure 3. Transmission Line Effects

This increases an electrical signal's net RC time constant, resulting in slower output slew rates and longer propagation delay times. In addition, heavy inductance in the propagated signal's path can contribute to excessive ringing during rising and falling output transitions as a result of undesired current interactions.

The critical nature of these characteristics is purely application dependant, and appropriate measures should be taken to optimize them based on specific design needs. It is also worth noting that series and parallel termination techniques offer system designers a reliable method of impedance matching for traces with excessive length. An example of power and ground rail bounce caused by large series inductances is shown in Figure 4.

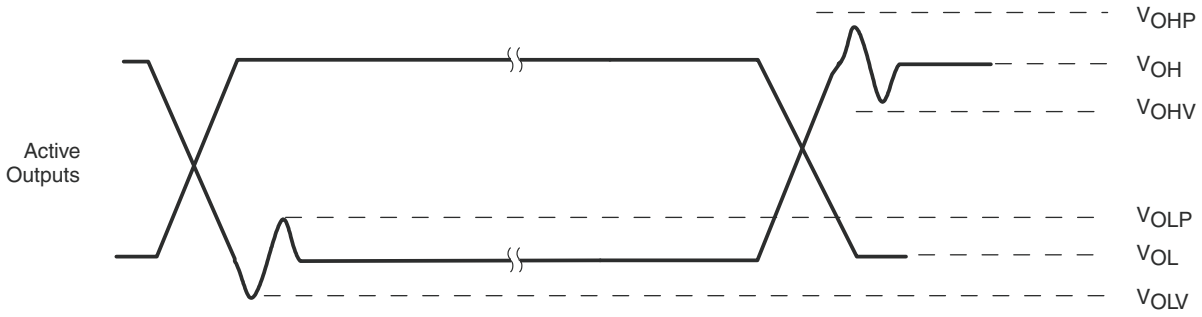

Figure 4. Power and Ground Rail Bounce

2.3.3 Solder Thieving

Another caveat for trace design depends on the chosen device package. Ball grid array and wafer chip scale style packages do not have leads and instead use solder balls that are reflowed during the solder process. The width of all traces routed to these balls determines how much solder is thieved away from them during reflow. Migration of solder away from the ball joints reduces package reliability and increases risk of shorted leads as well as other problems. Although solder resist can lessen this effect, it is still best to use symmetrical leadaway traces as a reliable method to mitigate issues involving solder thieving. As a result, traces routed from inner balls to just outside of the package outline should have a smaller width than that of their respective solder pads to prevent solder migration. Trace widths from 4 mils to 6 mils usually suffice as reliable general-purpose leadaway for WCSP and BGA applications. From there, leadaway traces can be routed elsewhere on the board using standard 8-mil to 10-mil traces or larger, depending on impedance matching or ampacity requirements. Correct leadaway trace routing for WCSP and BGA packages is shown in Figure 5.

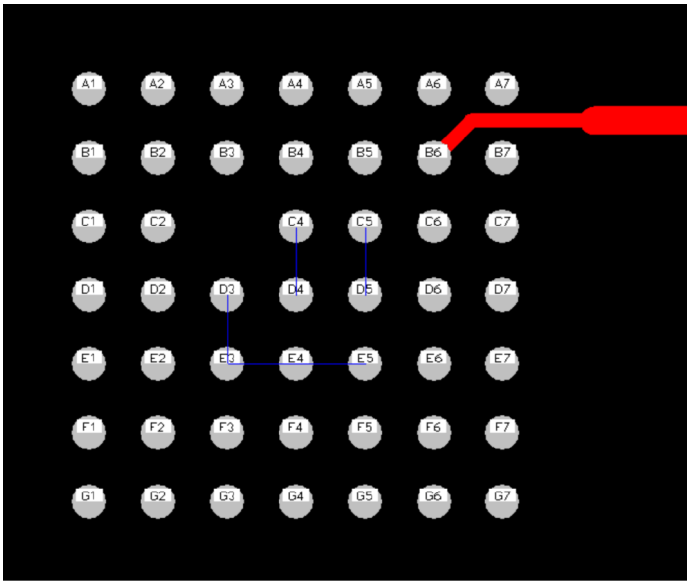

Figure 5. Leadaway Trace Routing for BGA or WCSP Packages

2.3.4 High-Speed Signals

When applying routing guidelines to any trace design, it often proves quite helpful to refer to the device data sheet for details on circuit architecture, principles of operation, and application information. Looking at the TWL1200 data sheet, it is evident that the design consists of both fully-buffered and semi-buffered input/output (I/O) sections with varying output drive characteristics (see Table 2).

Table 2. TWL1200 I/O Drive Strengths

2 mA	4 mA	8 mA
WLAN_EN(B)	AUDIO_OUT(A)	SDIO_CLK(B)
SLOW_CLK(B)	WLAN_IRQ(A)	BT_UART_TX(A)
BT_EN(B)	CLK_REQ(A)	BT_UART_RX(B)
	AUDIO_IN(B)	
	AUDIO_CLK(A)	
	BT_UART CTS(B)	
	BT_UART RTS(A)	
	AUDIO_F-SYNC(A)	

The drive strength of a corresponding output gives an indication of the amount of capacitive and/or resistive loading it can handle without severe degradation in its output high (V_{OH}) and output low (V_{OL}) voltages. A closer comparative look at Table 2 also reveals that all TWL1200 SDIO paths except for SDIO_CLK are semi-buffered and offer very little, if any, direct current (dc) drive. The issue is further compounded by the fact that these signals switch at frequencies up to 25 MHz, making them relatively high-speed and quite sensitive to local sources of electrical noise that may exist as a result of improper PCB layout design. From this, it becomes simple to conclude that the SDIO paths should receive the highest priority in proactively minimizing trace length to mitigate transmission line effects. A reasonable approach is to keep the total trace length for each semi-buffered SDIO line to a maximum of four inches. This includes the entire electrical length from baseband chipset to destination SDIO peripheral, through the TWL1200. The routing example in Figure 6 shows proper trace length sizing for the SDIO_DATA0 path to and from the A and B sides of the TWL1200.

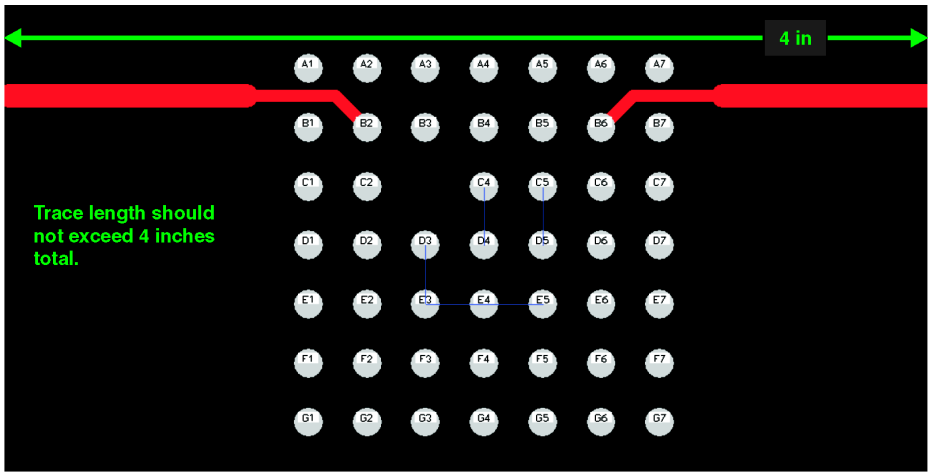

Figure 6. Trace Length Sizing for SDIO_DATA0

An additional concern arises when routing adjacent traces too close together. Crosstalk is essentially a capacitive coupling event that occurs when a signal "bleeds" onto nearby traces through a parasitic low-impedance path. To prevent this phenomenon, best design practice is to keep the distance between adjacent traces at least 2 to 3 times their width apart. For example, 10-mil traces should be kept at least 20 mils away from unrelated traces, pads, vias, or other electrical paths. Figure 7 shows proper distancing between a high-speed SDIO trace and a low-speed control signal routed on the same layer.

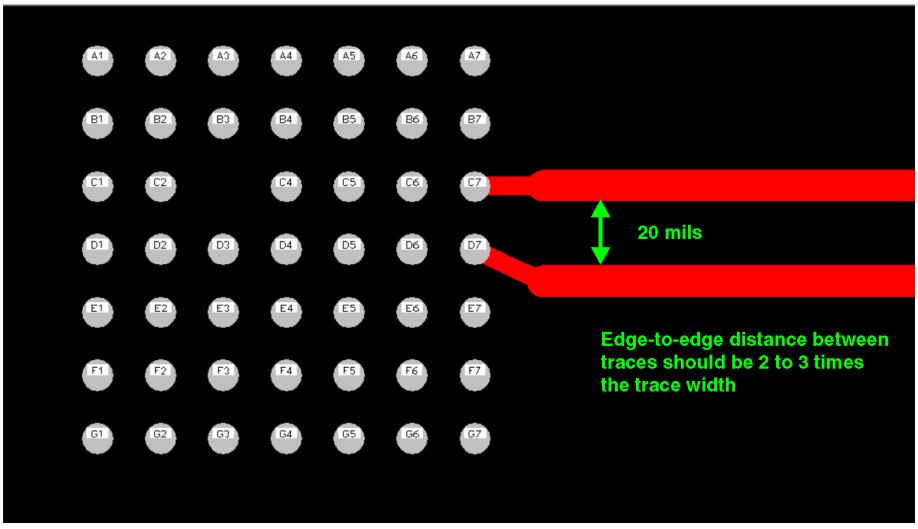

Figure 7. Proper High-Speed Trace Routing for Crosstalk Reduction

Another factor relevant to SDIO routing is in regards to discrete resistive and capacitive loading placed on these I/Os for line termination or filtering purposes. Resistive loading such as external pullup or pulldown resistors create additional problems for these I/Os and should be avoided entirely. If absolutely necessary for a given system design, they should be of relatively high-impedance values to prevent the possibility of overdriving the internal pullup resistors on the TWL1200 SDIO lines. Values of 50 kΩ or larger are well suited for this purpose if the end application finds them absolutely necessary. Failing to use proper values can compromise the current-sourcing capability of the internal pullups, creating an effective voltage divider, which can result in bus contention due to indeterminate input and output logic levels. Excessive capacitance on these traces is problematic as well and can lead to degradation of rising and falling SDIO edges. This eventually leads to duty-cycle distortion and can make it quite difficult to achieve higher data rates.

Another issue with heavy capacitive loading has to do with the design architecture of the TWL1200's semi-buffered, switch-type translation paths. For these I/Os, the dc drive is provided by internal pullup resistors in combination with the open-drain or push-pull drivers that are interfaced with the TWL1200. The ac drive, however, is provided by edge-acceleration circuitry that temporarily decreases the output impedance of the TWL1200 SDIO lines to achieve faster output rise and fall times. When excessive capacitance is present on these lines, the edge-acceleration circuitry times out and switches off before the SDIO output transition is fully completed. As the SDIO output signals are reflected back to the TWL1200, they see a higher impedance than before, causing signal reflections which can lead to glitches, ringing, or other troublesome oscillations. Overall, layout designers should avoid use of discrete loads or connectors on the SDIO lines where possible to keep capacitance low and manageable.

If onboard connectors are necessary, as is the case with Secure Digital (SD) cards, trace lengths to and from these connectors can be decreased to help compensate for the additional capacitance. Board-to-board connectors, however, may not be used, as the net capacitance from each board's parasitics will quickly overwhelm the semi-buffered TWL1200 SDIO lines, causing SDIO communication to and from the TWL1200 to break down. For best results, system designers must keep the capacitance for each SDIO line to less than 20 pF, as is stated in the Secure Digital specification. This helps to optimize data rates and provide increased noise margins for high-speed signal lines on the TWL1200 PCB design.

Once all of the TWL1200 SDIO lines are complete, the layout design should continue using the above guidelines for the slow clock, Bluetooth (BT) Universal Asynchronous Receiver/Transmitter (UART), and Pulse Code Modulation (PCM) audio traces. Finally, routing can proceed with the low-speed control signals traces, ideally on the bottom layer.

2.3.5 Vias

In routing out the inner balls of the TWL1200 package, it may prove quite difficult to keep sufficient clearance between multiple traces. Having multiple layers grants the designer the flexibility to route signals out from under the package using vias. As mentioned earlier, good results can be achieved by routing all of the high-speed signals on the top layer and keeping via usage reserved for power, ground, and low-speed signal connections only. If high-speed signal vias are unavoidable, blind or buried vias can be used instead, but they will contribute to increased cost for the PCB design. Blind vias connect an outer layer to an internal layer without routing through the entire board, while buried vias provide connections between internal layers only. This preventative helps eliminate signal reflection caused by through-hole vias, which create multilayer stubs. Examples of blind, buried, and traditional vias are shown in Figure 8.

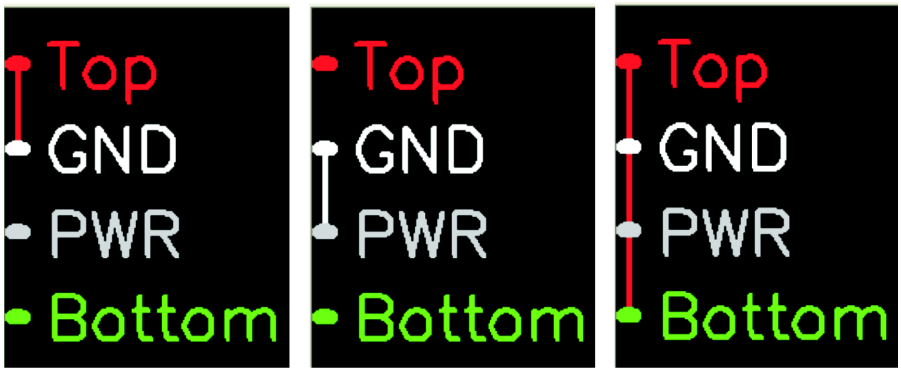

Figure 8. Cross-Sectional View of Blind, Buried, and Traditional Vias

Via sizing is another critical aspect to consider in all PCB designs. A good TWL1200 board design uses a pad size of 250 µm and a hole size of 75 µm when routing from layer 1 to layer 2. Similarly, vias routed from layer 2 to layer 3 or layer 3 to layer 4 should use a pad size of 150 µm and a hole size of 75 µm. Proper via sizing for different layer routes underneath the TWL1200 ball grid array package outline is shown in Figure 9.

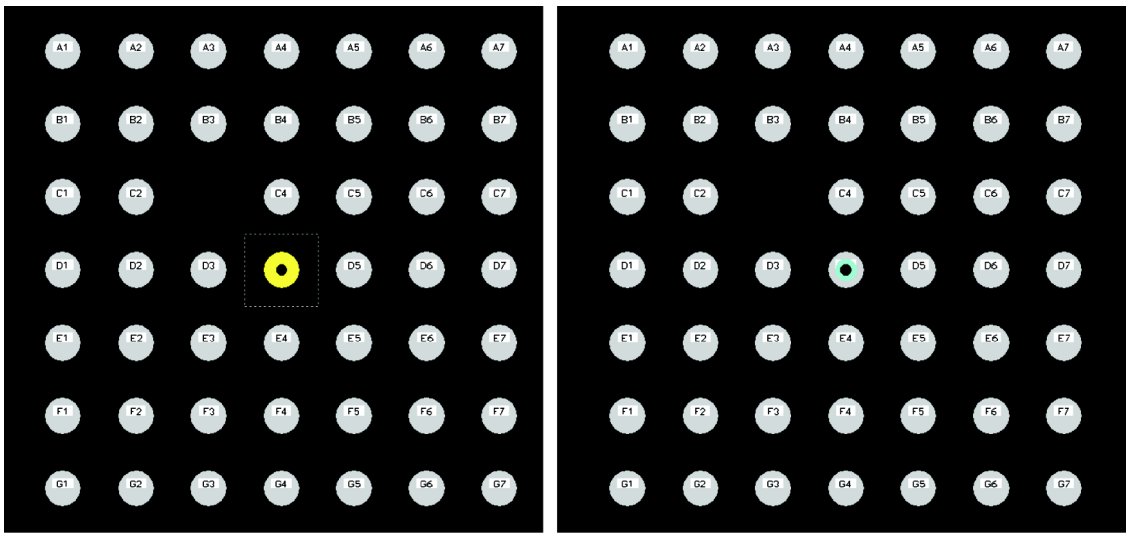

Figure 9. 250-µm and 150-µm Via Sizing for TWL1200 and WL1271/3 Pads

This rule also applies for vias outside of the TWL1200 package outline, except that the via pad size should be increased to 275 µm.

2.4 Power Supply Bypassing

Proper power supply bypassing must always be practiced to decouple unwanted noise from local integrated circuits (ICs). This is typically accomplished by placing low equivalent series resistance (ESR) capacitors as close to the power supply pins of a given IC as PCB real estate allows. Low ESR capacitors guarantee that an ideal low-impedance bypass to ground is available for efficient decoupling of high-frequency power-supply noise. Although many types of capacitors are available, low ESR ceramic capacitors appear to be the dominant choice nowadays. Other materials, such as tantalum, offer alternatives to ceramics and may be viable depending on application needs. It is always best to consider size, cost, ESR, and maximum voltage tolerance before proceeding with design implementation.

For decoupling needs, it is equally important to look at desired capacitance. The critical point to remember is that higher capacitance effectively decouples lower frequencies and lower capacitance achieves the same for higher frequencies. Thus, best practice dictates that small banks of different capacitor values be used across the PCB. Generally, 1-µF to 10-µF capacitors should be placed at the outputs of voltage regulators and at any connectors where external power is supplied to the PCB. Similarly, 0.1-µF to 0.01-µF capacitors should be connected to all IC power pins to facilitate effective bypassing. Via connections made to any of these capacitor terminals should always be placed in pairs of two or more to reduce equivalent series inductance (ESL). In addition, connections should be routed so that current is forced to flow across the capacitor terminals before reaching its intended destination. Component placement is just as crucial to stable power design. Capacitors should always be placed as close as possible to the respective power supply pin of the device it is decoupling. Because these capacitors are seen as a local source of additional supply current for switching ICs, it is best to keep the distance between them as small as possible. An example of proper decoupling design for the TWL1200 is shown in Figure 10.

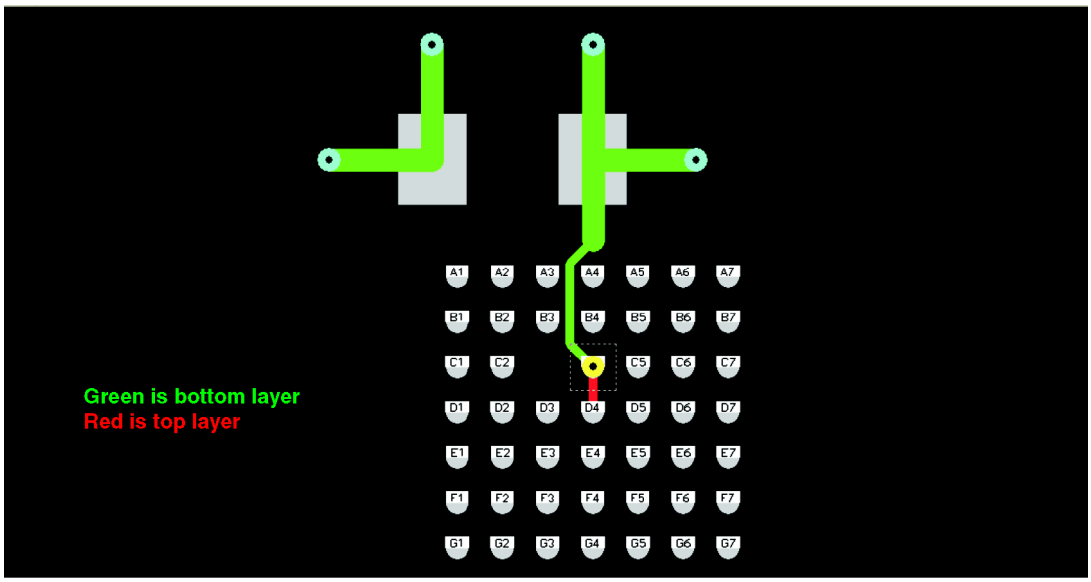

Figure 10. Proper TWL1200 Power Supply Decoupling

3 TWL1200 Reference Design Schematic

A reference schematic for the TWL1200 design is shown in Figure 11.

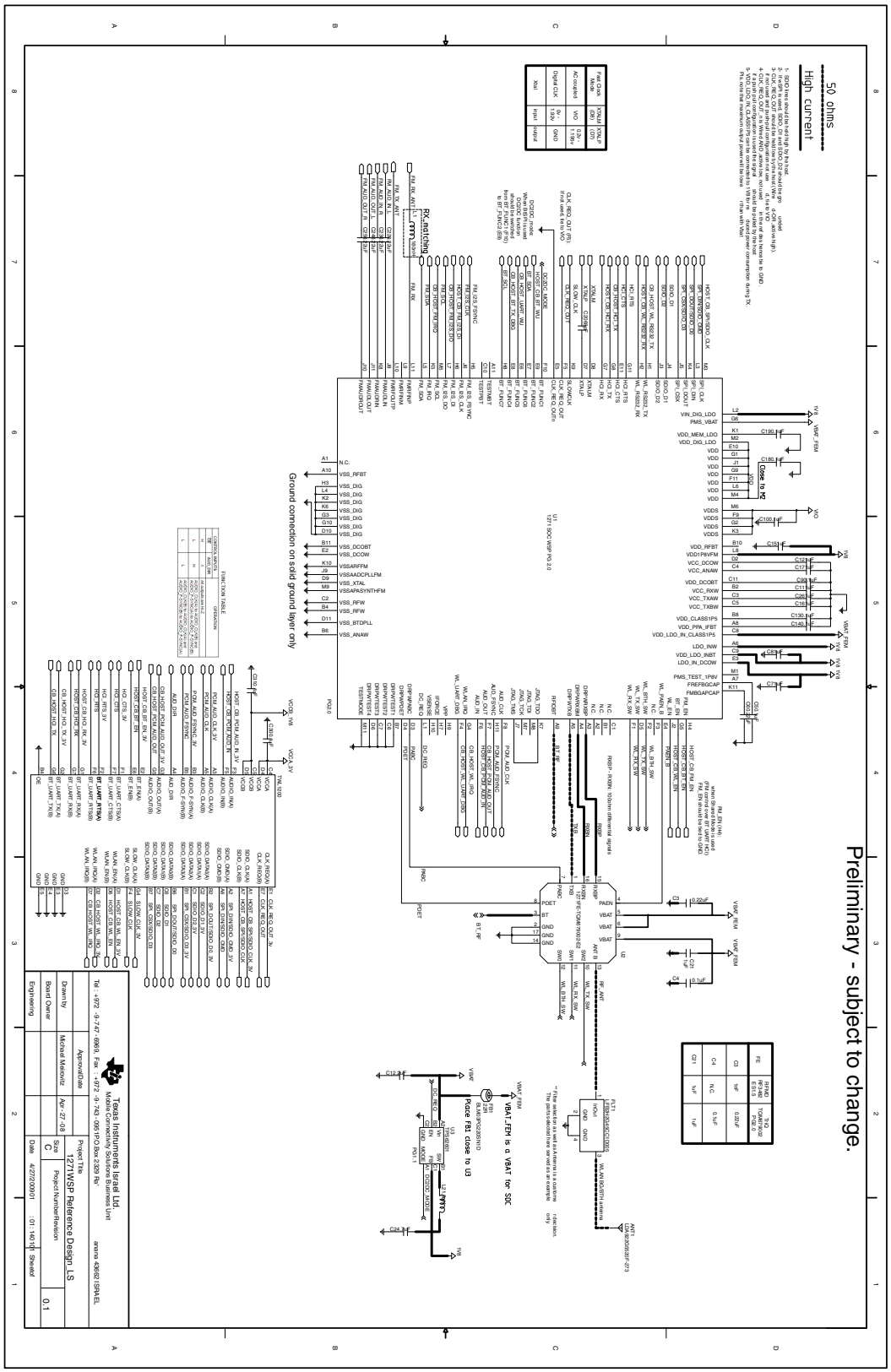

Figure 11. TWL1200 Reference Design

4 References

1. *WiLink 6.0 PCB Design Guidelines* (SWAA043)
2. *Simultaneous Switching Performance of TI Logic Devices* (SZZA038)
3. *The Bypass Capacitor in High-Speed Environments* (SCBA007)
4. TWL1200 (SDIO, UART, and Audio Voltage Translation Transceiver) data sheet (SCES786)
5. WL1271/3 (WiLink 6.0 Single-Chip WLAN/BT/FM Device) data sheet (SWAS017)
6. *High-Speed Digital Design: A Handbook of Black Magic* (Johnson, Howard W., 1993)

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