Logic Solutions for IEEE Std 1284

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Abstract

Since the creation of IEEE Std 1284, designers have been using this signaling method to interface between the personal computer and peripheral devices. Bulky discrete components, such as termination and pullup resistors and capacitors, were used extensively. To integrate into single-chip solutions that comply with IEEE Std 1284, Texas Instruments (TI™) offers three bus-interface devices that provide board-area savings and flexible level-type selection.

Introduction

This application report presents a brief overview of IEEE Std 1284-1994, provides information on each device available from TI that is a bus-interface solution for this standard, and discusses how to use the devices in applications. TI offers the SN74ACT1284, which is a 7-bit bus-interface transceiver, and the SN74LVC161284 and SN74LV161284, which are 19-bit bus-interface transceivers, as discrete IEEE Std 1284 bus-interface solutions.

Brief Overview of IEEE Std 1284

IEEE Std 1284, “Standard Signaling Method for a Bidirectional Parallel Peripheral Interface for Personal Computers,” is a high-speed, high-integrity parallel-port method for a bidirectional peripheral interface for personal computers. This standard was developed to provide an open path for communications between computers and peripherals. Furthermore, it recommends new electrical interfaces, cabling, and interface hardware that provides improved performance, while retaining backward compatibility.

Purpose and Benefits of IEEE Std 1284

With increased technology development in the personal computer (PC), a need for improved parallel-port performance has emerged. Pre-existing methods used a wide variety of hardware and software products, each with unique and incompatible signaling schemes. Using existing parallel-port architecture, the maximum data transfer rate is about 150 kbyte/s, and external cables are limited to 6 feet.

IEEE Std 1284 was created because of the need for an existing defined standard for bidirectional parallel communication between the PC and printing peripherals. Being backward compatible with the old Centronics specifications, this standard offers more functionality and performance for new PC and peripheral products. Data rates are increased to greater than 1Mbyte/s and maximum cable length is increased to 32 feet for the defined cable type.

IEEE Std 1284 Data Transfer Modes

IEEE Std 1284 defines five modes of data transfer. Not all modes are required in all peripherals; forward is defined as data transfer from host to peripheral, and reverse is defined as data transfer from peripheral to host. The bidirectional mode provides both forward and reverse transfer mode within the same operational mode. The modes are:

- Compatibility Mode: This is the basic mode of operation for all parallel communications. It is asynchronous, byte wide, forward direction, and offers 50-kbyte/s to 150-kbyte/s data-transfer rate.
- Nibble Mode: This asynchronous, reverse-channel mode provides two sequential, 4-bit nibbles to the host. It is used with the compatibility mode to implement a bidirectional channel. The data transfer rate is the same as in the compatibility mode.
- Byte Mode: This mode allows the transfer of data in the reverse direction if the data lines are bidirectional. The data transfer rate is the same as in the compatibility and nibble modes.
- Enhanced Parallel Port (EPP): This mode allows high-speed transfers of bytes in either direction. EPP is ideal for real-time-controlled peripherals, such as network adapters, data acquisition, portable hard drives, and other devices.
- Extended Capabilities Port (ECP): The ECP protocol was proposed as an advanced mode for communication with printer and scanner peripherals. Like the EPP protocol, ECP provides a high-performance, bidirectional communication path between the host and peripheral. ECP and EPP modes are ten times faster than the compatibility, nibble, and byte modes.

IEEE Std 1284 Driver Specification

IEEE Std 1284 specifies characteristics of parallel-port drivers and receivers, and describes two types of interfaces:

- Level I (open drain): Level I devices are designed to be consistent with the pre-existing installed devices. Applications using Level I should not be operated in the high-speed advanced modes, but should take advantage of reverse-channel capabilities of the standard.
- Level II (totem pole): Level II devices have stronger drivers and inputs with hysteresis. They are designed to operate in the advanced mode where a longer cable and higher data rates prevail. Level II offers better performance, while remaining compatible with the original interface.

IEEE Std 1284 Connectors

Three interface connectors defined in IEEE Std 1284 are:

- IEEE Std 1284-A: This is the existing DB25 connector, used primarily on the host side.
- IEEE Std 1284-B: This is the existing 36-pin, 0.085-inch centerline connector, used only on the peripheral side.
- IEEE Std 1284-C: This connector is a new 36-pin, 0.050-inch centerline connector recommended by IEEE Std 1284 that is used on both host and peripheral sides.

Since A- and B-type connectors do not have the same number of pins, Figures 1 and 2 detail pin connections for communication between the PC and peripheral. These connections (A host and B peripheral; A host and C peripheral) are the most commonly accepted in the industry.

As recommended in IEEE Std 1284, using the C-type connector on both host and peripheral sides provides a high-speed, high-integrity parallel port for reliable bidirectional communication. Figure 3 shows the straightforward connection between the two ports.

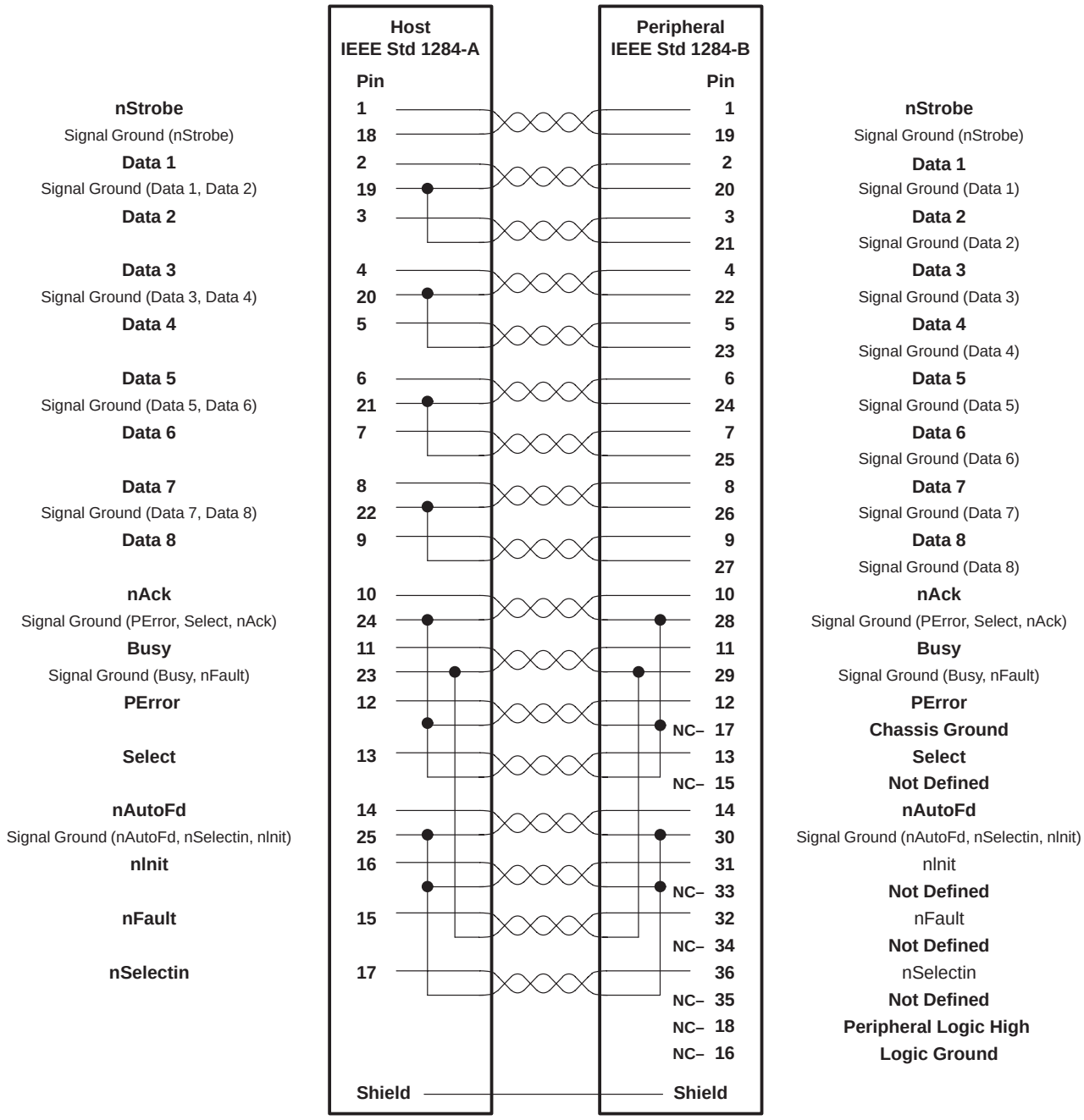


Figure 1. IEEE Std 1284-A (Host) to IEEE Std 1284-B (Peripheral) Wiring Diagram

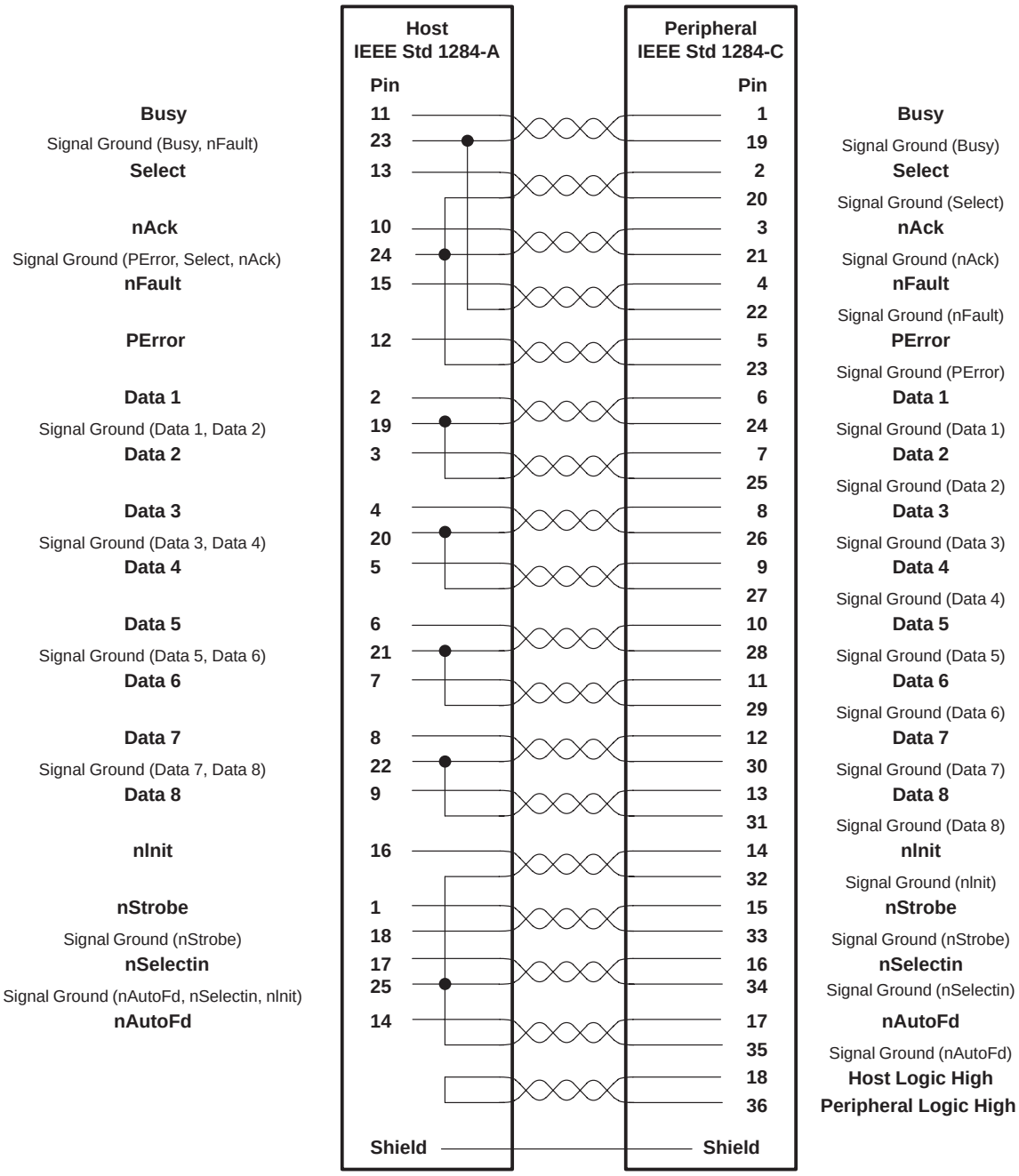


Figure 2. IEEE Std 1284-A (Host) to IEEE Std 1284-C (Peripheral) Wiring Diagram

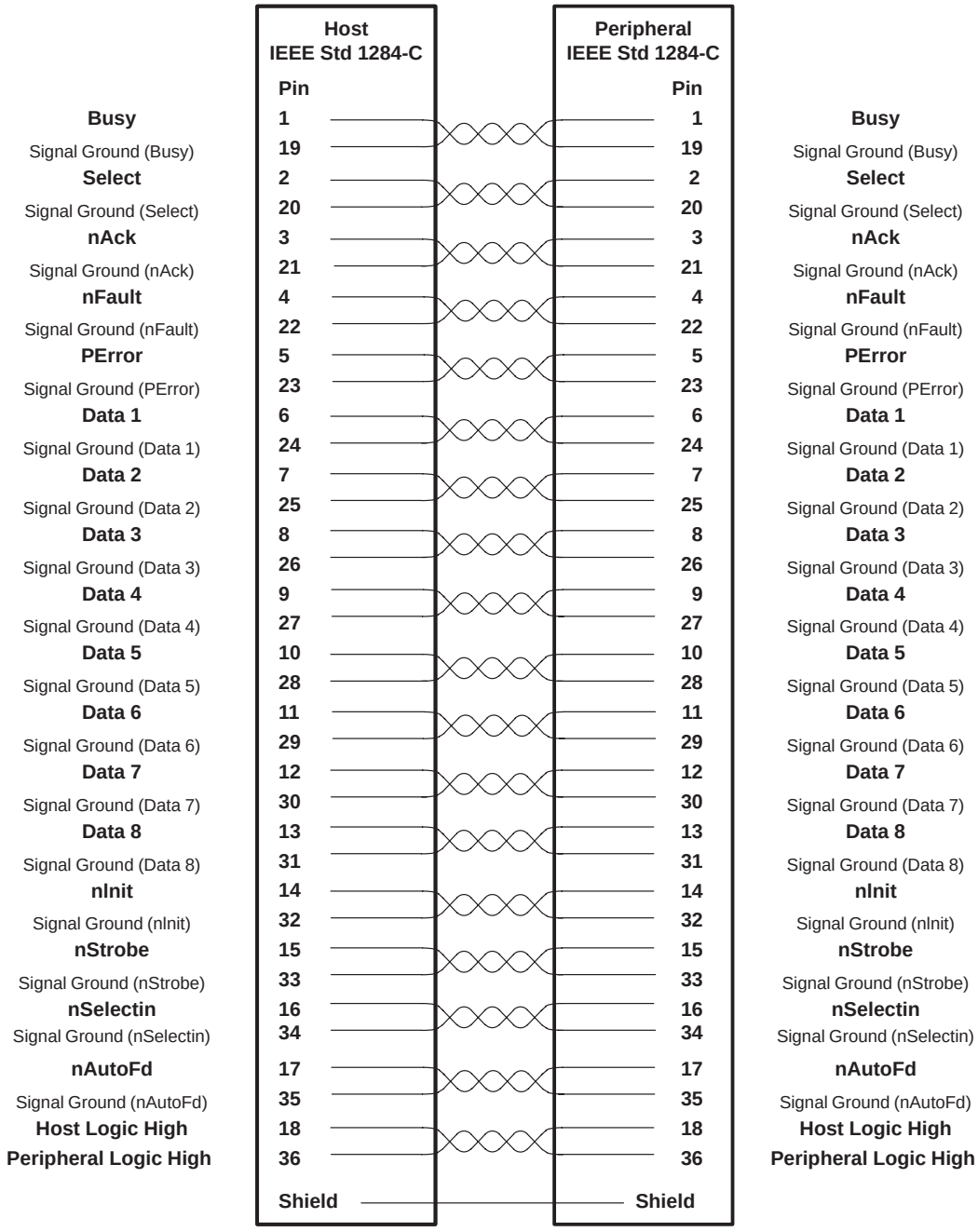


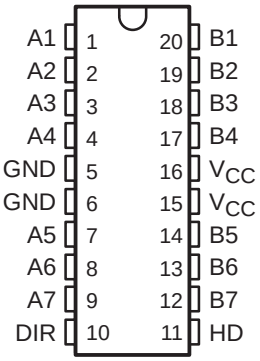
Figure 3. IEEE Std 1284-C (Host) to IEEE Std 1284-C (Peripheral) Wiring Diagram

Device Information

TI offers three bus-driver solutions that comply with the IEEE Std 1284 specification: SN74ACT1284, SN74LVC161284, and SN74LV161284. These devices can be used in the ECP mode to provide an asynchronous, bidirectional, parallel peripheral interface for personal computers. These devices allow data transmission in the A-to-B direction or B-to-A direction, depending on the logic level of the direction-control (DIR) pin. The output drive mode is determined by the high-drive (HD) control pin. HD enables the outputs (B and Y side only) to switch from open collector to totem pole. The A side outputs have totem-pole outputs only. This meets the drive requirements as specified in the IEEE Std 1284-I (level-1 type) and IEEE Std 1284-II (level-2 type) parallel peripheral-interface specifications. All these devices have two supply voltages, one for the cable side, and the other for the logic side. To reduce the chance of faulty signals being transferred over the system's parallel port, all these devices feature a finely tuned Output Edge-Rate Control (OEC™) circuit and an enhanced input hysteresis circuit.

The pinouts and function tables of these devices are given in Figures 4 and 5 and in Tables 1 and 2, respectively.

SN54ACT1284 . . . J OR W PACKAGE
SN74ACT1284 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ACT1284 . . . FK PACKAGE
(TOP VIEW)

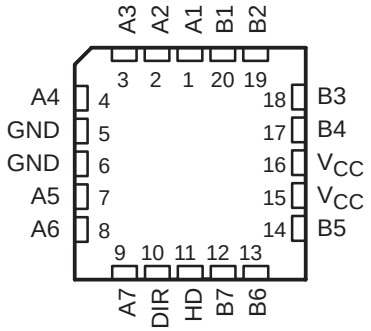


Figure 4. Pinout of SN54/SN74ACT1284

OEC is a trademark of Texas Instruments Incorporated.

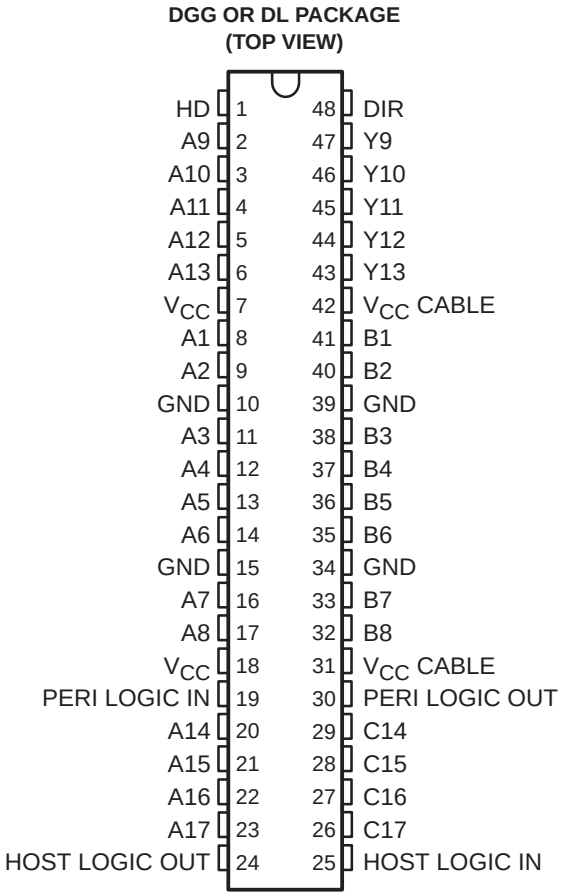


Figure 5. Pinout of SN74LV161284 and SN74LVC161284

Table 1. Function Table for SN74ACT1284

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A to B: Bits 5, 6, 7
		Totem pole	B to A: Bits 1, 2, 3, 4
L	H	Totem pole	B to A: Bits 1, 2, 3, 4 and A to B: Bits 5, 6, 7
H	L	Open drain	A to B: Bits 1, 2, 3, 4, 5, 6, 7
H	H	Totem pole	A to B: Bits 1, 2, 3, 4, 5, 6, 7

Table 2. Function Table for SN74LV161284 and SN74LVC161284

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A9–A13 to Y9–Y13 and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	B1–B8 to A1–A8 and C14–C17 to A14–A17
L	H	Totem pole	B1–B8 to A1–A8, A9–A13 to Y9–Y13, PERI LOGIC IN to PERI LOGIC OUT, and C14–C17 to A14–A17
H	L	Open drain	A1–A8 to B1–B8, A9–A13 to Y9–Y13, and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	C14–C17 to A14–A17
H	H	Totem pole	A1–A8 to B1–B8, A9–A13 to Y9–Y13, C14–C17 to A14–A17, and PERI LOGIC IN to PERI LOGIC OUT

Features and Benefits

Tables 3 and 4 summarize the features and corresponding benefits for three TI devices that are IEEE Std 1284 compliant.

Table 3. Features and Benefits of the SN74ACT1284

FEATURES	BENEFITS
Flow-through architecture	Optimizes printed circuit board layout
Center-pin V_{CC} and GND configuration	Minimizes high-speed switching noise
Software configurable to IEEE Std 1284-I (level-1 type) and IEEE Std 1284-II (level-2 type) electrical specifications	Easy level-type selection
A-to-B and B-to-A transmission for bits 1, 2, 3, and 4	Configurable data flow

Table 4. Features and Benefits of the SN74LV161284 AND SN74LVC161284

FEATURES	BENEFITS
Integrated 1.4-kΩ pullup resistors on all open-drain cable-side outputs†	Eliminates the need for discrete resistors
Software-configurable to IEEE Std 1284-I (level-1 type) and IEEE Std 1284-II (level-2 type) electrical specifications	Easy level-type selection
Flow-through architecture	Optimizes printed circuit board layout
V_{CC}CABLE from 3 V to 5.5 V, V_{CC} from 3 V to 3.6 V (SN74LVC161284 only)	Wide voltage range
4.5-V to 5.5-V V_{CC} and V_{CC}CABLE (SN74LV161284 only)	Single supply
Eight bidirectional data bits, five cable drivers and four receivers	Complete peripheral solution
Integrated PMOS transistors between V_{CC} and cable-side data and receiver outputs‡	Avoids back-drive current
Integrated 33-Ω termination resistors to all cable-side outputs	Eliminates the need for discrete resistors
Dedicated buffers for Peripheral Logic High and Host Logic High signals§	Complete peripheral solution

† Pullup resistors ensure operation with a Level I compatible device and provide sufficient voltage and timing margins as specified by IEEE Std 1284. In addition, the pullup resistors add margin for noisy cable environments.

‡ Avoiding back-drive current keeps the peripheral from being powered up by the host when the peripheral is off and allows for a 5-V system to be connected to the cable side. Laboratory experiments using TI's SN74LVC161284 and a competitor's 1284 transceiver show how the two devices compare, while simulating a typical PC-to-peripheral application. In this situation, a '161284 is used on the peripheral.

§ Hosts and peripherals indicate their readiness to communicate by asserting Host Logic High and Peripheral Logic High, respectively. All hosts and peripherals with IEEE Std 1284-C connectors shall provide Host Logic High and Peripheral Logic High. Because devices with IEEE Std 1284-A or IEEE Std 1284-B connectors may or may not support Host Logic High or Peripheral Logic High, there are no reliable means of initiating a transfer.

Performance Comparison

As the Super I/O transmits a high level to the peripheral via the cable, the ’161284 on the printer side receives the signal because it is configured as a receiver. In TI’s laboratory, the host PC side is simulated by driving +5 V to the ’161284 receiver. Any back-drive current is measured and plotted as the peripheral device is being powered down and is receiving a high-level input (H level). The experiment is repeated for the competitor’s part. Figure 6 shows the test setup. Results, plotted on Figures 7, 8, 9, and 10, show the superior performance of the TI SN74LVC161284 vs a competitor’s equivalent device.

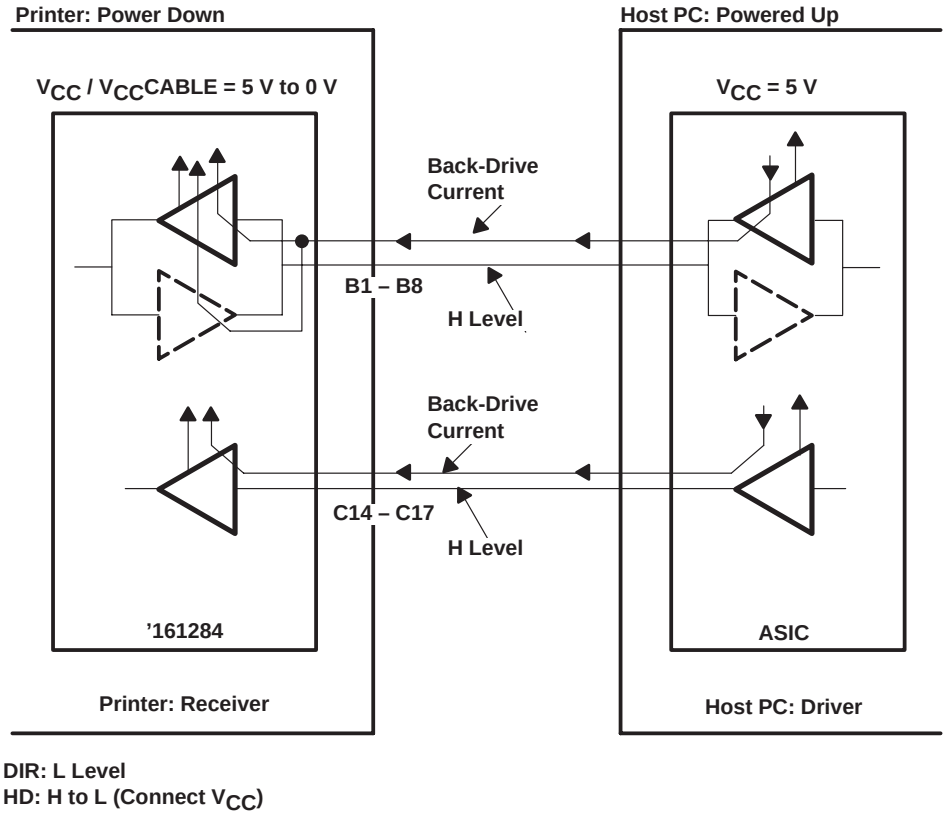


Figure 6. Test Setup for Back-Driving Current

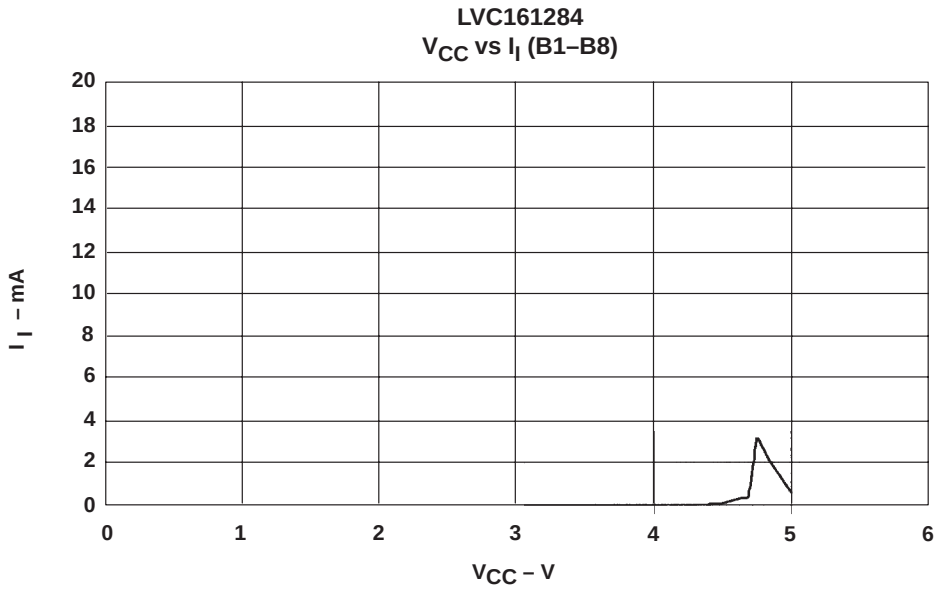


Figure 7. Back-Driving Current for LVC161284 for B1 to B8. (V_{CC} = V_{CC}CABLE = 5 V to 0 V)

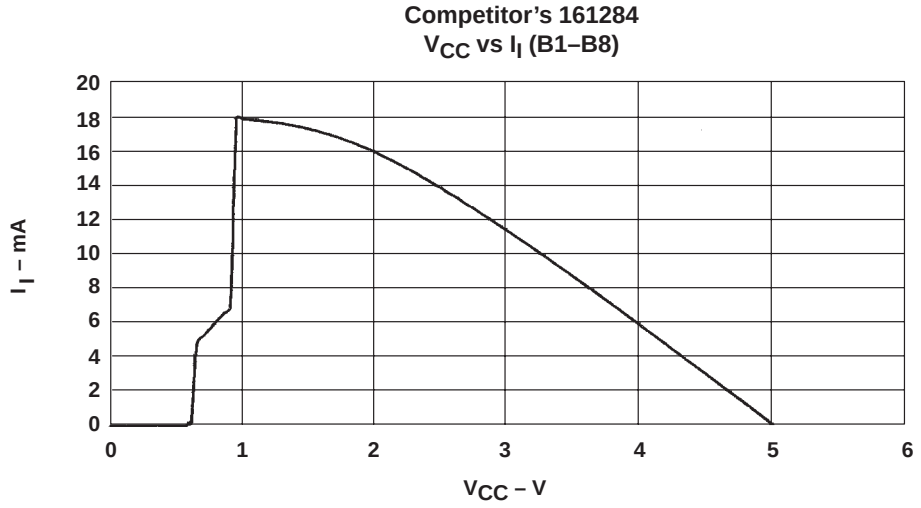


Figure 8. Back-Driving Current for Competitor's 161284 for B1 to B8. (V_{CC} = V_{CC}CABLE = 5 V to 0 V)

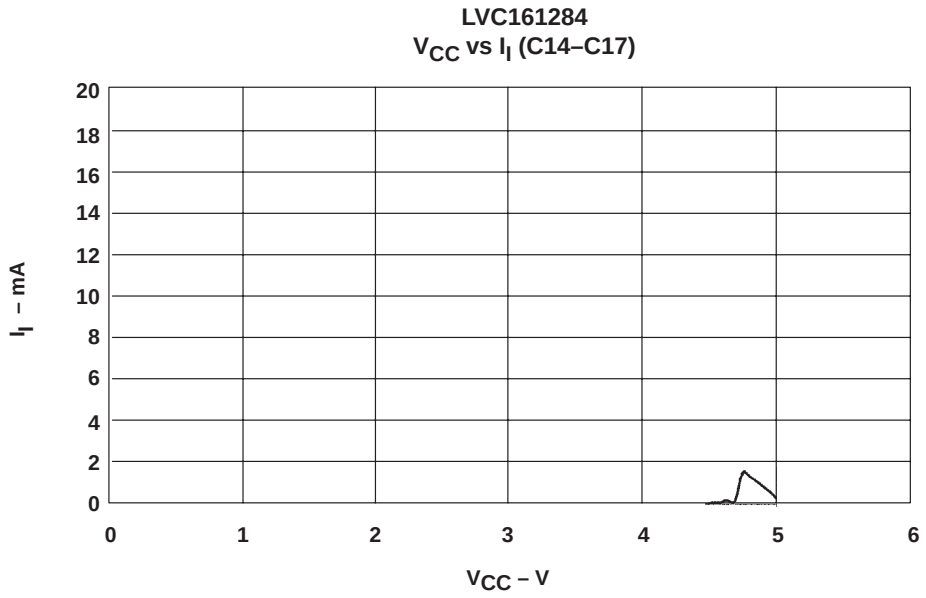


Figure 9. Back-Driving Current for LVC161284 for C14 to C17. (V_{CC} = V_{CC}CABLE = 5 V to 0 V)

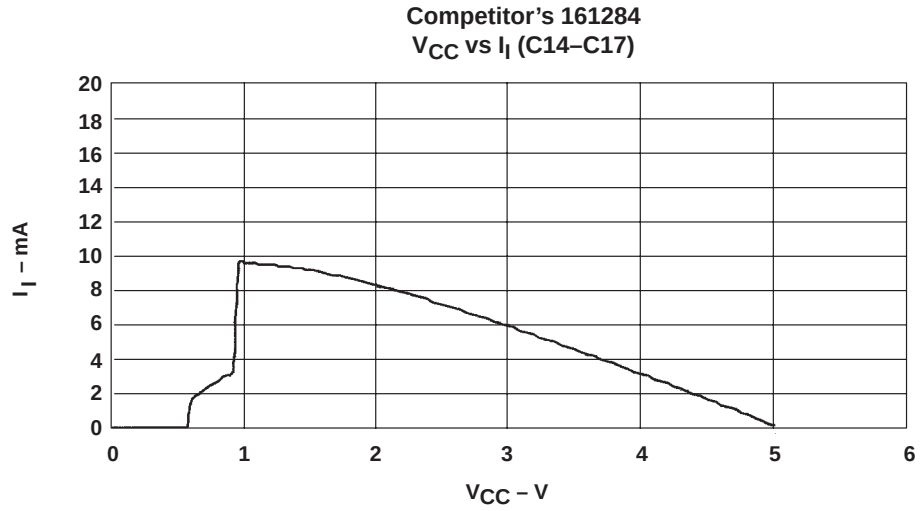


Figure 10. Back-Driving Current for Competitor's 161284 for C14 to C17. (V_{CC} = V_{CC}CABLE = 5 V to 0 V)

Table 5 provides a comparison of characteristics of the SN74ACT184, SN74LVC161284, and SN74LV161284 devices.

Table 5. Comparisons of Device Characteristics

DEVICE CHARACTERISTICS	SN74ACT1284	SN74LVC161284	SN74LV161284
Number of pins	20	48	48
Number of data bits	Four bidirectional bits	Eight bidirectional bits	Eight bidirectional bits
Number of control and status bits	Three unidirectional bits for control or status	Five driver and four receiver for status and control bits, one receiver for host logic, and one driver for peripheral logic	Five driver and four receiver for status and control bits, one receiver for host logic, and one driver for peripheral logic
Supply voltage	4.7 V ≤ V_{CC} ≤ 5.5 V	3 V ≤ V_{CC} ≤ 3.6 V 3 V ≤ V_{CC}CABLE ≤ 5.5 V V_{CC}CABLE ≥ V_{CC}	4.5 V ≤ V_{CC} ≤ 5.5 V 4.5 V ≤ V_{CC}CABLE ≤ 5.5 V V_{CC}CABLE ≥ V_{CC}
Temperature range	0°C to 70°C		–40°C to 85°C
Available package types	SOIC (DW) SSOP (DB) TSSOP (DW) DIP (N)	Plastic 300-mil Shrink Small-Outline (DL) Thin Shrink Small-Outline (DGG)	Plastic 300-mil Shrink Small-Outline (DL) Thin Shrink Small-Outline (DGG)
Input hysteresis	All inputs have hysteresis to provide noise margin		
Pullup resistors	No pullup resistor is included	1.4-kΩ pullup resistor is included in all cable-side pins, except for Host Logic and Peripheral Logic	1.4 k-Ω pullup resistor is included in all cable-side pins, except for Host Logic and Peripheral Logic
Termination resistors	No internal series termination resistor included	33-Ω series resistor integrated into cable-side data output	33-Ω series resistor integrated into cable-side data output

Application Information

Why the IEEE Std 1284 Driver is Needed

Before IEEE Std 1284, there was no defined electrical specification for driver, receiver, termination, and capacitance requirements that required compatibility between devices. Host adapters and peripherals were built with different pullup values on the control lines, open-collectors or open-drains, and totem-pole drivers for the data and control lines. Often, up to 10,000-pF capacitors on the data and strobe lines were used. Figure 11 shows a typical pre-IEEE Std 1284 application host solution. All capacitors and pullup and termination resistors are replaced by TI's discrete integrated bus-interface solution (dashed box around components in Figure 11) that provides efficient designs of parallel-port communication between the PC and peripheral.

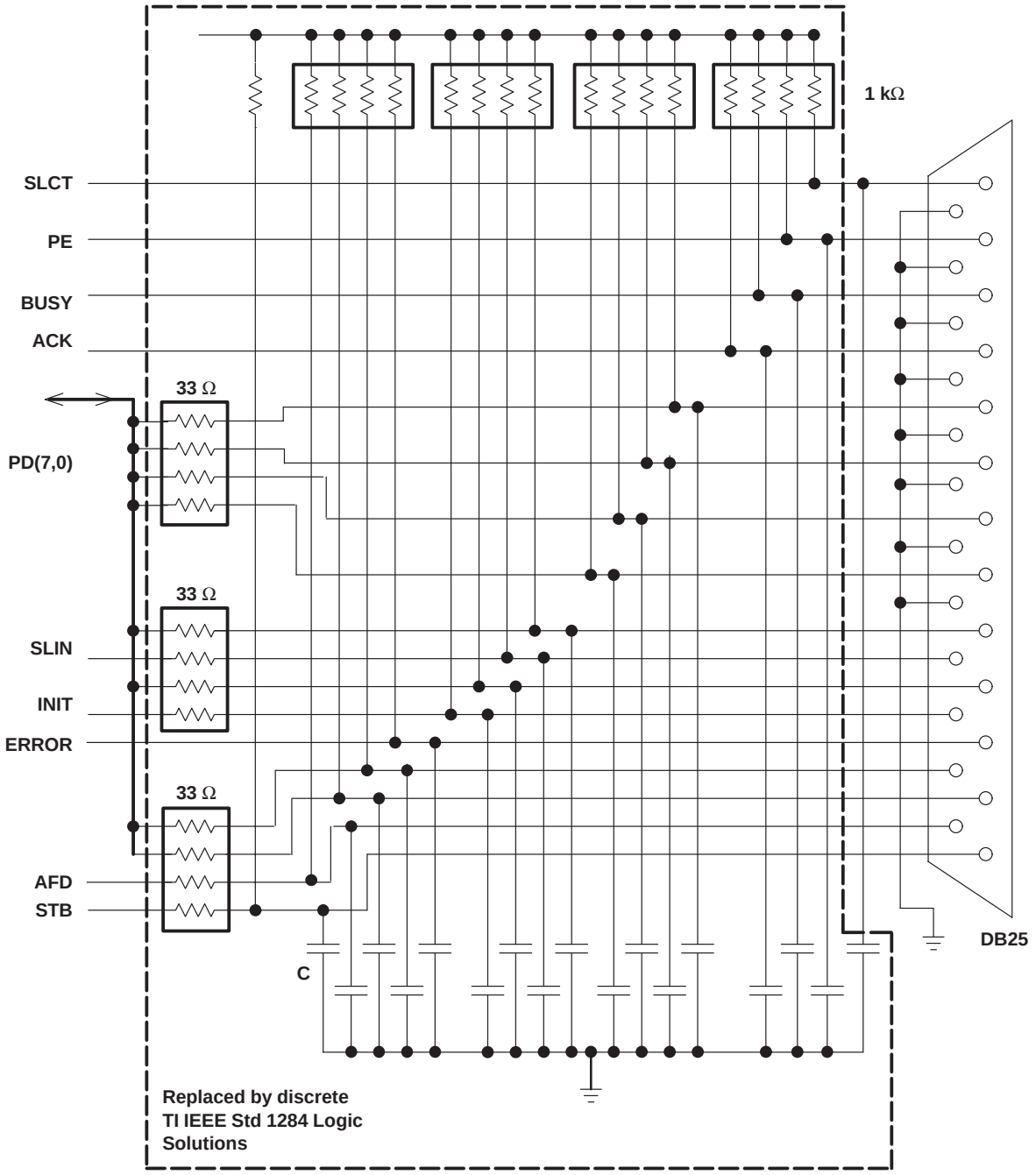


Figure 11. Pre-IEEE Std 1284 Parallel-Port Host Solution

IEEE Std 1284 Parallel-Port Solutions Using TI Bus-Interface Devices

Figure 12 is a basic block diagram of an IEEE Std 1284 parallel port. Only one SN74LV161284 or SN74LVC161284 is used per side, but two SN74ACT1284 devices are required per port.

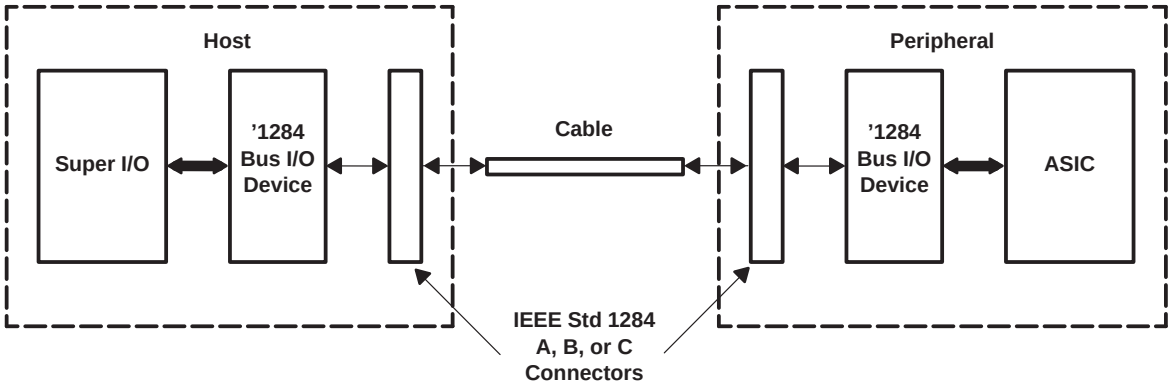


Figure 12. Block Diagram of Parallel Interface Port Between the PC and Peripheral

To illustrate how to apply the SN74ACT1284 as shown in Figure 12, Figures 13 and 14 explicitly show all data, control, and status lines from the Super I/O on the host side to the ASIC on the peripheral. The designer must decide which connector is suitable for a particular application and to what level type to set the devices using the HD pin.

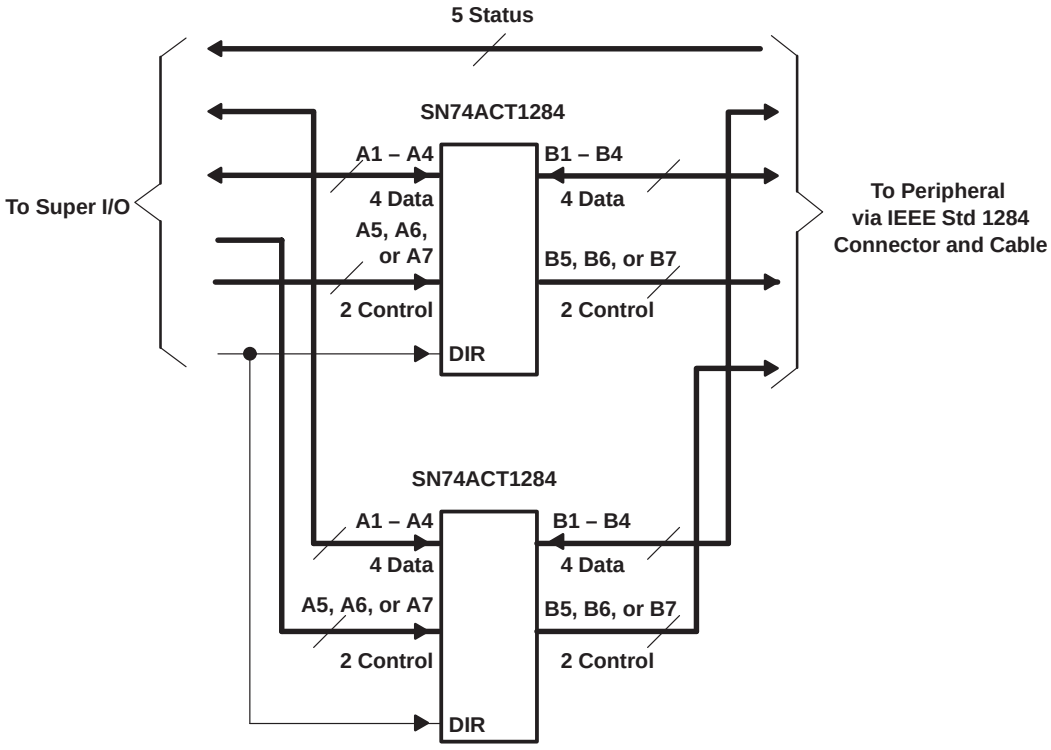


Figure 13. IEEE Std 1284 Host Solution Using Two SN74ACT1284 Devices

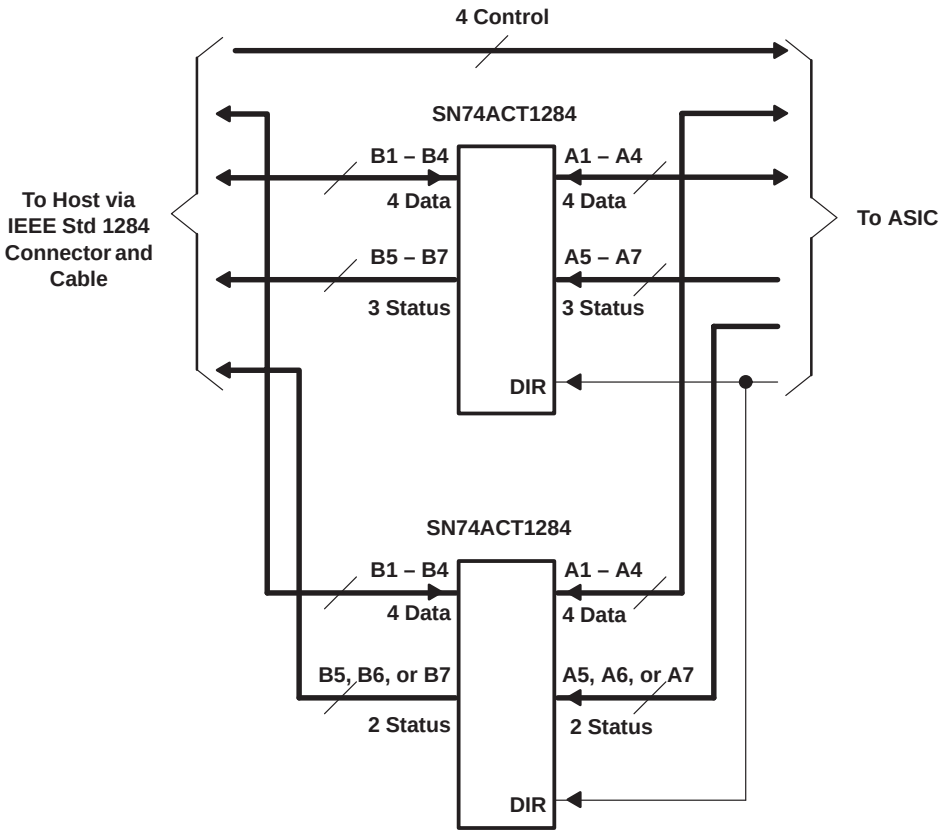


Figure 14. IEEE Std 1284 Peripheral Solution Using Two SN74ACT1284 Devices

While the SN74ACT1284 provides an acceptable two-chip solution, the SN74LV161284 and SN74LVC161284 devices provide optimum applicability—specifically, on the peripheral side. Figures 15 and 16 show all data, control, and status lines from the Super I/O on the host to the ASIC on the peripheral using these 19-bit bus interface devices.

Note that Host Logic In (pin 25) on the host side is connected via the IEEE Std 1284 connector and cable to Peri Logic Out (pin 30) on the peripheral. Likewise, Peri Logic Out (pin 30) on the host is connected the IEEE Std 1284 connector and cable to Host Logic In (pin 25) on the peripheral.

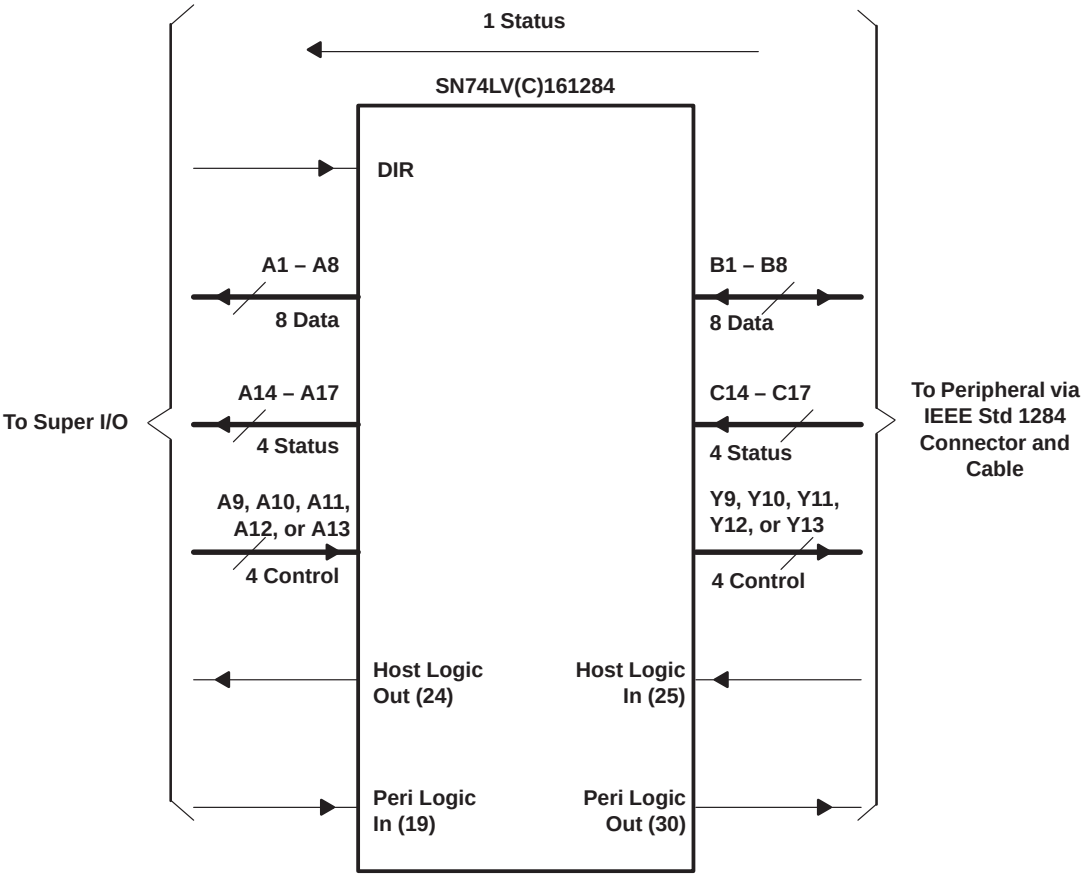


Figure 15. IEEE Std 1284 Host Solution Using the SN74LV161284 or SN74LVC161284

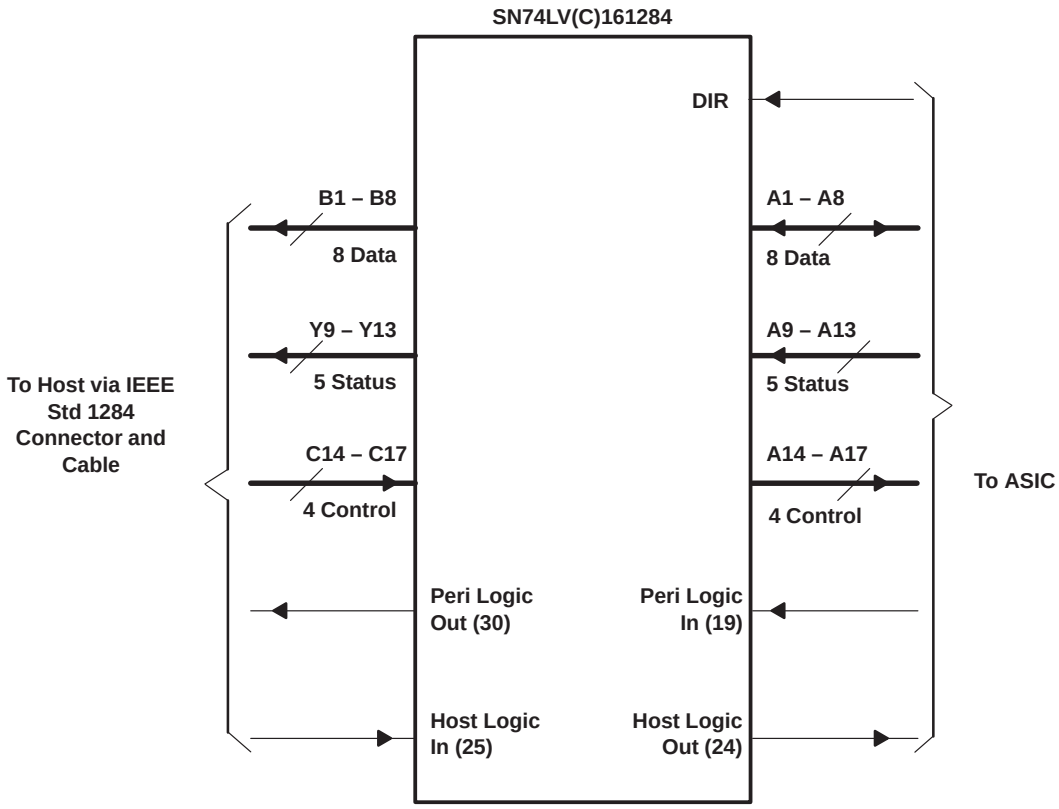


Figure 16. IEEE Std 1284 Peripheral Solution Using the SN74LV161284 or SN74LV161284

Conclusion

This report gives a brief description of IEEE Std 1284-1994 and TI's logic solutions that conform to this standard. TI offers the bus interface SN74ACT1284, SN74LVC161284, and SN74LV161284 devices as complete solutions for a high-performance parallel port, and, as shown by laboratory data, the '161284 devices offer superior performance in back-drive current generation when compared to the competition. Furthermore, this report guides designers in choosing the correct bus interface device in their IEEE Std 1284 applications.

Acknowledgment

The authors of this report are Nadira Sultana and Manny Soltero.

Commonly Asked Questions

1. How is the SN74LVC161284 used with a parallel port?

   The *Application Information* section of this application report, in conjunction with Figures 15 and 16, explains how to use the 'LVC161284 with the parallel port, whether it is on the host side or on the peripheral side.

2. If somebody wants an IEEE Std 1284 compliant design, is an IEEE Std 1284 transceiver required? What is so special about the SN74ACT1284, SN74LV161284, and SN74LVC161284?

   To comply fully with IEEE Std 1284, one of TI's IEEE Std 1284 transceiver solutions should be used. Separate device descriptions are discussed in full, and one can see that these devices are the optimum choice.

3. How does the back-drive current of these devices compare to our competition?

   The *Features and Benefits* section of this application report shows the excellent performance of the back-driving current of the SN74LVC161284. The SN74LV61284 has similar performance.

4. IEEE Std 1284 calls for series termination resistors on the driver lines before the pullup resistors. What is TI's recommendation for those termination resistors? Are they already included in the device (SN74ACT1284, SN74LVC161284, SN74LV161284)?

   The SN74ACT1284 does not have any series termination resistors, but the other two parts have 33-Ω series termination resistors included in the part to conform to IEEE Std 1284. An external 33-Ω series resistor must be connected if the SN74ACT1284 is used.

5. What is the driver configuration for an IEEE Std 1284 level-1 driver?

   The driver configuration for an IEEE Std 1284 level-1 driver is open drain.

6. Can the SN74LVC161284 be used on the host as well as on the peripheral side?

   Yes, the SN74LVC161284 can be used on the host side, but it is optimized for use on the peripheral side. However, on the host side, one status line cannot be buffered through the device. Figures 15 and 16 show this in detail.

7. If someone does not want to use Host Logic and Peri Logic, what should be done with those terminals—tie them high, or low, or leave them open?

   If the signal from the transmitting side is not to be used on their end, leave it open on the receiving side. However, the other signal should be driven true so that the other end of the cable sees it and can use it for better signal reliability.

Glossary

A

ASIC	Application-Specific Integrated Circuit

E

ECP	Extended-Capabilities Port
EPP	Enhanced Parallel Port

H

HD	High Drive

O

OEC™	Output Edge-Rate Control

P

PC	Personal Computer